SECTION VII

SERVICE

7-1 INTRODUCTION

This section contains general information, disassembly/reassembly instructions, and service information – circuit descriptions, schematics, parts locator diagrams, and troubleshooting data – for the overall sweep generator and individual printed circuit boards (PCBs). This service information is organized as shown in Table 7-1 (facing page).

7-2 GENERAL INFORMATION

7-2.1 Printed Circuit Board (PCB) Exchange Program

WILTRON has an exchange program that includes most of the 6600A Series PCBs. Upon request, WILTRON will immediately ship a replacement for any sweep generator PCB covered by this program. The customer has 30 days in which to return the defective PCB. Contact Customer Service at 415-969-6500 to make arrangements for an exchange.

7-2.2 Recommended Test Equipment for Troubleshooting

A list of the recommended test equipment for troubleshooting the sweep generator is provided in Table 7-2.

7-3 6600A SERIES PROGRAMMABLE SWEEP GENERATOR, REMOVAL AND REINSTALLATION INSTRUCTIONS

Instructions for the removal and reinstallation or the disassembly and reassembly of certain 6600A Series Sweep Generator components and subassemblies are provided in paragraphs 7-3.1 thru 7-3.5.

7-3.1 Front Panel Assembly, Removal and Reinstallation Instructions

a. Removal.

1. Turn off ac power.
2. Remove the top, bottom, and side covers of the basic frame as follows:
   (a) Remove the four corner brackets from the rear panel (Figure 7-1).
   (b) Slide the covers to the rear and remove.
3. Stand the sweep generator on its side, with the RF Deck up.
4. Disconnect the cable connector from A14P37 (Figure 7-2).
5. Using a 3/32-inch hex wrench, remove the four corner and two mid-panel screws securing the front panel assembly to the basic frame (Figure 7-3).
6. Reposition the sweep generator top-side up (sitting on its feet); gently push the front panel assembly away from the front of the basic-frame assembly.
7. Disconnect the ribbon connectors from P5, P6, and P7 on the A12 Microprocessor PCB. Use care to avoid bending the connector pins.

b. Reinstallation. The reinstallation procedure for the front panel assembly is a reversal of the removal procedure.

CAUTION

To prevent chafing, insure that the 3-wire harness going

Table 7-2. Recommended Test Equipment for Troubleshooting

INSTRUMENT	REQUIRED CHARACTERISITCS	RECOMMENDED MANUFACTURER
Digital Multimeter	Dc Voltage: .05% to 30V .002% to 10V.	John Fluke Co. Model 8600A
Oscilloscope	60 MHz bandwidth, 1mV vertical sensitivity, and variable external horizontal input capability.	Tektronix Models 5440/ 5A18/5B10
Scalar Network Analyzer	Ability to display frequency response of sweep generator.	WILTRON Model 560A
RF Detector	Ability to detect signals within the 10 MHz to 26.5 GHz frequency range.	WILTRON Model 7S50, Option 2
Signature Analyzer	Ability to make signature analysis of microprocessor circuitry.	Hewlett-Packard Model 5004A
Directional Coupler	Ability to couple signals within a portion of the 10 MHz to 18 GHz frequency range.	NARDA Model 3202B-10
DC Power Supply	3 volts @ 3 amps	HP 6281
Dual DC Power Supply	1 supply = 0 to 7V 1 supply = +15V Common ground OK.	HP 6236B
DC Power Supply	30V - Isolated from ground and other voltage supplies.	HP 6216

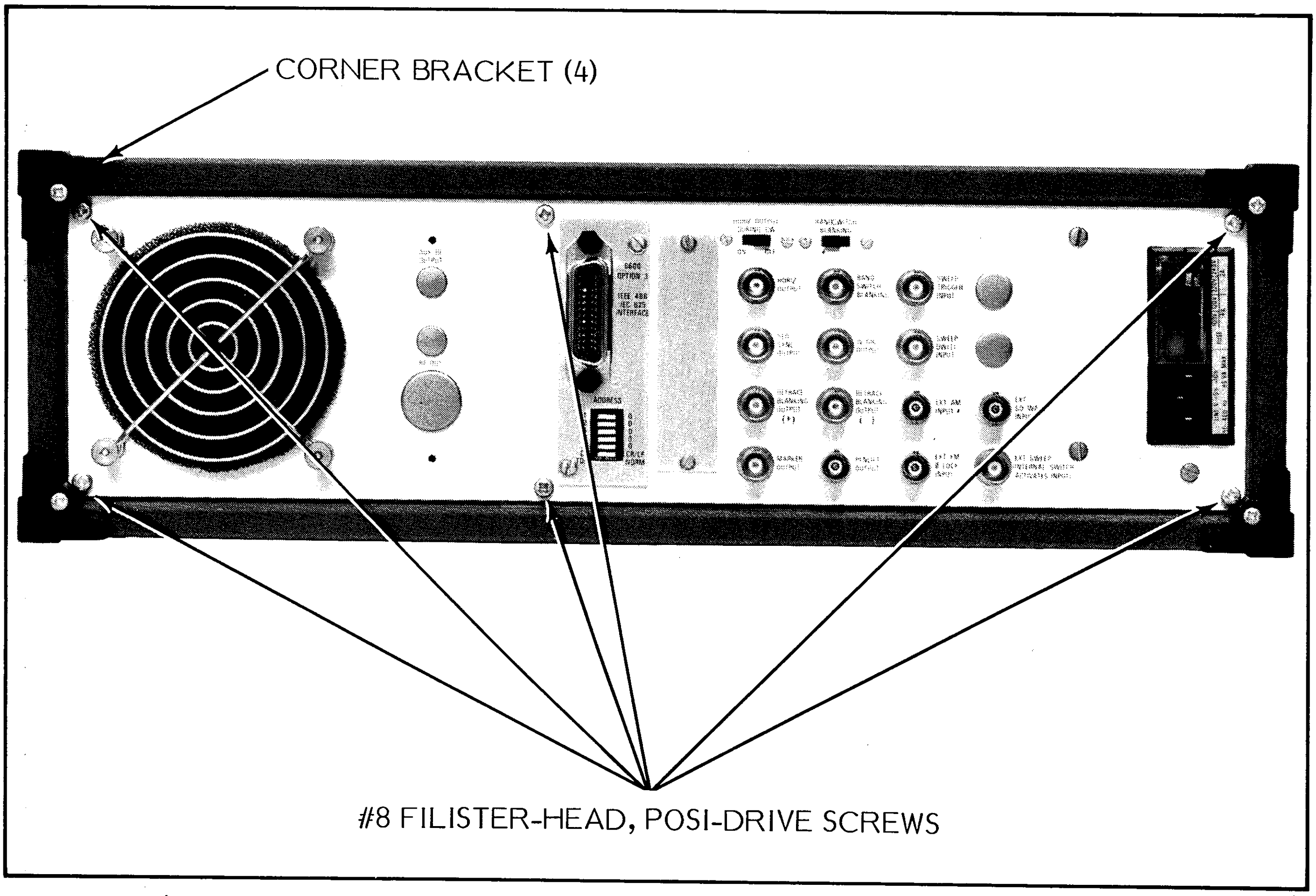


Figure 7-1. 6600A Series Programmable Sweep Generator, Rear Panel

to A12P8 is well clear of the bottom mid-panel screw that secures the front panel assembly to the basic frame.

7-3.2 Front Panel, Disassembly and Reassembly Instructions

a. Disassembly.

1. Remove the front panel assembly from the basic frame; refer to paragraph 7-3.1.

CAUTION

The INCREASE/DECREASE lever extends out approximately 1/4 inch beyond the surfaces of the front panel pushbuttons. Use care to prevent bending the lever shaft.

2. Disconnect the 5-wire connector from A12P4.

3. Disconnect the 3-wire connector from A12P8.

CAUTION

The A12 and A11 PCBs are interconnected using 4 in-line-pin connectors (Figure 7-4). When separating the two PCBs, use care to avoid bending connector pins.

4. Remove the six 1/2-inch 4-40 screws, flatwashers, and lockwashers from the A12 PCB; separate the A12 PCB from the A11 PCB.

5. Remove the knobs from the MANUAL SWEEP, MARKER AMPLITUDE, and EXTERNAL ALC GAIN

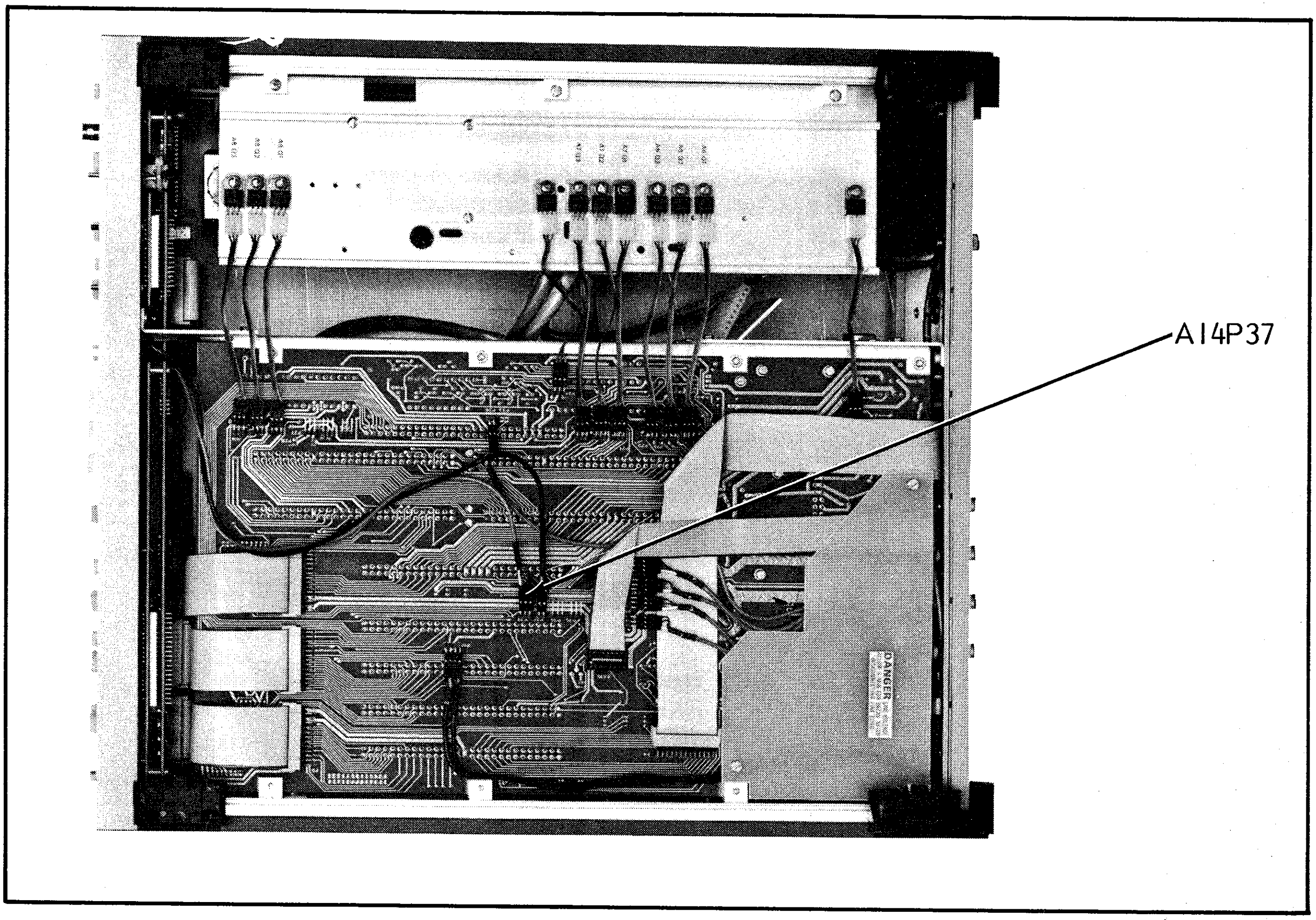


Figure 7-2. 6600A Series Programmable Sweep Generator, Bottom View

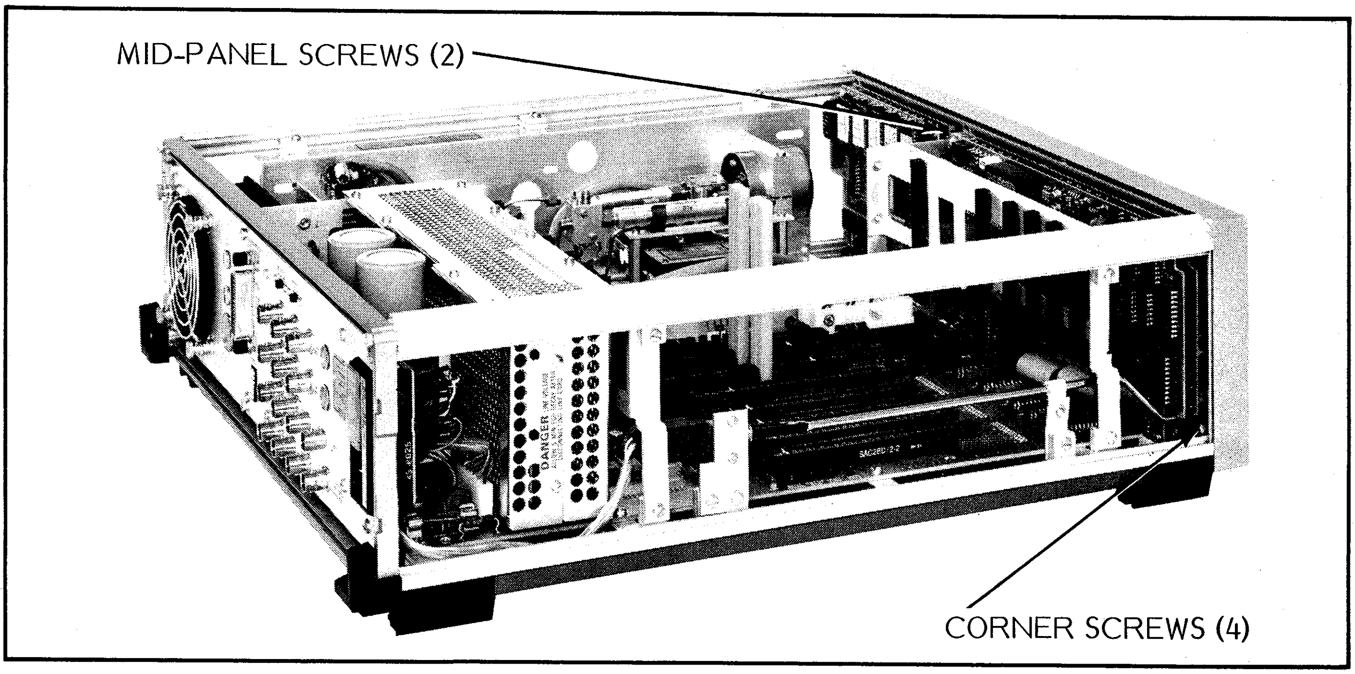


Figure 7-3. 6600A Series Programmable Sweep Generator, Side View

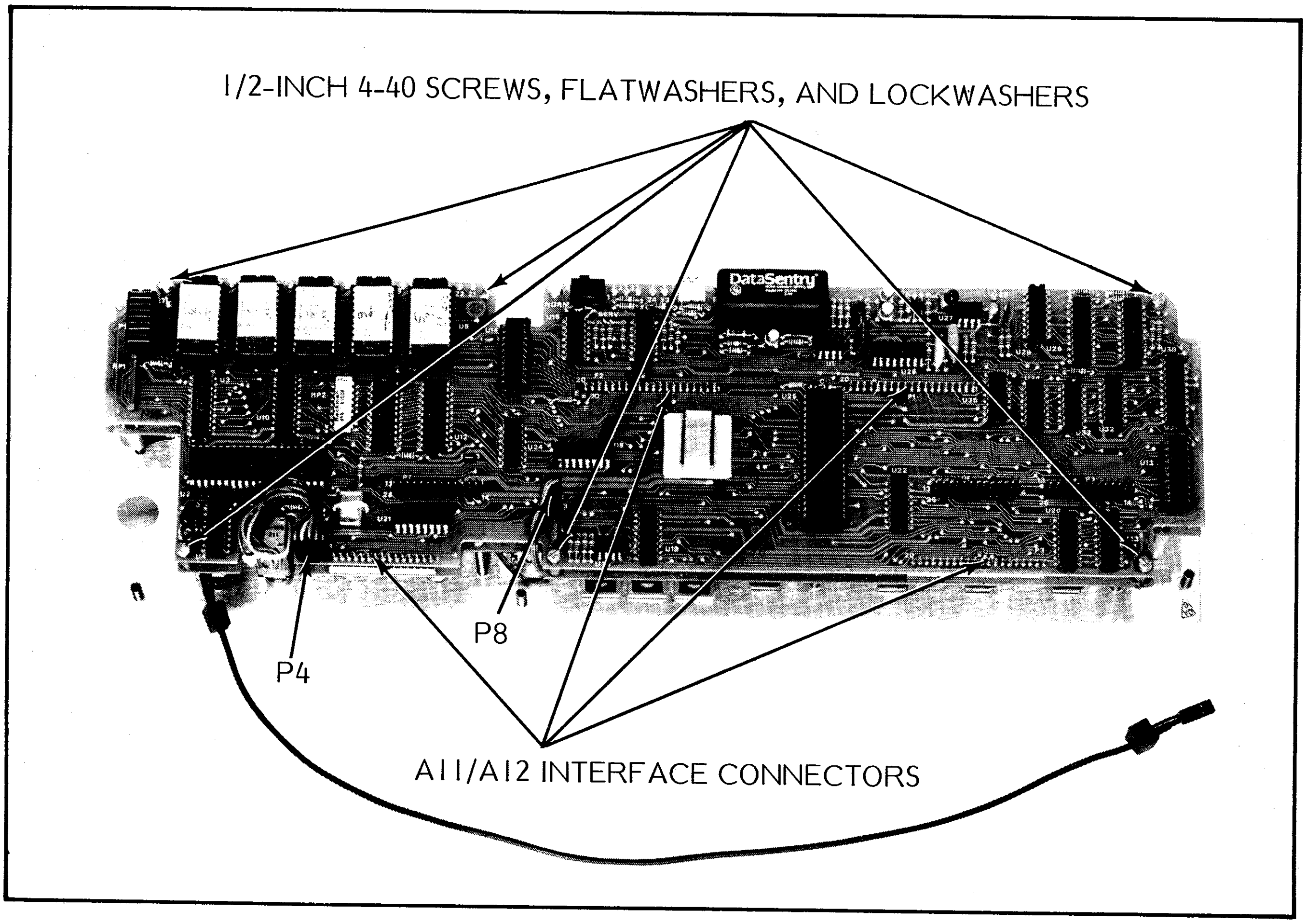


Figure 7-4. 6600A Series Programmable Sweep Generator, Front Panel Assembly

controls. To remove, pull knobs straight off.

6. Remove the eight 7/8-inch 4-40 screws, flatwashers, and lockwashers from the A11 PCB.

7. Separate the A11 PCB from the front panel.

b. Reassembly.

1. Mount the A11 PCB onto the front panel. Use care to insure that the LEDs and pushbuttons are properly aligned with their respective cutouts on the front panel.

2. Reinstall the eight 7/8-inch 4-40 screws, flatwashers, and lockwashers so that they are snug, but not tight, to the PCB.

3. Check each pushbutton, especially those on the keypad, and insure that none is binding. Reposition the A11 PCB slightly, if required, to prevent pushbutton binding.

4. Tighten the eight A11 retaining screws.

5. Reinstall the knobs on the MANUAL SWEEP, MARKER AMPLITUDE, and EXTERNAL ALC GAIN controls.

NOTE

The knob with the "shoulder" goes on the EXTERNAL ALC GAIN potentiometer.

6. Rejoin the A11 and A12 PCBs, as follows:

   (a) Position the A12 PCB so that the male pins on P3 and P4 mate with their respective female pins on A11J3 and A11J4. Insure that the pins of A12P1 and A12P2 are aligned with their mating pins on A11J1 and A11J2.

   (b) While observing the four connectors, gently press the two PCBs together until the connectors are properly seated.

   (c) Reinstall the six 1/2-inch 4-40 screws, flatwashers, and lockwashers.

7. Reconnect the 5-wire connector to A12P4 (green wire to pin 20); see Figure 7-4.

8. Reconnect the 3-wire connector to A12P8 (brown wire to pin 1); see Figure 7-4.

9. Reinstall the front panel assembly into the basic frame; refer to paragraph 7-3.1.

7-3.3 INCREASE/DECREASE Lever, Switch-Assembly Replacement

The INCREASE/DECREASE lever switch-assembly is not repairable in the field. In the event of an electrical or mechanical failure, the entire switch-assembly must be replaced. To replace this assembly, proceed as follows:

NOTE

The knob on the INCREASE/DECREASE lever is secured to the lever shaft with an epoxy compound. The removal of this knob may cause its destruction. Consequently, when ordering a replacement INCREASE/DECREASE lever switch-assembly, a replacement knob (WILTRON part number 430-106) should be ordered also.

a. Remove the front panel assembly from the basic frame; refer to paragraph 7-3.1.

b. Disassemble the front panel assembly; refer to paragraph 7-3.2.

c. Remove the knob from the INCREASE/DECREASE lever (see NOTE above).

d. Remove the two 1/4-inch 4-40 screws, flatwashers, and lockwashers, and remove the assembly from the front panel.

e. Install the new assembly and secure using the 4-40 hardware.

f. Install new knob on lever shaft, and secure it in place using a quick-drying cement (such as a 3-minute epoxy compound).

g. Reassemble the front panel assembly; refer to paragraph 7-3.2.

h. Reinstall the front panel assembly into basic frame; refer to paragraph 7-3.1.

7-3.4 Rear Panel Assembly, Removal and Reinstallation Instructions

a. Removal.

   1. Turn off ac power and disconnect the input line voltage.

   2. Remove the top and side covers from the sweep generator as follows:

      (a) Remove the 4 corner-brackets from the rear panel of the sweep generator, Figure 7-1.

      (b) Slide the top and side covers to the rear and remove.

WARNING

There are dangerous charged-capacitor voltages present on P1 pins 3 thru 10 when power is removed. Discharge these pins to chassis ground before performing maintenance.

3. Disconnect the Molex connector from A14P1 (Figure 7-5).

4. Remove the six #8 fillister-head, posi-drive screws from the rear panel (Figure 7-1).

5. Gently push the rear panel out from the basic frame and lay it back on the work surface. It is not necessary to remove the rear panel assembly completely; all rear panel components are accessible with the panel in this position.

b. Reinstallation. The reinstallation procedure for the rear panel assembly is a reversal of the removal procedure.

7-3.5 A13 Switching Power Supply PCB, Removal and Reinstallation

WARNING

Voltages hazardous to life are present through the A13/A14 Switching Power Supply, even when power is turned off and the ac line cord is removed. Before performing maintenance on this power supply, observe the following precautions:

After ac power is turned off and the line cord is removed,

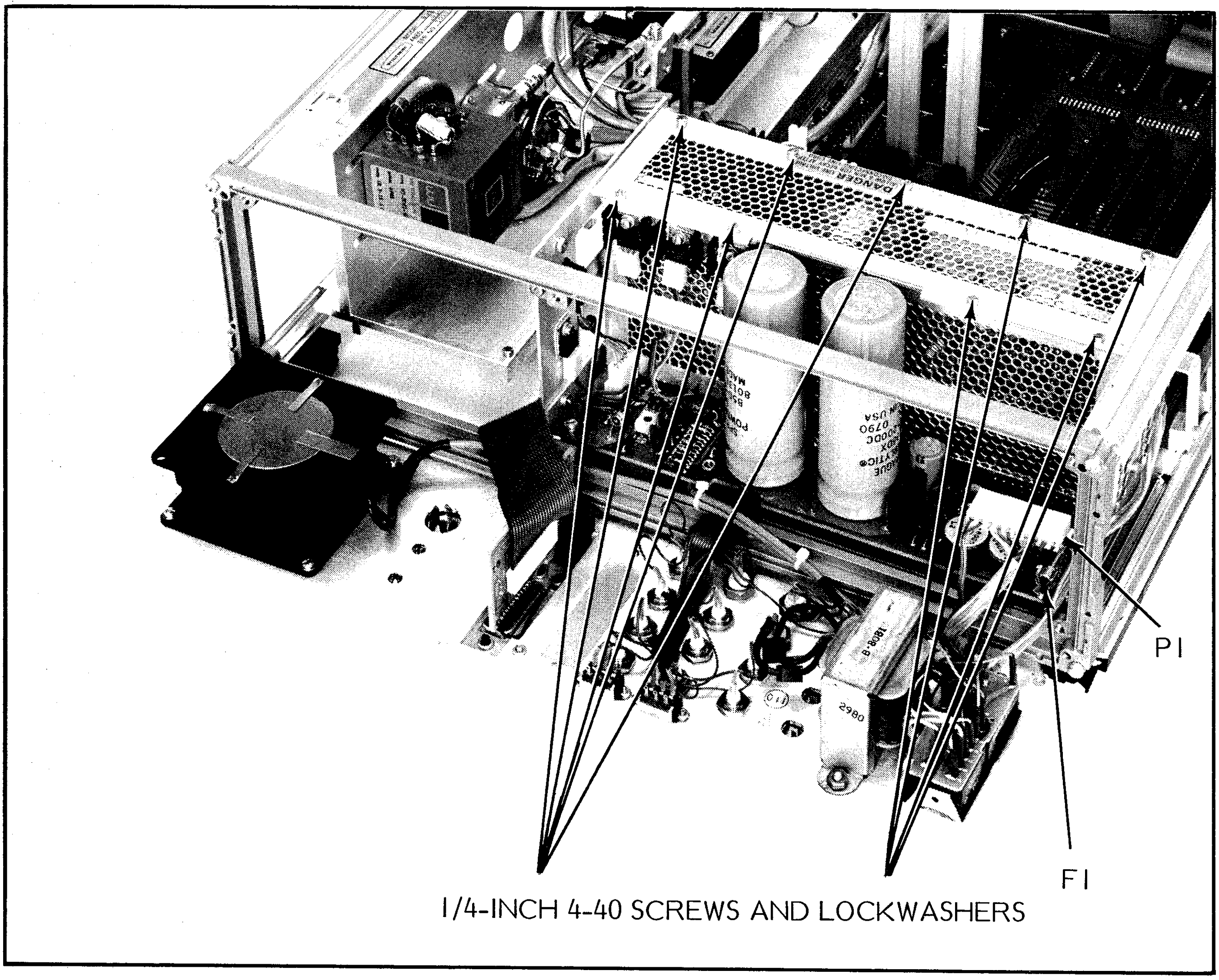


Figure 7-5. 6600A Series Programmable Sweep Generator, Rear Quarter Panels and Assemblies

allow 5 minutes for the capacitor voltages to decay.

Avoid touching the terminals on the 5A FB fuse, A14F1, (Figure 7-5) when power is turned on. +165 Vdc is present on these terminals.

a. Removal.

1. Turn off the ac power and disconnect the ac line cord from the Voltage Selector Module.

2. Remove the top cover from the sweep generator, as follows:

   (a) Remove the two top, corner brackets from the rear panel of the sweep generator (Figure 7-1).

   (b) Slide the cover to the rear and remove.

3. Remove the ten 1/4-inch 4-40 screws and lockwashers from the top cover of the A13 card-cage assembly, and remove the cover.

4. Using the ejectors on the ends of the PCB, eject the PCB from the XA13 socket.

b. Reinstallation. The reinstallation instructions are a reversal of the removal instructions.

NOTE

The A13 PCB power supply switching-frequency is in the RF spectrum (50 kHz). To prevent this RF energy from being radiated, insure that the card-cage cover is securely seated and fastened with all ten screws before the ac power is reapplied.

7-4 6600A SERIES PROGRAMMABLE SWEEP GENERATOR, OVERALL CIRCUIT DESCRIPTION

The 6600A Series Programmable Sweep Generator is a microprocessor-controlled, broadband sweeper that uses drop-in (rather than plug-in) radio- and microwave-frequency components. Like most other sweepers, the 6600A is organized into "mainframe" circuits that are universal for all models and frequency components that are model-dependent. For descriptive purposes, the model-dependent circuits are subdivided into five classes: Models 6609A/6617A, Models 6621A/ 6621A-40/ 6629A/ 6629A-40, Models 6637A/ 6637A-40/ 6638A/ 6647A/ 6648A, Models 6653A/6659A, and Model 6642A. Overall block diagrams for the 6609A/6617A, 6637A/6637A-40/6638A/6647A/6648A, and 6653A/6659A are provided in Figures 7-7 thru 7-9 respectively.

a. Universal Circuits. The 6600A series universal circuits consist of the following printed circuit boards (PCBs): A12 Microprocessor, A11 Front Panel, A1 GPIB Interface (Option 3), A2 Ramp Generator, A3 Marker Generator, A4 Automatic Level Control (ALC), A5 Frequency Instruction, and A10 FM/Attenuator.

The A12 Microprocessor PCB provides overall control for RF signal generation. As shown in Figure 7-7, the A12 PCB interfaces with the Analog Circuits via the **µP Bus**, and with the front panel controls via the A11 PCB. The A12 PCB is described in paragraph 7-6.1.

The A11 Front Panel PCB provides an interface for all of the front panel pushbuttons except RESET and SELF TEST. These two pushbuttons are connected directly to the A12, where their activation causes microprocessor interrupt routines to be generated. The A11 PCB is described in paragraph 7-7.1.

The A1 GPIB Interface PCB is only installed for sweep generators containing Option 3. This PCB provides interface between the IEEE-488 Interface Bus (General Purpose Interface Bus--GPIB) and the sweep generator. The A1 PCB is described in paragraph 7-8.1.

The A2 Ramp Generator PCB is the sweep-generation source when either the

TRIGGER-AUTO, -LINE, or -EXT OR SINGLE pushbutton is used to select the triggering mode. These three pushbuttons control the A2 sweep ramp via the **µP BUS.** Triggering for the A2 sweep ramp is accomplished via the **µP Bus** for the single sweep mode, via the **EXT TRIGGER IN** line for the external sweep mode, or via the **AC LINE VOLTAGE** input for the line trigger mode. The remaining two input lines, **INTENSITY MARKER** and **EOB,** cause the A2 sweep ramp to dwell momentarily. The **INTENSITY MARKER** line causes the ramp to dwell when an intensity marker is commanded. And the **EOB** line causes the ramp to dwell during an oscillator bandswitch (see NOTE). The A2 PCB output lines include the **RAMP OUT** signal that goes to the A5 PCB and the five signals that go to the rear panel connectors: **BANDSWITCH BLANKING (+), (-); RETRACE BLANKING (+), (-);** and **SEQ SYNC.** The A2 PCB is described in paragraph 7-9.1.

NOTE

As shown in Figure 7-8, three YIG oscillators are used to generate a full-band sweep with the Models 6637A/38A/47A/48A. The frequency at which the sweep (or CW tuning) goes from a lower- to a higher-frequency oscillator (or from the heterodyne band to the first oscillator band) is known as the bandswitch point.

The A3 Marker Generator PCB generates the F0, M1, and M2 markers. The marker frequency and mode (VIDEO, RF, INTENSITY) data enters A3 via the **µP BUS.** The frequency data is converted to an analog voltage, compared with the **RAMP, 0-10V,** signal, and used to generate the frequency marker. The mode data selects the type of marker to be displayed: either intensity, RF, or video. The **RAMP, 0-10V,** signal is also buffered on A3 and supplied to the rear panel HORIZ OUTPUT connector. The A3 PCB, in addition to generating markers, also contains the logic circuitry associated with the front panel INCREASE/DECREASE lever. The **MODIFY SIGNAL** line provides the input to this logic circuitry. The frequency data generated by this logic circuitry is in the form of an 8-bit digital word. This word is sent to the microprocessor via the **µP Bus.** The A3 PCB is described in paragraph 7-10.1.

The A4 Automatic Level Control PCB is the control arm for the RF-output-signal leveling loop. The input arm for the leveling loop is either the built-in Coupler/Detector that is used for internal leveling, or it is the external coupler and detector (or power meter) that is required for external leveling. The output arm of the leveling loop is the PIN switch attenuator current-driver circuit (not shown) located on the A6-A9 YIG Driver PCBs. These current-driver circuits operate the **MOD DRIVER 1, 2, 3,** and **4** lines used to control Mod and PIN switch attenuation. The A4 also performs the following functions:

1. It sets the magnitude of the RF output power, which the user selects using the front panel LEVEL pushbutton.
2. It creates a "dip" in output power at the RF marker frequency.
3. It provides the RF SLOPE correction to the output power signal.

The A4 PCB, in addition to controlling the leveling loop, provides a latch for the **ATTN 1** through **ATTN 4** control bits. These control bits come from the microprocessor and go to the A10 PCB. The A4 PCB is described in paragraph 7-11.1.

The A5 Frequency Instruction PCB generates tuning and bandswitch-control voltages for the A6-A9 YIG Driver PCBs. The bandswitch-control voltage is the **FCEN/VPF** signal, and the tuning voltages are the **F CEN, ΔF>50 MHz,** and **F CORR** signals. There are three sweep-voltage-producing sources in the sweep generator: The A2 PCB, the front panel MANUAL SWEEP potentiometer, and the Step Frequency DAC (digital-to-analog converter, paragraph 3-7.2), located on A5. One of these sources, as determined by the microprocessor, is selected on A5 and used to generate the **ΔF >50 MHz** signal. The center frequency, which the user selects using the front panel FREQUENCY RANGE controls, provides the **F CEN** signal. And a correction voltage, which is the sum of the FREQUENCY VERNIER signal from the front panel and the Linearizing ROM signal (see NOTE) from the applicable A6-A9 YIG Driver PCB, provides the **F CORR** signal. The FREQUENCY VERNIER signal enters A5 via the **µP Bus**, and the linearizing ROM signal enters via the **FC** (frequency correction) **Bus**. The A5 PCB also supplies a tuning signal, **ΔF≤50 MHz**, for the FM coil in the YIG oscillator; this signal goes to the A10 PCB. The **ΔF≤50 MHz** signal sweeps the YIG oscillator via the FM coil when the sweep width is ≤50 MHz. The A5 PCB is described in paragraph 7-12.1.

NOTE

Many YIG oscillators, though inherently linear, often have linearity errors due to magnetic saturation effects. To correct for linearity errors, digital data providing up to ±64 MHz of frequency correction may be stored in read-only memory (ROM). If required by the installed YIG oscillator, a Linearizing ROM is mounted on the applicable A6, A7, A8, or A9 YIG Driver PCB.

The A10 FM/Attenuator PCB provides a tuning current for the YIG Osc 1-4 FM (frequency modulation) coils and the Osc 1 YIG tracking filter. The tracking filter tuning current is derived from the **TRACK FILTER 1** voltage generated on the A6 PCB. The FM coil tuning current may be derived from either of two sources: an external FM signal from the rear panel via the EXT FM ØLOCK INPUT connector or a sweep width voltage from the A5 PCB via the **ΔF≤50 MHz** signal line. In addition to the FM and tracking filter currents, the A10 generates an end-of-band pulse (**EOB**) whenever a bandswitch occurs. The **HET YIG SEL** and **YIG 1, 2, 3** and **4 SEL** lines from the A6-A8 PCBs provide the input for the **EOB** circuit. The A10 PCB is described in paragraph 7-13.1.

The A14 Motherboard PCB provides an interconnecting plane for the A1 through A10 PCBs. It also provides interconnection via connectors between the A1-A10 PCBs and the A12 PCB, the rear panel connectors, and the RF Deck components. The A14 PCB also contains diagnostic (self-test) and PIN Switch port drive and attenuator circuitry; it also contains part of the switching power supply circuitry. The A14 PCB is described in paragraph 7-15.2.

The A13 Switching Power Supply PCB, in conjunction with the power supply circuits on the A14 PCB, provides power supply voltages for the sweep generator circuits. The A13/A14 Switching Power Supply is described in paragraph 7-15.1.

The A18 GPIB Interface Connector PCB provides a connecting plane for the Option 3 rear panel GPIB connector and address switches. This PCB is installed only on sweep generators containing Option 3. The A18 PCB is described in paragraph 7-16.

b. Models 6609A/6617A. The model-dependent circuits and components for the 6609A and 6617A consist of the A6 Het/YIG Driver PCB and the components shown on the RF Deck.

The A6 Het/YIG Driver PCB provides tuning and bias currents for the YIG tuning coil. The tuning current is derived from the three tuning voltages (**F CEN, ΔF >50 MHz, F CORR**) supplied by the A5 PCB. The oscillator bias current is generated on the A6 PCB. In addition to tuning and bias currents, the A6 PCB also generates a tracking filter voltage, which is supplied to the A10 PCB. This voltage indirectly provides tuning for the YIG tracking filter that is built into the 6617A

YIG module. The other A6 output is the **HET YIG SEL** line that is supplied to the A10 PCB (6617A). The A6 PCB is described in paragraph 7-12.3.

The RF Deck is a subassembly; it contains all of the sweep generator RF components. This subassembly is described in paragraph 7-14.

c. Models 6621A/6621A-40/6629A/6629A-40. The model-dependent circuits and components for these four models are as follows (Figure 7-8):

1. The 6621A and 6621A-40 consist of the A6 Het/YIG Driver PCB, A7 YIG Driver PCB, YIG OSC 1, YIG OSC 2, PIN Switch, and Coupler/Detector.
2. The 6629A and 6629A-40 consist of the A7 and A8 YIG Driver PCBs, YIG OSC 2, YIG OSC 3, PIN Switch, and Coupler Detector.

The circuit description for the model-dependent circuits is the same as that for the 6637A/6638A/6647A/6648A circuits in subparagraph d. below.

d. Models 6637A/6637A-40/6638A/6647A/6648A. The model-dependent circuits and components for these five models consist of the A6, A7, and A8 YIG Driver PCBs, and the components shown on the RF Deck (Figure 7-8).

The A6 Het/YIG Driver and the A7 and A8 YIG Driver PCBs provide tuning and bias currents for the Osc 1, 2, and 3 YIG tuning coils. The tuning currents are derived from the three tuning voltages (**F CEN, ΔF >50 MHz, F CORR**) supplied by the A5 PCB. The oscillator bias currents are generated individually on each A6-A8 PCB. In addition to tuning and bias currents, the A6 PCB also generates a tracking filter voltage, which is supplied to the A10 PCB. This voltage indirectly provides tuning for the YIG tracking filter that is built into the Osc 1 YIG module. With the exception of the MOD DRIVER signals previously described, the other A6-A8 outputs are control lines. The **SNB** and **SNR** lines are select-next-band and select-next-ROM lines, respectively. When the presently selected oscillator band has reached its upper-most frequency, the **SNB** line selects the next oscillator band and the **SNR** line enables this next oscillator band's linearizing ROM. The **HET YIG SEL** and **YIG 1, 2,** and **3 SEL** lines are supplied to the A10 PCB. A detailed overall description of the A6-A8 PCBs is given in paragraph 7-12.2. The A6 PCB is described in paragraph 7-12.3, and the A7 and A8 PCBs are described in paragraph 7-12.4.

The RF Deck is a subassembly; it contains all of the sweep generator RF components. This subassembly is described in paragraph 7-14.

e. Models 6653A/6659A. The model-dependent components for the 6653A and 6659A consist of the A6-A9 YIG Driver PCBs and the components shown on the RF Deck (Figure 7-9).

The A6 Het-YIG Driver and A7, A8, and A9 YIG Driver PCBs provide tuning and bias currents for the Osc 1, 2, 3 and 4 YIG tuning coils. The tuning currents are derived from the three tuning voltages (**F CEN, ΔF >50 MHz, F CORR**) supplied by the A5 PCB. The oscillator bias currents are generated individually on the A6-A9 PCBs. In addition to tuning and bias currents, the A6 PCB also generates a tracking filter voltage, which is supplied to the A10 PCB. This voltage indirectly provides tuning for the YIG tracking filter that is built into the Osc 1 YIG module. With the exception of the Mod Driver signals previously described, the other A6-A9 outputs are control lines. The **SNB** and **SNR** lines are select-next-band and select-next-ROM lines, respectively. When the presently-selected oscillator has reached its upper-most frequency, the **SNB** line selects the next oscillator band and the **SNR** line enables this next oscillator band's linearizing ROM. The **HET YIG SEL** and **YIG 1, 2, 3,** and **4 FM COIL SEL** lines are supplied to the A10 PCB. An overall description of the A6-A9 PCBs is given in paragraph 7-12.2. The A6 PCB is described in paragraph 7-12.3 and the A7-A9 PCBs are described in paragraph 7-12.4.

The RF Deck is a subassembly; it contains all of the sweep generator RF components. This subassembly is described in paragraph 7-14.

f. Model 6642A. The model-dependent circuits and components for the 6642A consist of the A6 and A7 PCBs and the RF Deck components, as shown in Figure 7-6.

The A6 and A7 YIG Driver PCBs provide tuning and bias currents for the Osc 1 and 2 YIG tuning coils. The tuning currents are derived from the three tuning voltages (**F CEN, ΔF >50 MHz, F CORR**) supplied by the A5 PCB. The oscillator bias currents are generated individually on the A6 and A7 PCBs. With the exception of the MOD DRIVER signals previously described, the other A6 and A7 outputs are control lines. The **SNB** and **SNR** lines are select-next-band and select-next-ROM lines, respectively. When the presently-selected oscillator band has reached its upper-most frequency, the **SNB** line selects the next oscillator band and the **SNR** line enables this next oscillator band's linearizing ROM. The **YIG 1, 2, 3,** and **4 SEL** lines are supplied to the A10 PCB. An overall description of the A6/A7 PCBs is given in paragraph 7-12.2. The A6 PCB is described in paragraph 7-12.3 and the A7 PCB is described in paragraph 7-12.4.

The RF Deck is a subassembly; it contains all of the sweep generator RF components. This subassembly is described in paragraph 7-14.

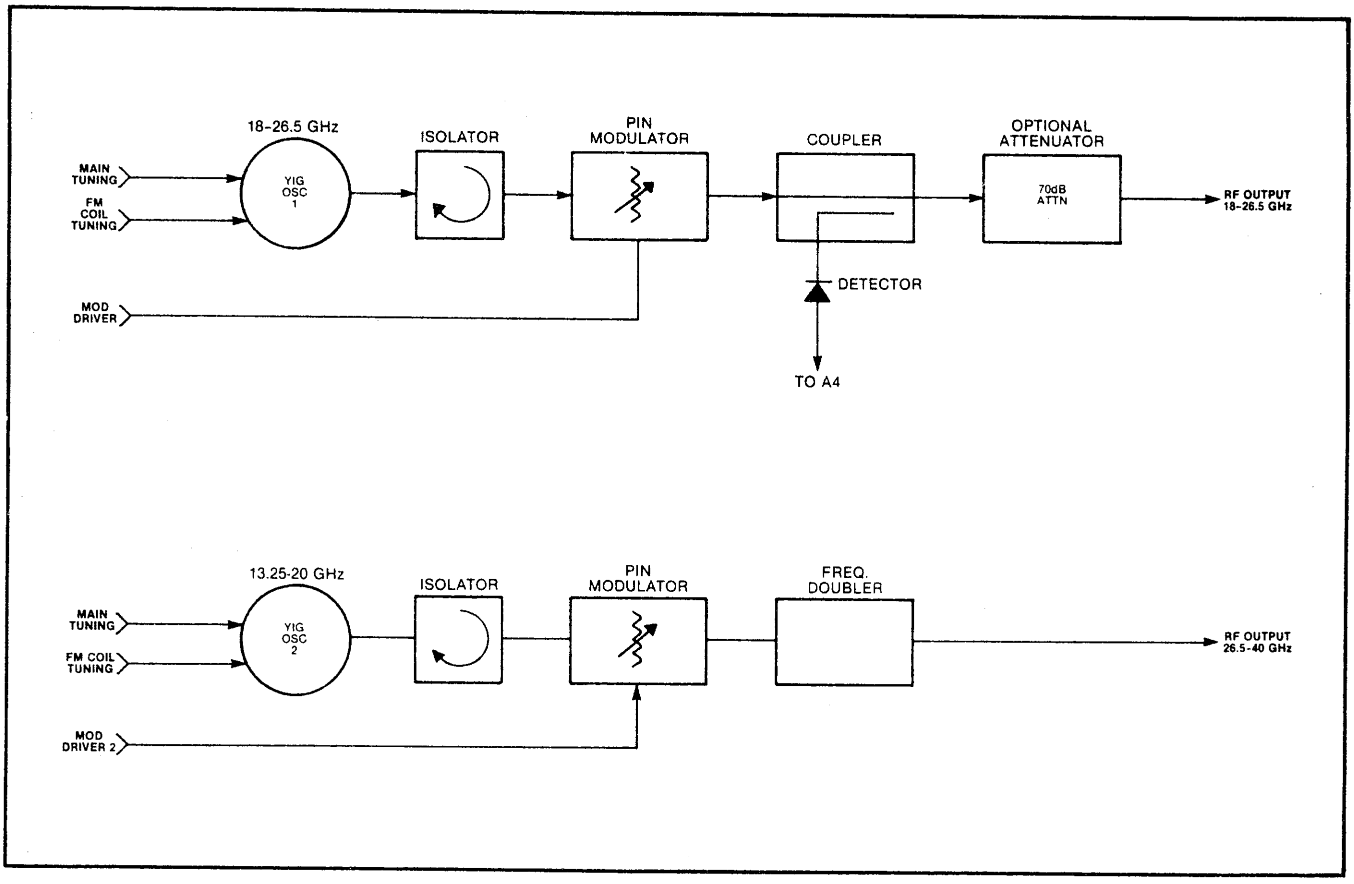
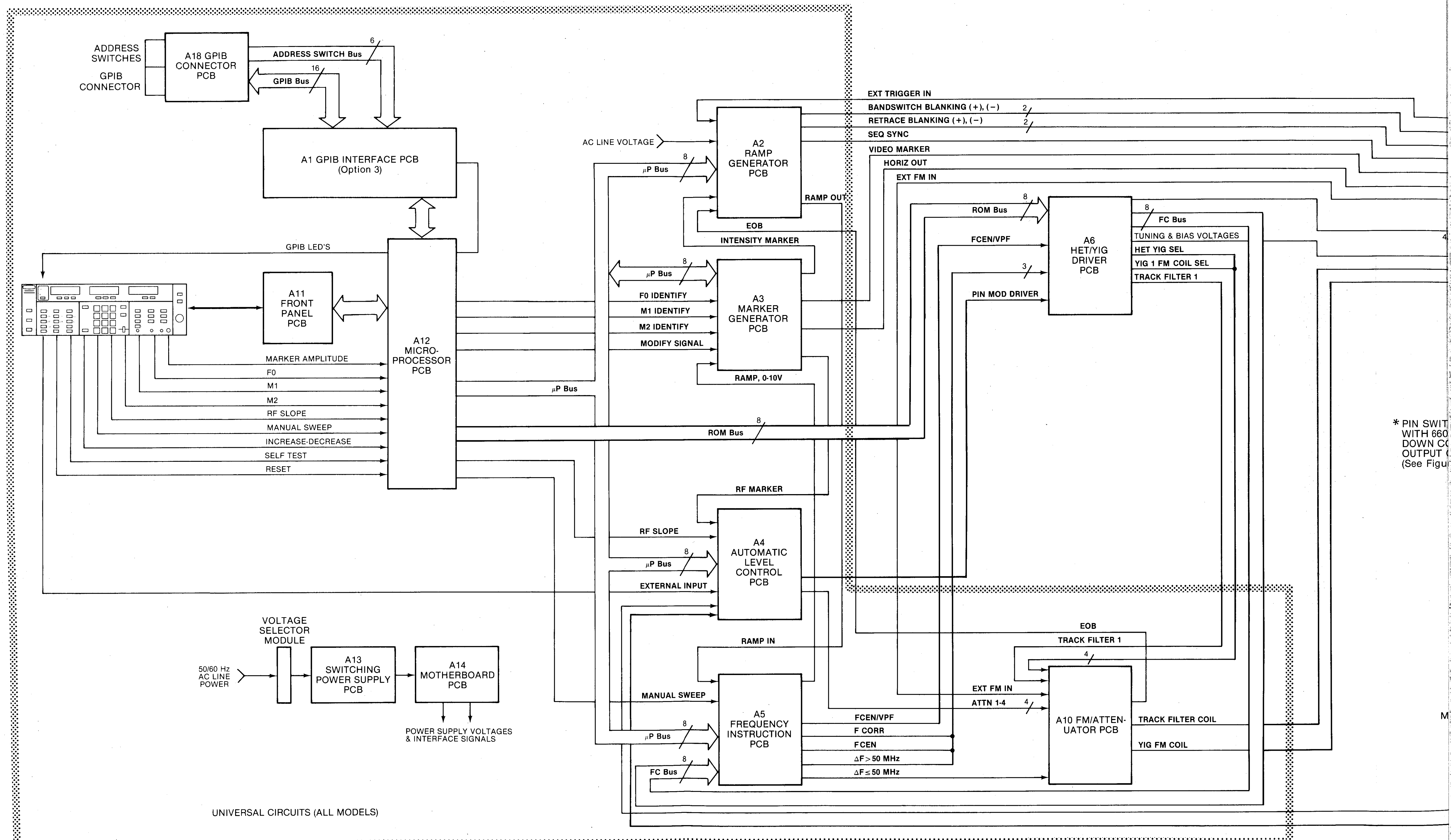


Figure 7-6. Model 6642A RF Components Deck


ADDRESS SWITCHES
GPIB CONNECTOR
A18 GPIB CONNECTOR PCB
ADDRESS SWITCH Bus
GPIB Bus
A1 GPIB INTERFACE PCB (Option 3)
GPIB LED'S
A11 FRONT PANEL PCB
A12 MICRO-PROCESSOR PCB
MARKER AMPLITUDE
F0
M1
M2
RF SLOPE
MANUAL SWEEP
INCREASE-DECREASE
SELF TEST
RESET
AC LINE VOLTAGE
μP Bus
A2 RAMP GENERATOR PCB
RAMP OUT
EOB
INTENSITY MARKER
A3 MARKER GENERATOR PCB
F0 IDENTIFY
M1 IDENTIFY
M2 IDENTIFY
MODIFY SIGNAL
RAMP, 0-10V
ROM Bus
RF MARKER
A4 AUTOMATIC LEVEL CONTROL PCB
RF SLOPE
EXTERNAL INPUT
RAMP IN
A5 FREQUENCY INSTRUCTION PCB
MANUAL SWEEP
FC Bus
FCEN/VPF
F CORR
FCEN
ΔF>50 MHz
ΔF≤50 MHz
EXT TRIGGER IN
BANDSWITCH BLANKING (+), (−)
RETRACE BLANKING (+), (−)
SEQ SYNC
VIDEO MARKER
HORIZ OUT
EXT FM IN
A6 HET/YIG DRIVER PCB
PIN MOD DRIVER
FC Bus
TUNING & BIAS VOLTAGES
HET YIG SEL
YIG 1 FM COIL SEL
TRACK FILTER 1
A10 FM/ATTEN-UATOR PCB
TRACK FILTER 1
ATTN 1-4
TRACK FILTER COIL
YIG FM COIL
VOLTAGE SELECTOR MODULE
50/60 Hz AC LINE POWER
A13 SWITCHING POWER SUPPLY PCB
A14 MOTHERBOARD PCB
POWER SUPPLY VOLTAGES & INTERFACE SIGNALS
UNIVERSAL CIRCUITS (ALL MODELS)
* PIN SWIT
WITH 660
DOWN C
OUTPUT
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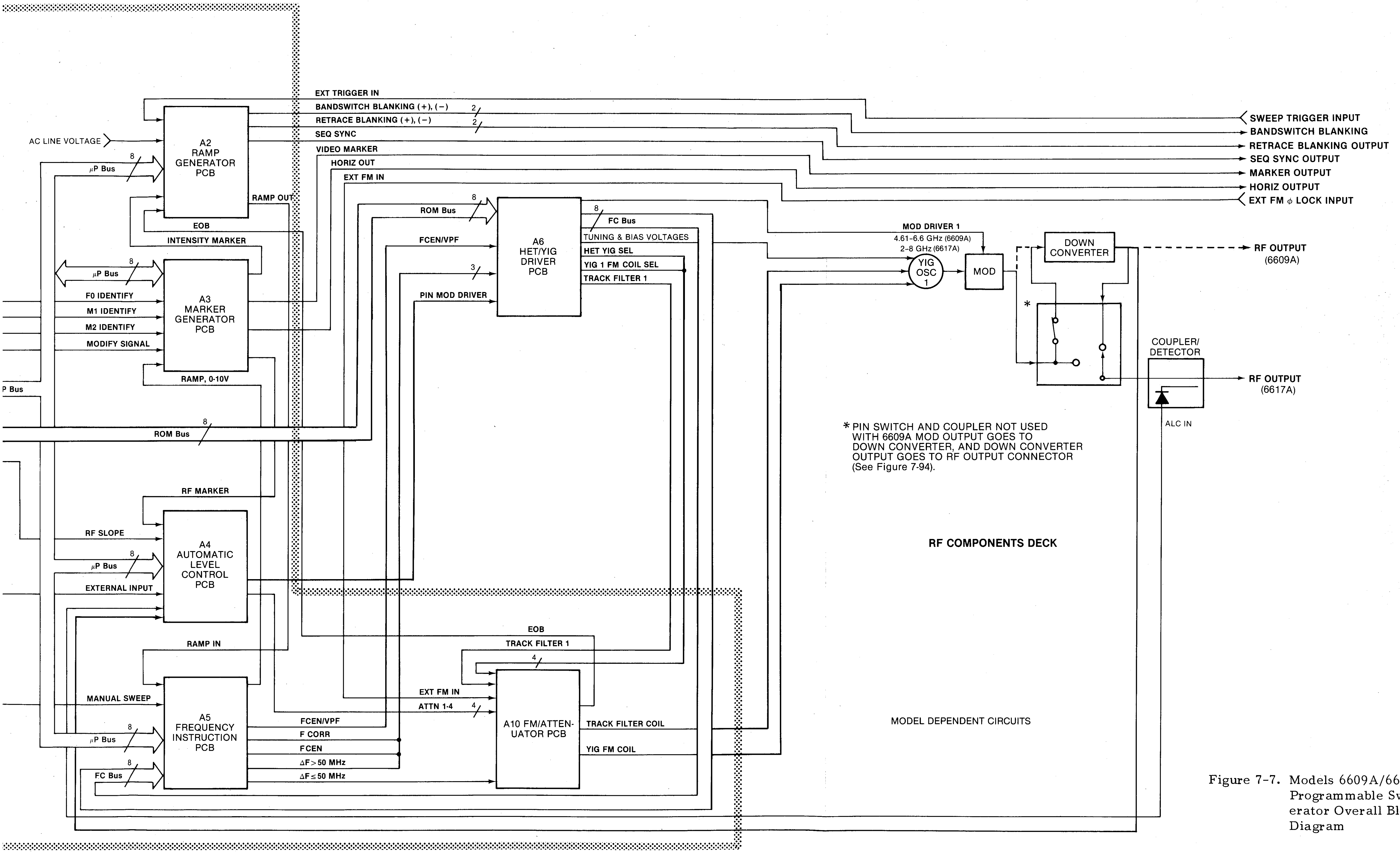
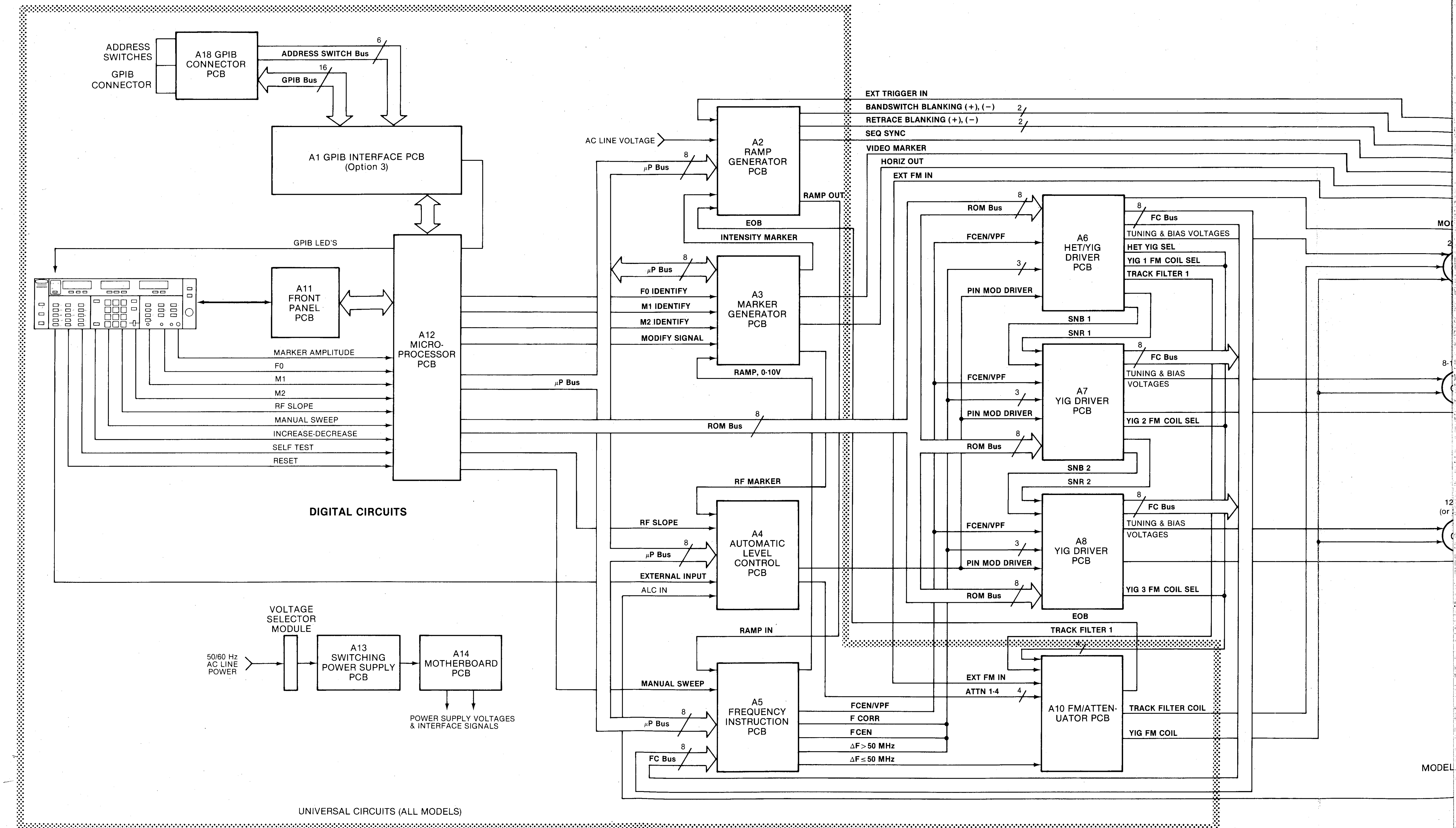


Figure 7-7. Models 6609A/6617A Programmable Sweep Generator Overall Block Diagram



ADDRESS SWITCHES
GPIB CONNECTOR
A18 GPIB CONNECTOR PCB
ADDRESS SWITCH Bus
GPIB Bus
A1 GPIB INTERFACE PCB (Option 3)
GPIB LED'S
A11 FRONT PANEL PCB
A12 MICRO-PROCESSOR PCB
MARKER AMPLITUDE
F0
M1
M2
RF SLOPE
MANUAL SWEEP
INCREASE-DECREASE
SELF TEST
RESET
DIGITAL CIRCUITS
VOLTAGE SELECTOR MODULE
50/60 Hz AC LINE POWER
A13 SWITCHING POWER SUPPLY PCB
A14 MOTHERBOARD PCB
POWER SUPPLY VOLTAGES & INTERFACE SIGNALS
UNIVERSAL CIRCUITS (ALL MODELS)
AC LINE VOLTAGE
μP Bus
A2 RAMP GENERATOR PCB
RAMP OUT
EOB
INTENSITY MARKER
A3 MARKER GENERATOR PCB
F0 IDENTIFY
M1 IDENTIFY
M2 IDENTIFY
MODIFY SIGNAL
RAMP, 0-10V
ROM Bus
RF MARKER
RF SLOPE
A4 AUTOMATIC LEVEL CONTROL PCB
EXTERNAL INPUT
ALC IN
RAMP IN
MANUAL SWEEP
A5 FREQUENCY INSTRUCTION PCB
FC Bus
FCEN/VPF
F CORR
FCEN
ΔF > 50 MHz
ΔF ≤ 50 MHz
EXT TRIGGER IN
BANDSWITCH BLANKING (+), (−)
RETRACE BLANKING (+), (−)
SEQ SYNC
VIDEO MARKER
HORIZ OUT
EXT FM IN
A6 HET/YIG DRIVER PCB
PIN MOD DRIVER
TUNING & BIAS VOLTAGES
HET YIG SEL
YIG 1 FM COIL SEL
TRACK FILTER 1
SNB 1
SNR 1
A7 YIG DRIVER PCB
YIG 2 FM COIL SEL
SNB 2
SNR 2
A8 YIG DRIVER PCB
YIG 3 FM COIL SEL
TRACK FILTER 1
A10 FM/ATTEN-UATOR PCB
ATTN 1-4
TRACK FILTER COIL
YIG FM COIL
MODEL

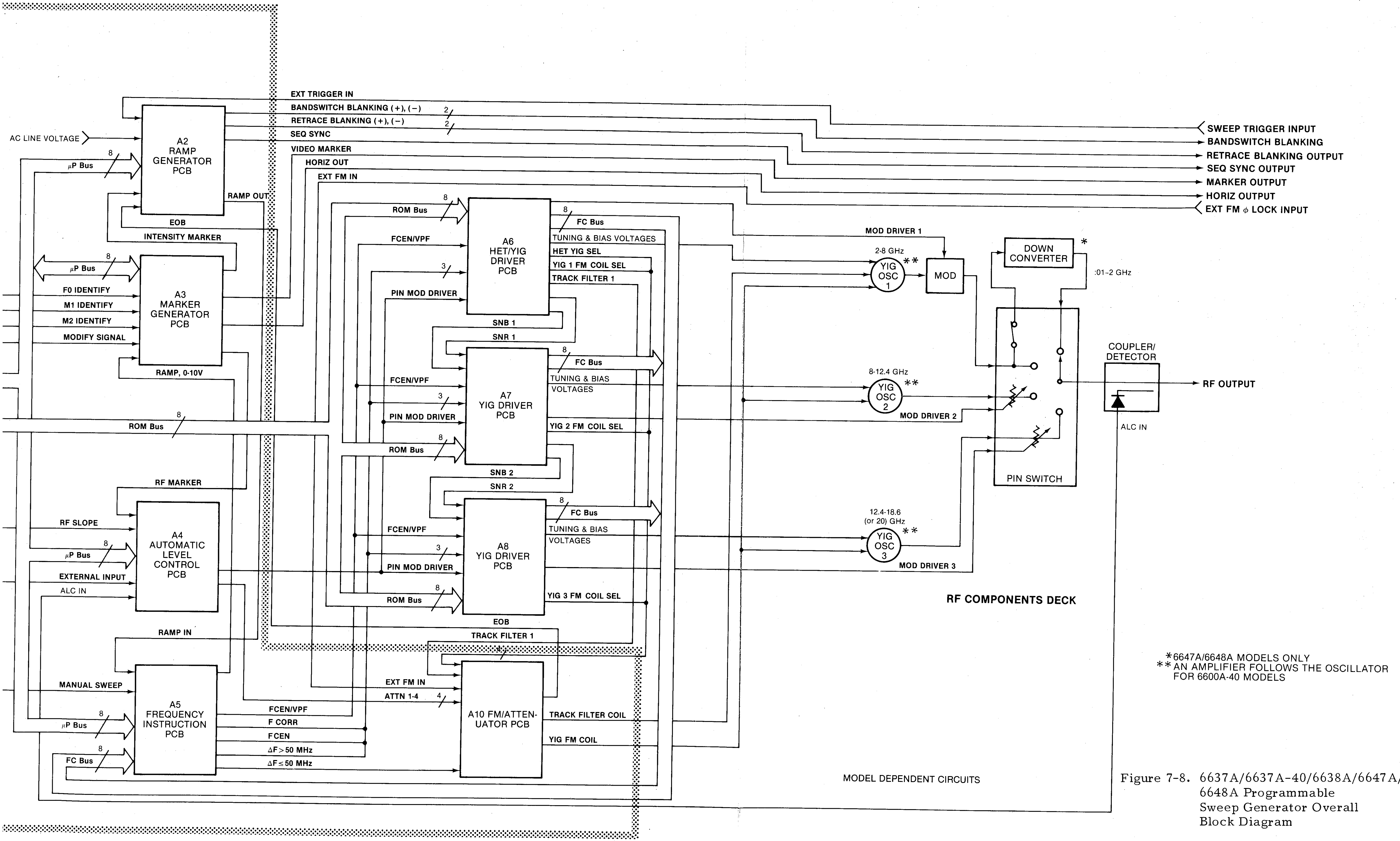
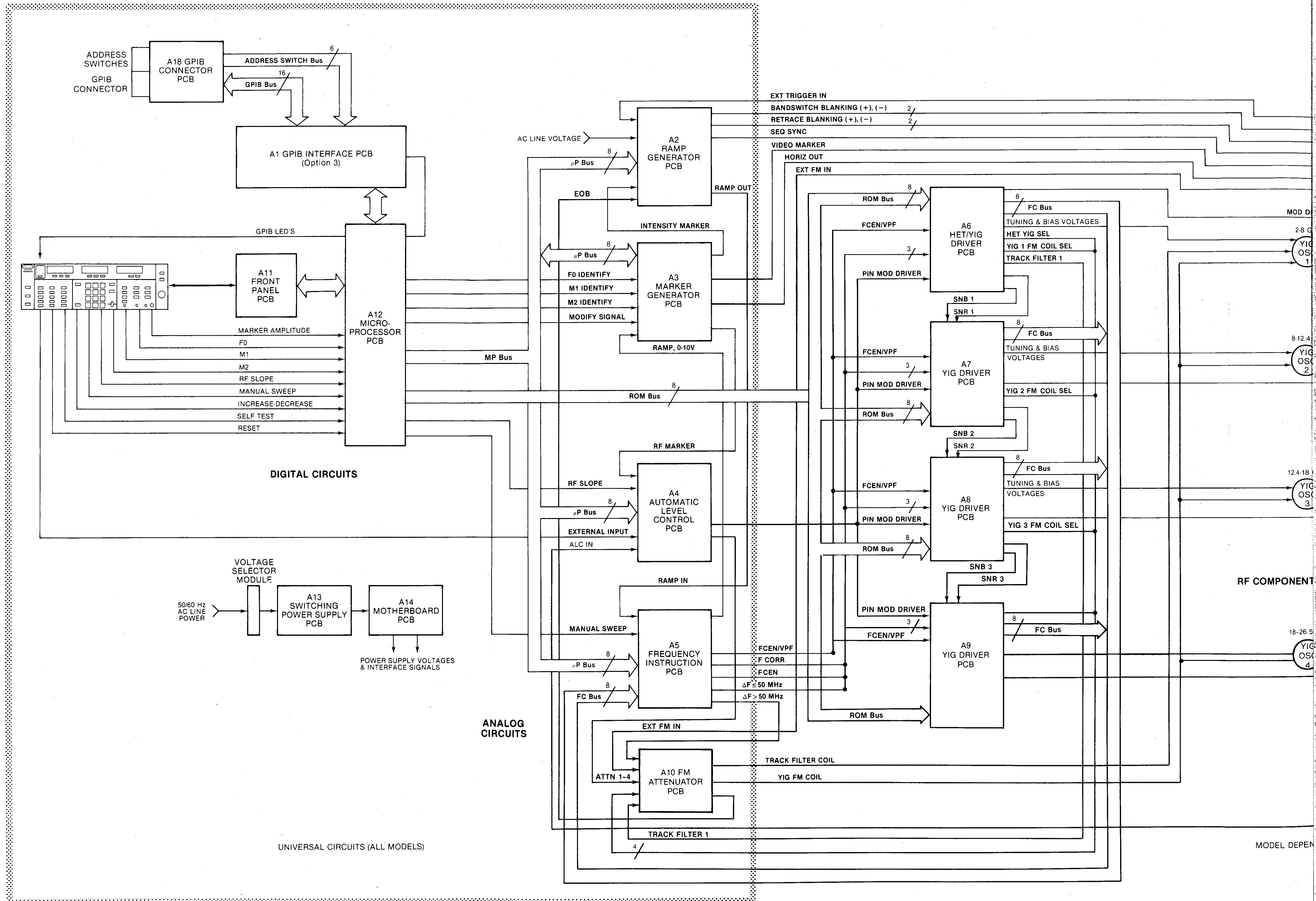


Figure 7-8. 6637A/6637A-40/6638A/6647A/6648A Programmable Sweep Generator Overall Block Diagram


ADDRESS SWITCHES
GPIB CONNECTOR
A18 GPIB CONNECTOR PCB
ADDRESS SWITCH Bus
GPIB Bus
A1 GPIB INTERFACE PCB (Option 3)
GPIB LED'S
A11 FRONT PANEL PCB
A12 MICRO-PROCESSOR PCB
MARKER AMPLITUDE
F0
M1
M2
RF SLOPE
MANUAL SWEEP
INCREASE-DECREASE
SELF TEST
RESET
DIGITAL CIRCUITS
VOLTAGE SELECTOR MODULE
50/60 Hz AC LINE POWER
A13 SWITCHING POWER SUPPLY PCB
A14 MOTHERBOARD PCB
POWER SUPPLY VOLTAGES & INTERFACE SIGNALS
UNIVERSAL CIRCUITS (ALL MODELS)
ANALOG CIRCUITS
AC LINE VOLTAGE
μP Bus
EOB
A2 RAMP GENERATOR PCB
RAMP OUT
INTENSITY MARKER
A3 MARKER GENERATOR PCB
F0 IDENTIFY
M1 IDENTIFY
M2 IDENTIFY
MODIFY SIGNAL
RAMP, 0-10V
MP Bus
ROM Bus
RF MARKER
A4 AUTOMATIC LEVEL CONTROL PCB
RF SLOPE
EXTERNAL INPUT
ALC IN
RAMP IN
A5 FREQUENCY INSTRUCTION PCB
MANUAL SWEEP
FC Bus
FCEN/VPF
F CORR
FCEN
ΔF ≤ 50 MHz
ΔF > 50 MHz
EXT FM IN
A10 FM ATTENUATOR PCB
ATTN 1-4
TRACK FILTER COIL
YIG FM COIL
TRACK FILTER 1
EXT TRIGGER IN
BANDSWITCH BLANKING (+), (−)
RETRACE BLANKING (+), (−)
SEQ SYNC
VIDEO MARKER
HORIZ OUT
EXT FM IN
A6 HET/YIG DRIVER PCB
TUNING & BIAS VOLTAGES
HET YIG SEL
YIG 1 FM COIL SEL
TRACK FILTER 1
PIN MOD DRIVER
SNB 1
SNR 1
A7 YIG DRIVER PCB
TUNING & BIAS VOLTAGES
YIG 2 FM COIL SEL
SNB 2
SNR 2
A8 YIG DRIVER PCB
YIG 3 FM COIL SEL
SNB 3
SNR 3
A9 YIG DRIVER PCB
MOD D
2-8 G
8-12.4
12.4-18
18-26.5
RF COMPONENT
MODEL DEPEN

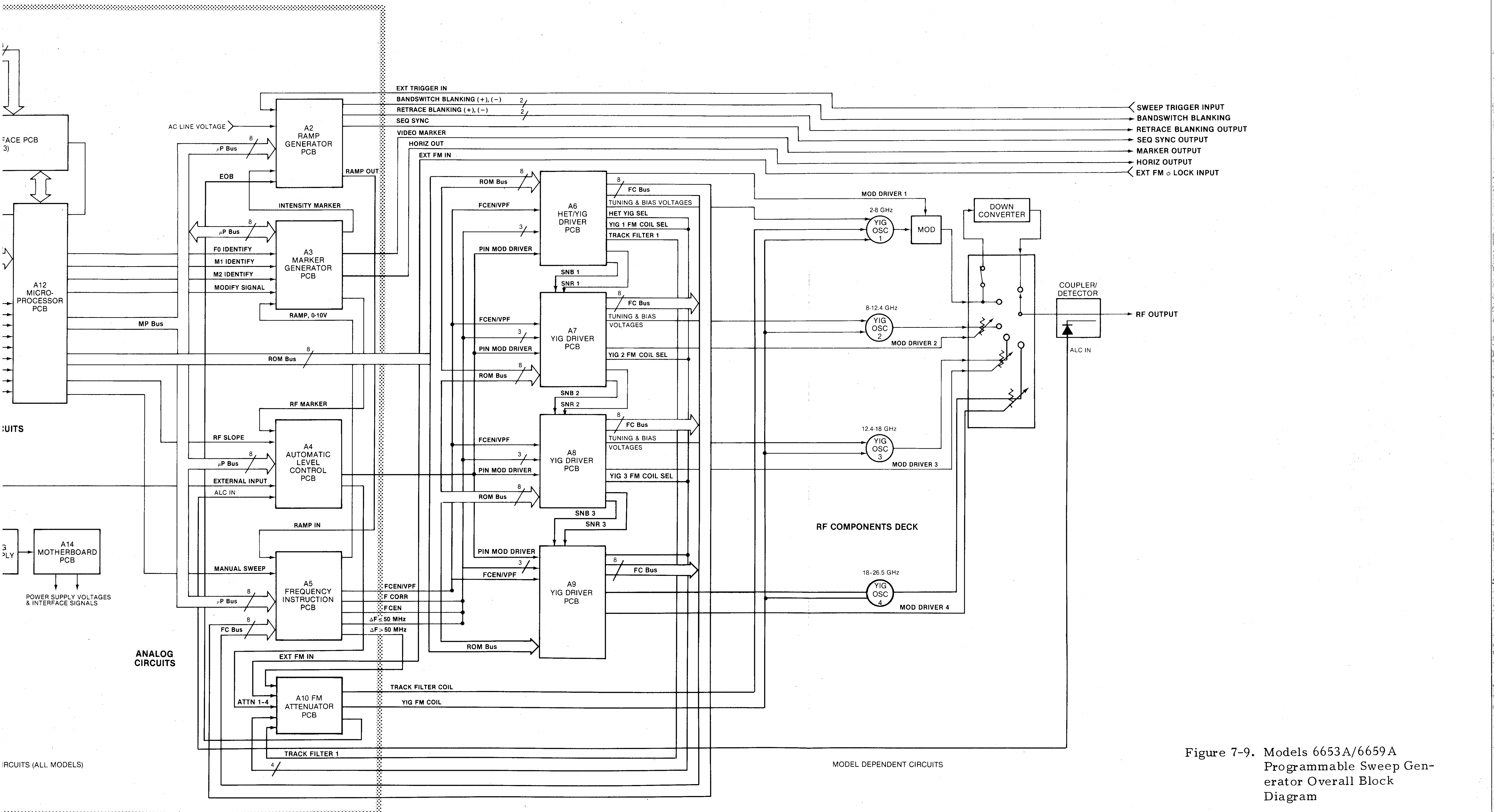
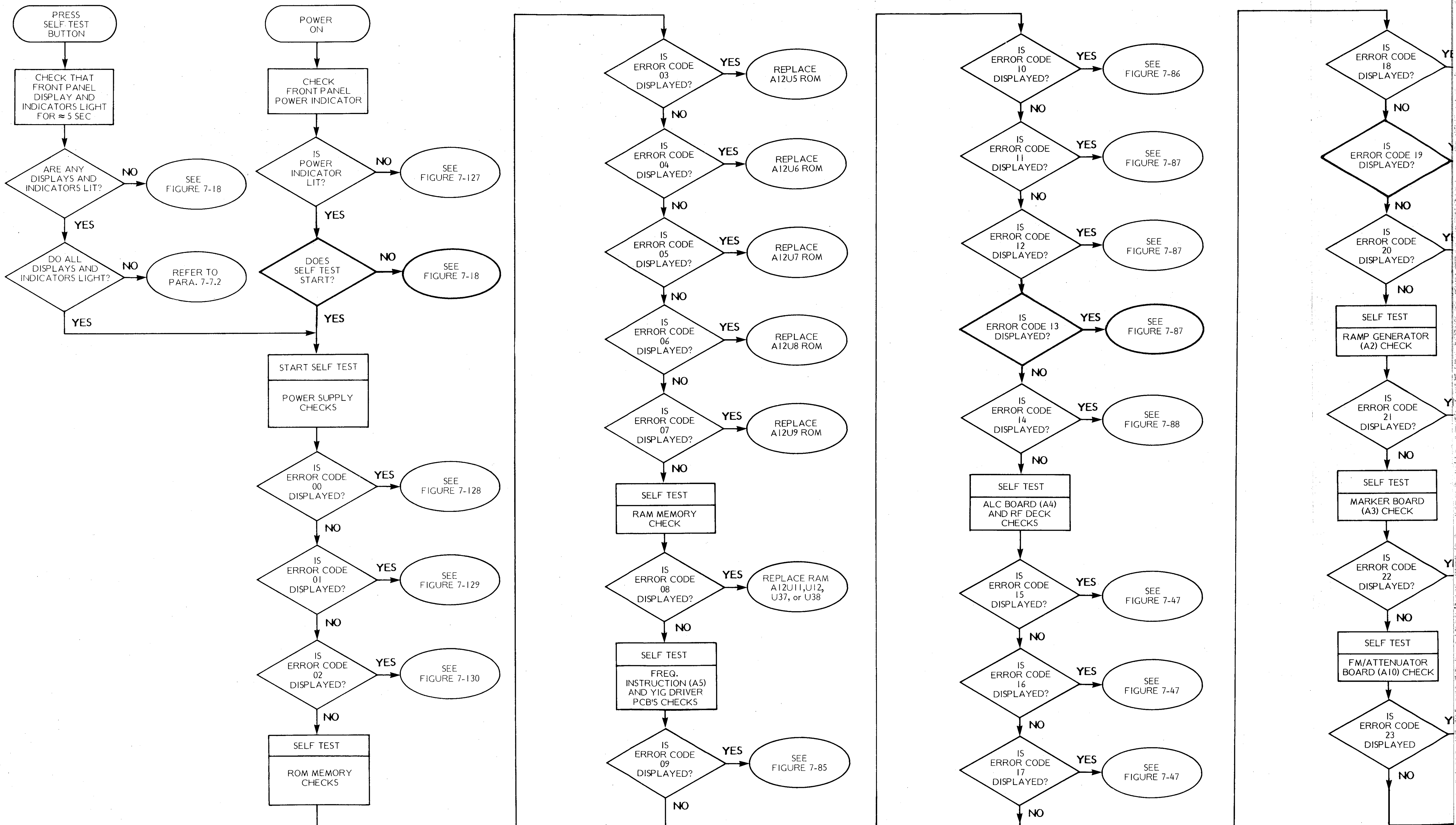


Figure 7-9. Models 6653A/6659A Programmable Sweep Generator Overall Block Diagram


PRESS SELF TEST BUTTON
CHECK THAT FRONT PANEL DISPLAY AND INDICATORS LIGHT FOR ≈ 5 SEC
ARE ANY DISPLAYS AND INDICATORS LIT?
NO
SEE FIGURE 7-18
YES
DO ALL DISPLAYS AND INDICATORS LIGHT?
NO
REFER TO PARA. 7-7.2
YES
POWER ON
CHECK FRONT PANEL POWER INDICATOR
IS POWER INDICATOR LIT?
NO
SEE FIGURE 7-127
YES
DOES SELF TEST START?
NO
SEE FIGURE 7-18
YES
START SELF TEST
POWER SUPPLY CHECKS
IS ERROR CODE 00 DISPLAYED?
YES
SEE FIGURE 7-128
NO
IS ERROR CODE 01 DISPLAYED?
YES
SEE FIGURE 7-129
NO
IS ERROR CODE 02 DISPLAYED?
YES
SEE FIGURE 7-130
NO
SELF TEST
ROM MEMORY CHECKS
IS ERROR CODE 03 DISPLAYED?
YES
REPLACE A12U5 ROM
NO
IS ERROR CODE 04 DISPLAYED?
YES
REPLACE A12U6 ROM
NO
IS ERROR CODE 05 DISPLAYED?
YES
REPLACE A12U7 ROM
NO
IS ERROR CODE 06 DISPLAYED?
YES
REPLACE A12U8 ROM
NO
IS ERROR CODE 07 DISPLAYED?
YES
REPLACE A12U9 ROM
NO
SELF TEST
RAM MEMORY CHECK
IS ERROR CODE 08 DISPLAYED?
YES
REPLACE RAM A12U11,U12, U37, or U38
NO
SELF TEST
FREQ. INSTRUCTION (A5) AND YIG DRIVER PCB'S CHECKS
IS ERROR CODE 09 DISPLAYED?
YES
SEE FIGURE 7-85
NO
IS ERROR CODE 10 DISPLAYED?
YES
SEE FIGURE 7-86
NO
IS ERROR CODE 11 DISPLAYED?
YES
SEE FIGURE 7-87
NO
IS ERROR CODE 12 DISPLAYED?
YES
SEE FIGURE 7-87
IS ERROR CODE 13 DISPLAYED?
YES
SEE FIGURE 7-87
NO
IS ERROR CODE 14 DISPLAYED?
YES
SEE FIGURE 7-88
NO
SELF TEST
ALC BOARD (A4) AND RF DECK CHECKS
IS ERROR CODE 15 DISPLAYED?
YES
SEE FIGURE 7-47
NO
IS ERROR CODE 16 DISPLAYED?
YES
SEE FIGURE 7-47
NO
IS ERROR CODE 17 DISPLAYED?
YES
SEE FIGURE 7-47
NO
IS ERROR CODE 18 DISPLAYED?
NO
IS ERROR CODE 19 DISPLAYED?
NO
IS ERROR CODE 20 DISPLAYED?
NO
SELF TEST
RAMP GENERATOR (A2) CHECK
IS ERROR CODE 21 DISPLAYED?
NO
SELF TEST
MARKER BOARD (A3) CHECK
IS ERROR CODE 22 DISPLAYED?
NO
SELF TEST
FM/ATTENUATOR BOARD (A10) CHECK
IS ERROR CODE 23 DISPLAYED
NO

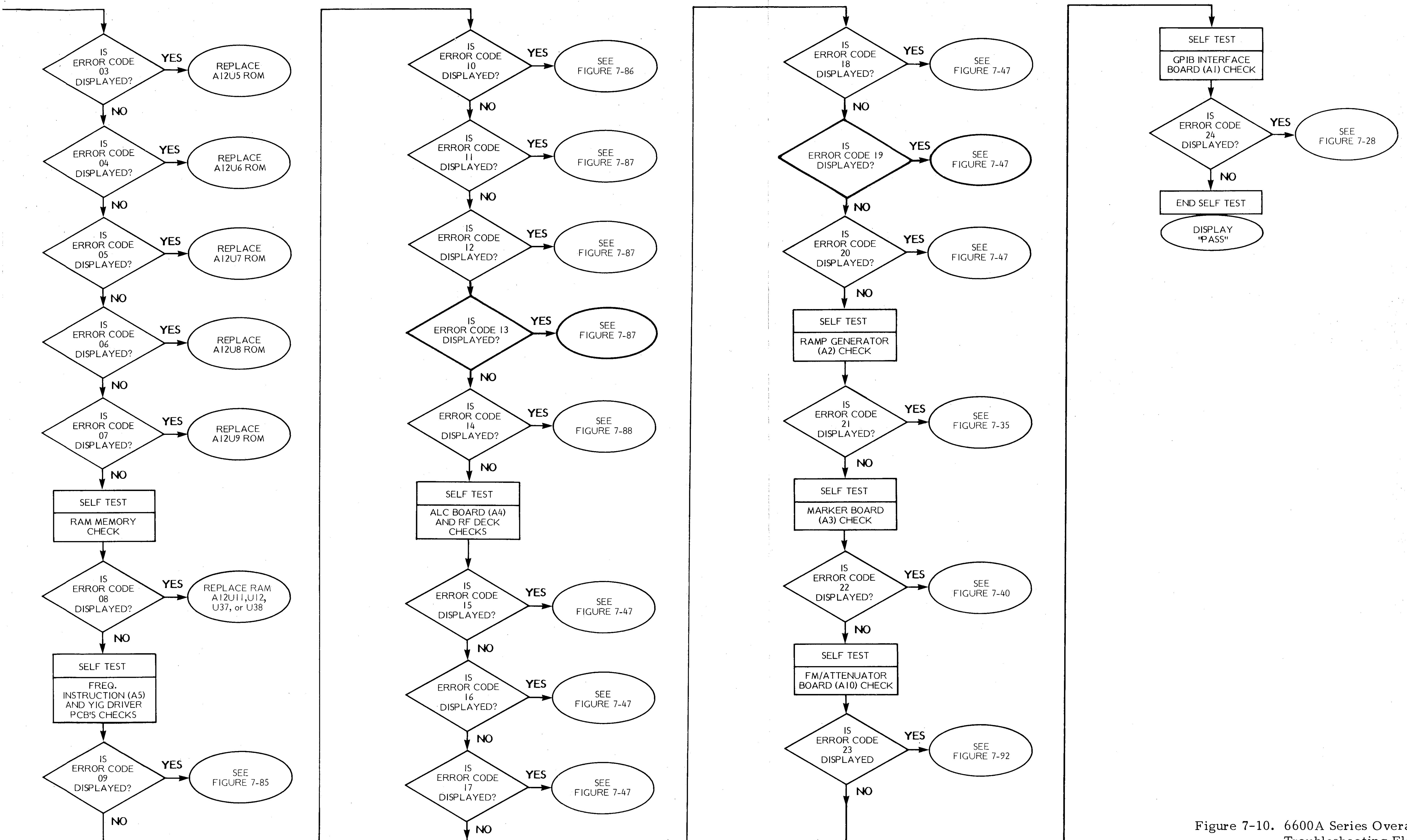


Figure 7-10. 6600A Series Overall Troubleshooting Flowchart

7-5 6600A SERIES PROGRAMMABLE SWEEP GENERATOR, OVERALL TROUBLESHOOTING

Troubleshooting for the 6600A Series Sweep Generators is facilitated by the self-test error codes described in paragraph 3-4. When used with the supplemental flowcharts and block diagrams provided in this section, these error codes can be used to isolate most malfunctions to the defective functional or integrated circuit. A flowchart for troubleshooting the self-test error codes is provided in Figure 7-10 (facing page).

7-6 A12 MICROPROCESSOR PCB

7-6.1 A12 Microprocessor PCB, Circuit Description

The A12 Microprocessor PCB controls the operation of the sweep generator. It also provides, via the A11 Front Panel PCB, the interface between the front panel pushbuttons and the analog sweep- and microwave-generating circuitry. To provide this control, the A12 PCB contains an 8085 Microprocessor integrated circuit (IC), an 8279 Keyboard/Display Interface IC, 10k bytes of read-only memory (ROM), and 512 bytes of read/write memory (RAM). A block diagram of the A12 PCB circuitry is provided in Figure 7-11. A diagram showing the distribution of control-group data between the A12 PCB and the A2-A5 and A14 PCBs is provided in Figure 7-12; descriptions of these data are provided in Appendix III. A flowchart showing the microprocessor's ac power-on operational program is provided in Figure 7-13. A parts locator diagram for the A12 PCB is provided in Figure 7-14. And the A12 PCB schematics (5 sheets) are provided in Figure 7-15.

The 8279 IC (U25) (Figure 7-11) interfaces the microprocessor with the front panel pushbuttons and numeric displays. This IC, via its scan lines (the **SL0-SL3 &L CAD Bus**), causes the front panel pushbuttons and numeric-display digits to be continually scanned. When the user selects a pushbutton, an 8-bit digitally coded word (keycode) representing that pushbutton is sent over the **COL1-COL8 Bus** to the keyboard controller (8279), and eventually to the microprocessor. Conversely, when the microprocessor selects a numeric display for update, a likewise-coded word representing the display segment is sent over the **NA0-NA3/NB0-NB3 Bus** to one of the three displays.

The Latch (U31) and Flash Logic (U34, U35) circuits interface the microprocessor with the EXTERNAL ALC GAIN CAL (ALC CAL), SWEEPING, RF OFF, and UNLEVELED (flashing) front panel LEDs. The interface with the other (non-flashing) LEDs is via the data bus and six latches on the A11 PCB.

The Bidirectional Buffer #2 circuit (U13) interfaces the microprocessor with analog PCBs A2-A5, ROM Bus latch A14U6, and diagnostic (self-test) latches A14U7, U8, and U10 – all on the motherboard. Also, if Option 3 is installed, U13 interfaces the microprocessor with the A1 GPIB Interface PCB.

The Control Signal Input Ports (U29, U30) are latch/buffers that allow control signal data from the A2, A3, and A4 analog PCBs, the A1 GPIB Interface PCB (Option 3 only), and the A11 Front Panel PCB to be input into the microprocessor.

The Bidirectional Buffer #1 circuit (U14) buffers the input/output interface circuitry from the microprocessor "kernel," the control element on the A12 PCB. This kernel consists of:

a. <u>8085 Microprocessor (U2)</u>. U2 is a complete central-processing unit (CPU); it contains all of the necessary registers, plus the arithmetic logic unit (ALU) and control circuitry.

b. <u>Address Decoders (U3, U4)</u>. U3 and U4 decode the A8-A14 and A0-A7 address lines, providing addresses for the memory circuits.

c. <u>5101 RAM (U11, U12, U37, U38), RAM Buffer (U10), and RAM Battery (B1, U1)</u>. The RAM circuits store the data input via the front panel pushbuttons. The RAM Battery provides operating power for the read/write memory when the ac power is turned off, making this memory non-volatile.

d. 2716 ROM (U5-U9). The ROM circuits contain both the microprocessor ac power-on operational program (Figure 7-13) and the reset (default) parameter data (paragraph 3-7.1).

e. Free-Run Socket (J9). J9 provides for testing of the microprocessor. The removal of J9 forces a series of no-operation (NOP) instructions on the microprocessor, thus causing it to free-run.

f. Port Decoders (U18-U23). The port decoders are divided between input and output ports. U19-U21 are output port decoders, U22 and U23 are input port decoders, and U18 is a port-decoder-enable circuit.

U19-U21 decode the microprocessor output-port data and select one of 24 output ports. The selected port then receives the data that the microprocessor has concurrently sent over the data bus. The output-port-select lines are **SP0** thru **SP23**. The **SP0-SP15** lines go to the analog PCB ports, located on the individual A2-A5 and A14 PCBs (Figure 7-12). **SP16-SP21** go to the front-panel non-flashing LED ports, A11U1 thru A11U6. The **SP22** line goes to the front-panel flashing LED port, A12U31. And the **SP23** line goes to the GPIB Interface PCB µP-data input port, A1U22 (Option 3 only).

U22 and U23 decode the microprocessor input-port data and select one of the eight latch/buffer circuit input ports. When selected, the port then allows the data that is concurrently on the A14 **µP Data Bus** to be input into the microprocessor. The input port data is divided into four types: diagnostics (self-test) data, GPIB data (Option 3 only), INCREASE/DECREASE lever frequency data, and control-signal data. Input port select lines **SX1**, **SX2**, and **SX7** select the diagnostics data; SX3 selects the GPIB data; **SX4** and **SX29** select the INCREASE/DECREASE lever frequency data; and **SX24** and **SX25** select the control-signal data.

g. SERVICE-NORMAL Switch **(S1)**. In the SERVICE position, S1 interrupts the microprocessor and causes it to run a stimulus routine for signature-analysis testing.

The A14 Motherboard PCB components that are functionally part of the microprocessor circuitry consist of the Linearizer ROM Latch, A14U6, and the Diagnostic (Self Test) Latches A14U7, U8, and U10.

The Linearizer-ROM Latch, U6, supplies address data to the linearizer ROMs located on the A6, A7, A8, and A9 YIG Driver PCBs. When clocked by SP5, U5 latches the microprocessor-supplied ROM address data from its input to its output circuit. The output-circuit data is supplied to each of the YIG driver PCBs, via the ROM bus.

The Diagnostic (Self Test) and Misc'l Signal Buffers, U7, U8, and U10, are respectively enabled by the **SX1**, **SX2**, and **SX7** input-port select lines from the microprocessor. When a buffer is enabled, the data that has been latched into its input circuit is allowed to pass to its output circuit. The input lines to the diagnostic buffers are as follows:

h. U7 Buffer:

1. **L YIG 1 SEL**, from A6 PCB.
2. **L YIG 2 SEL**, from A7 PCB.
3. **L YIG 3 SEL**, from A8 PCB.
4. **L YIG 4 SEL**, from A9.
5. **H SNR 1**, from A6 PCB.
6. **H SNR 2**, from A7 PCB.
7. **H SNR 3**, from A8 PCB.
8. **H SNR 4**, from A9.

i. U8 Buffer:

1. **H DWELL**, from A2 PCB.
2. **L HET YIG SEL**, from A6 PCB.
3. **H FM DIAG**, from A10 PCB.

j. U10 Buffer:

1. **L OR**, from A14U5 (switching power supply).
2. **L HL**, from A14U5 (switching power supply).

Para. 7-6.1 (cont'd.)

3. **L LL**, from A14U5 (switching power supply).
4. **GPIB IN**, from A1 PCB (Option 3).
5. **L DWELL DETECTED**, from A2 PCB.
6. **HORIZ OUTPUT DURING CW**, from XA16 connector.

:B.
:rom

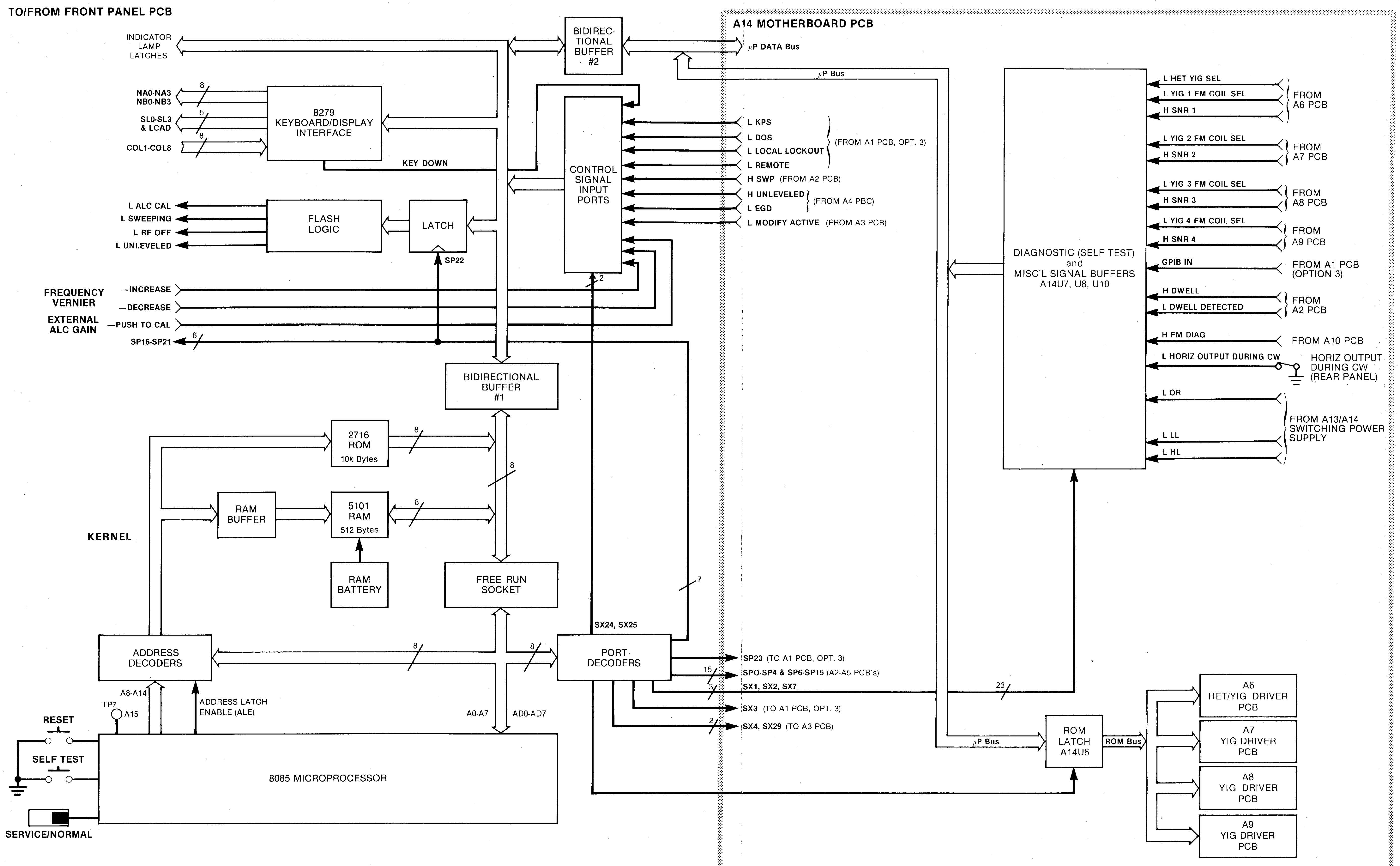


Figure 7-11. Microprocessor Overall Block Diagram

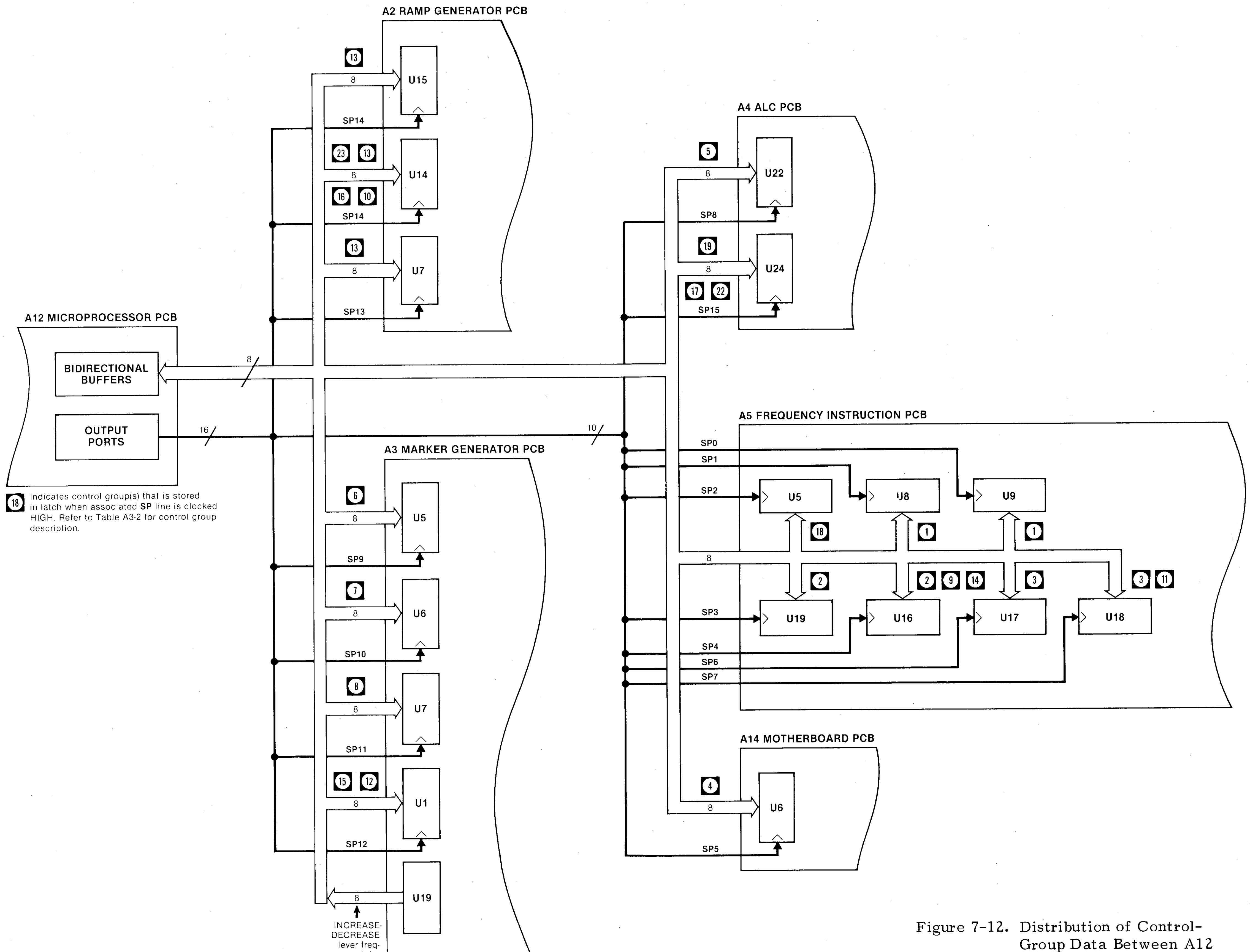


Figure 7-12. Distribution of Control-Group Data Between A12 and A2-A5 and A14 PCBs

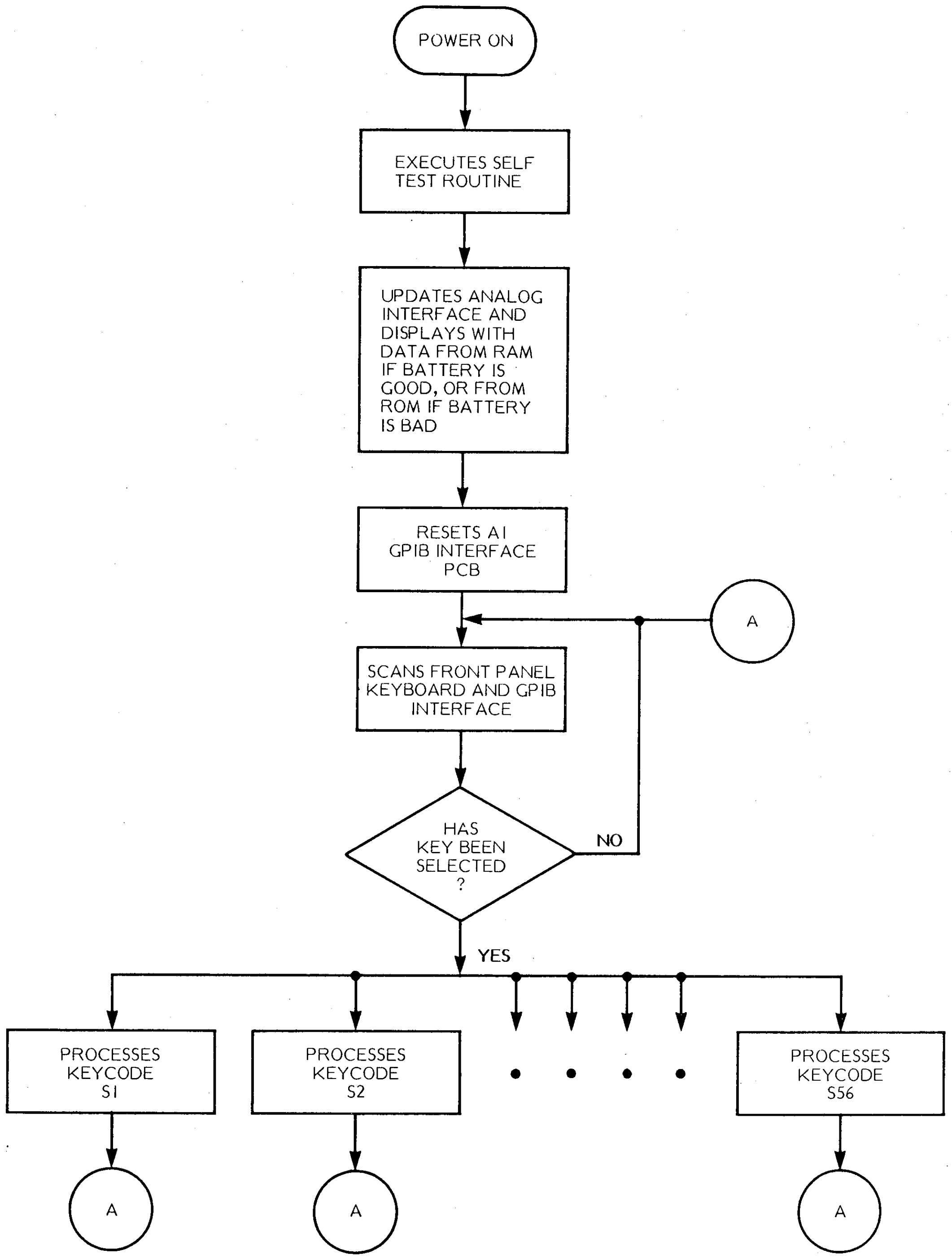


Figure 7-13. A12 Microprocessor PCB AC Power-On Operational Flowchart

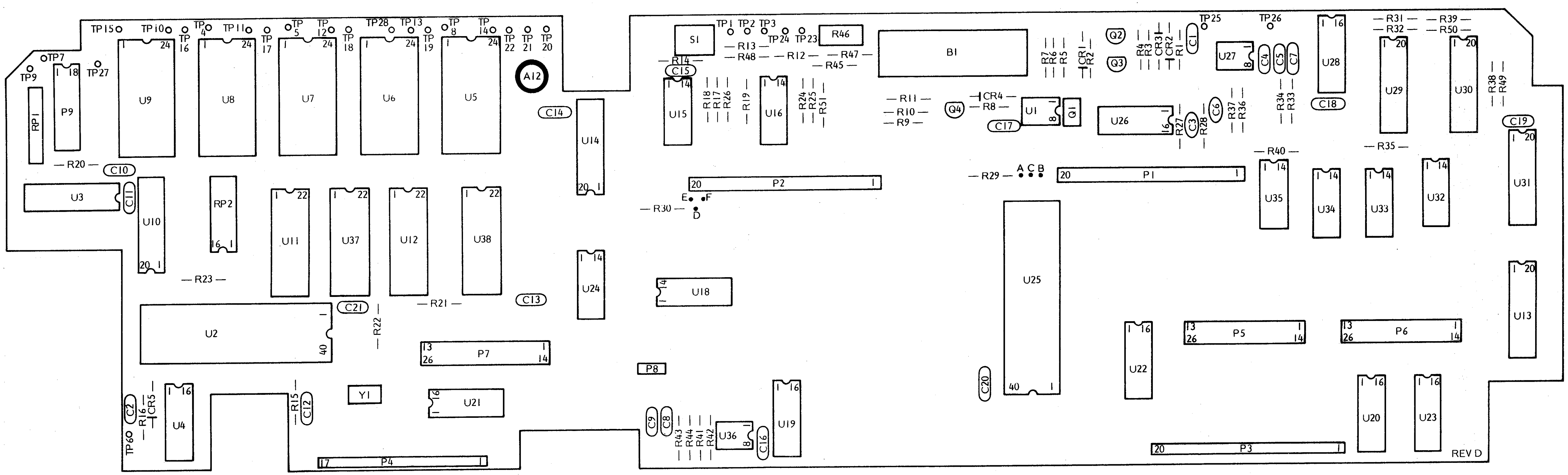
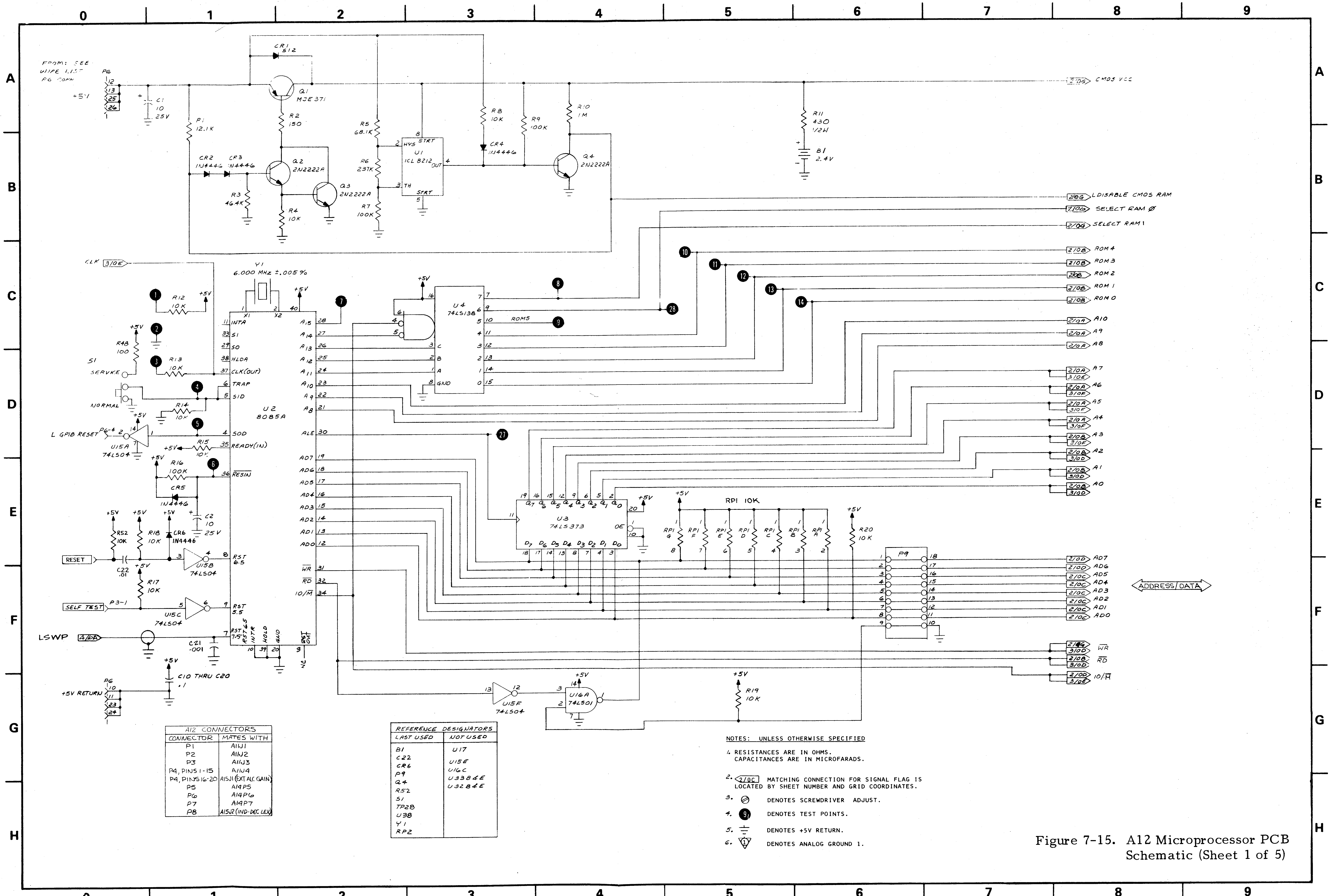


Figure 7-14. A12 Microprocessor PCB Parts Locator Diagram



A12 CONNECTORS	
CONNECTOR	MATES WITH
P1	A11J1
P2	A11J2
P3	A11J3
P4, PINS 1-15	A11J4
P4, PINS 16-20	A15J1 (EXT ALC GAIN)
P5	A14P5
P6	A14P6
P7	A14P7
P8	A15J2 (IND-DEC LEV)

REFERENCE DESIGNATORS	
LAST USED	NOT USED
B1	U17
C22	U15E
CR6	U16C
P9	U33B&E
Q4	U32B&E
R52	
S1	
TP28	
U38	
Y1	
RP2	

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS.
2. 2/0C MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
3. DENOTES SCREWDRIVER ADJUST.
4. 9 DENOTES TEST POINTS.
5. DENOTES +5V RETURN.
6. 1 DENOTES ANALOG GROUND 1.

Figure 7-15. A12 Microprocessor PCB Schematic (Sheet 1 of 5)

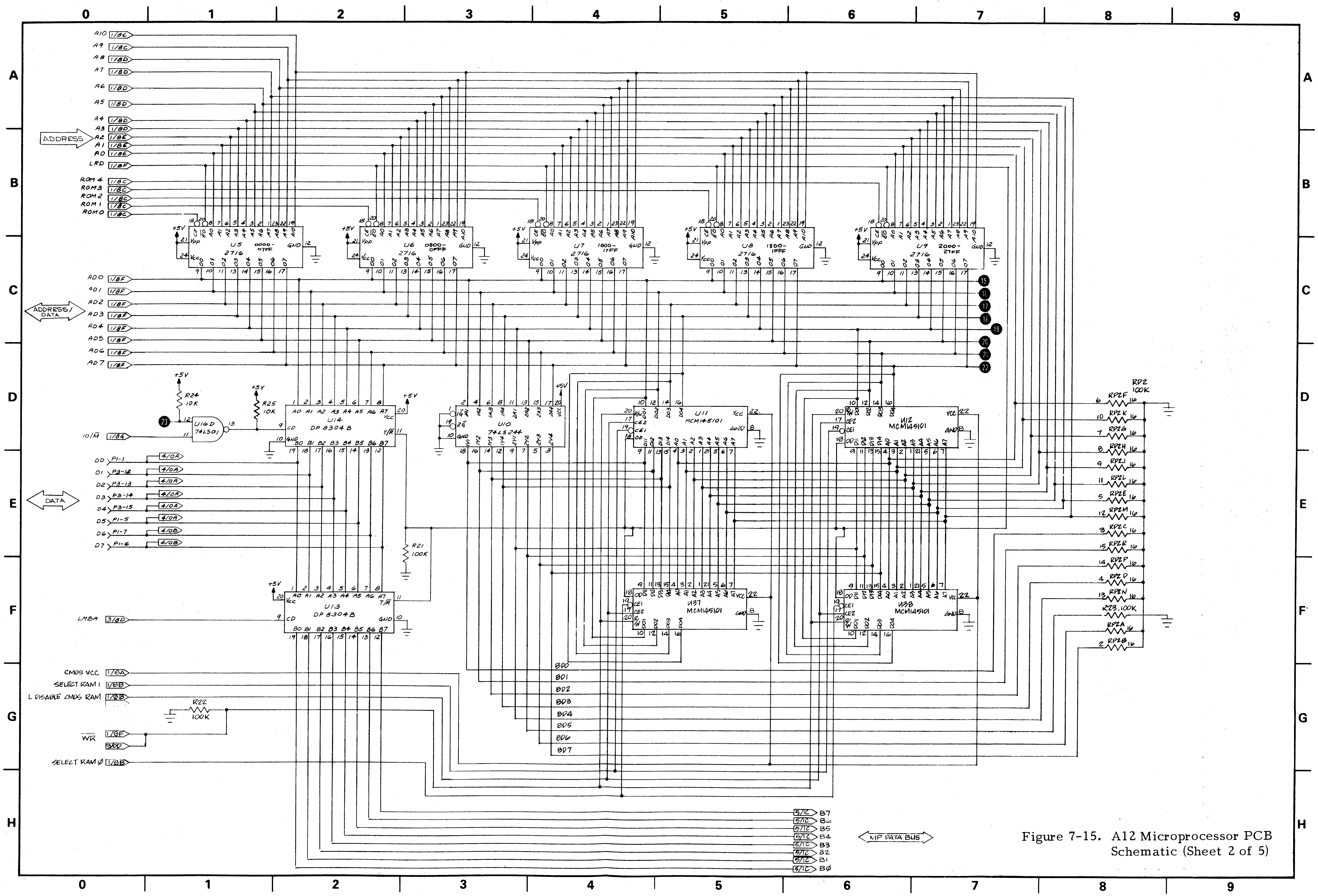


Figure 7-15. A12 Microprocessor PCB Schematic (Sheet 2 of 5)

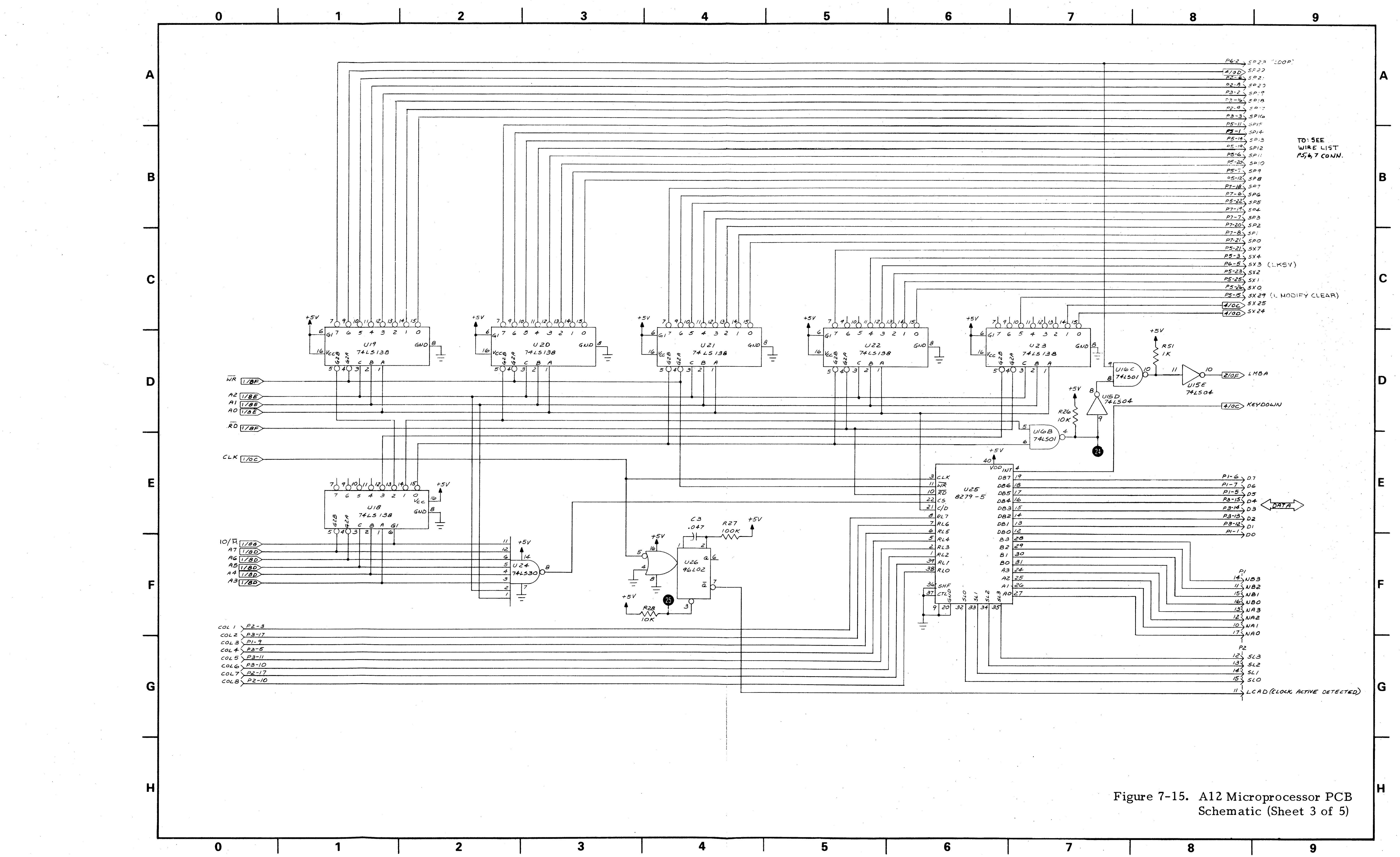


Figure 7-15. A12 Microprocessor PCB Schematic (Sheet 3 of 5)

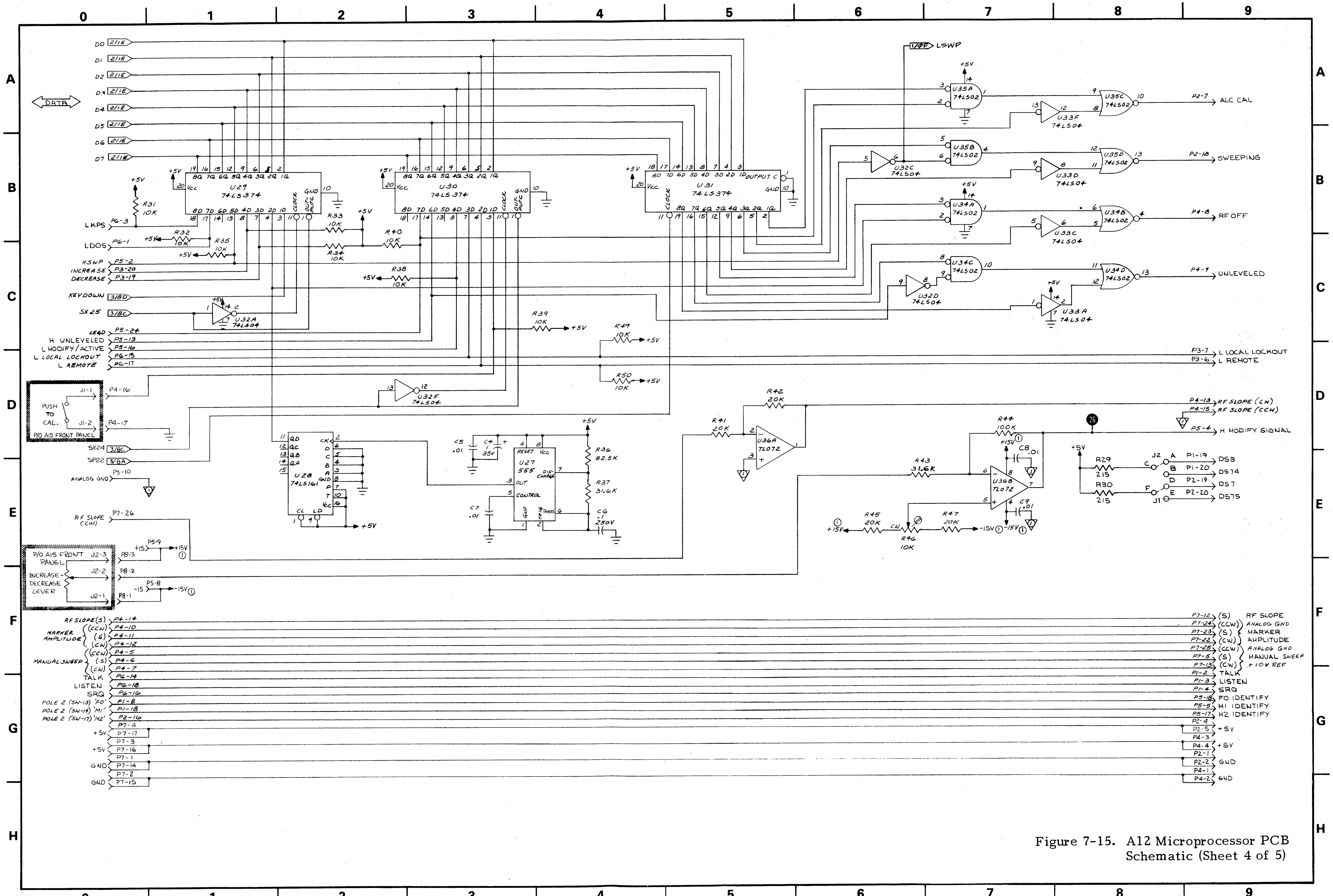


Figure 7-15. A12 Microprocessor PCB Schematic (Sheet 4 of 5)

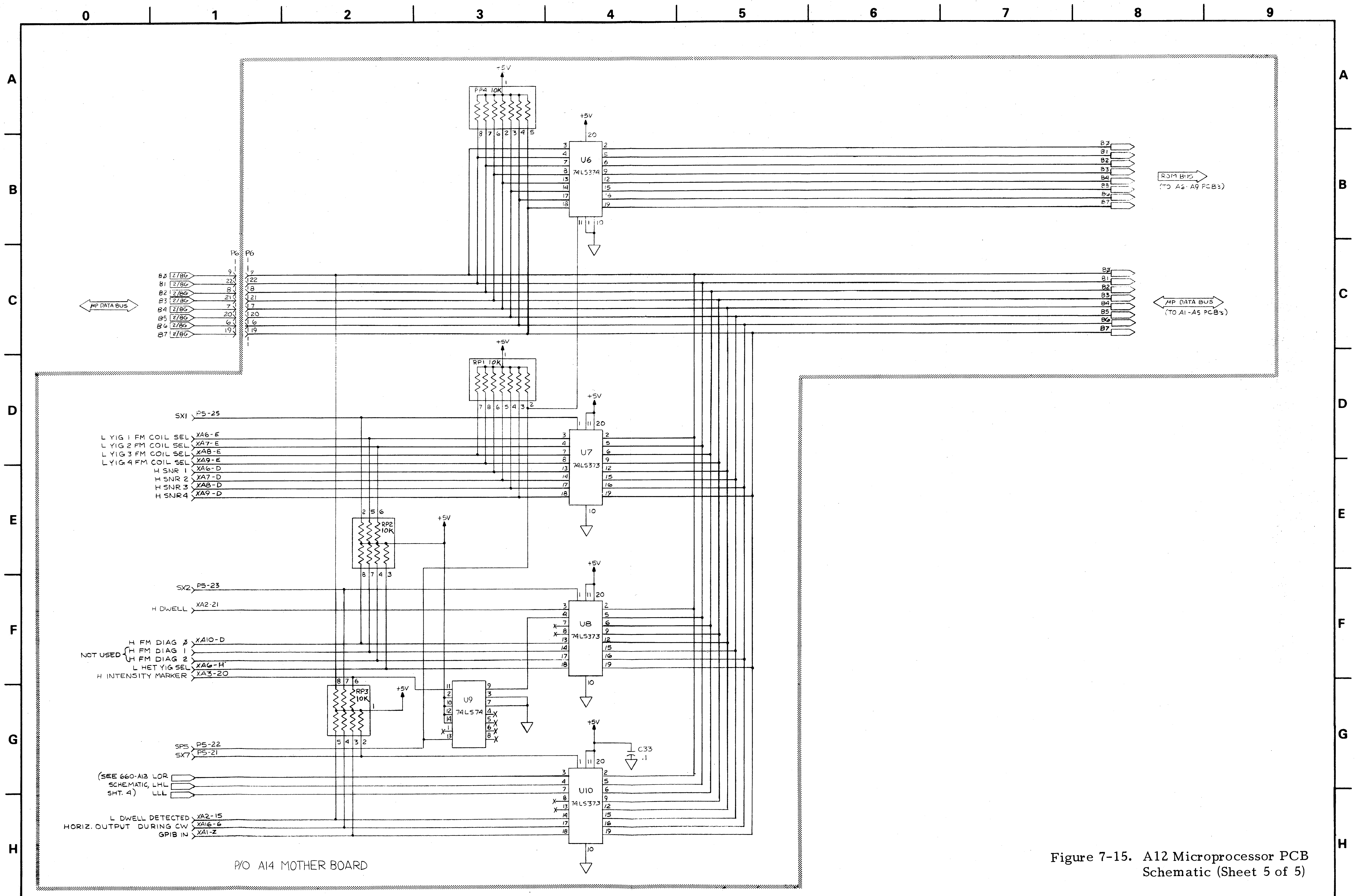


Figure 7-15. A12 Microprocessor PCB Schematic (Sheet 5 of 5)

7-6.2 A12 Microprocessor PCB, Troubleshooting Information and Data

There is no error code for the A12 Microprocessor PCB. Read-only-memory (ROM) or read/write memory (RAM) malfunctions occurring in the microprocessor kernel (Figure 7-11) will cause the respective ROM's or RAM's error code to be displayed. Other malfunctions occurring within the kernel will probably result in the sweep generator's not turning on. And malfunctions occurring outside the kernel will probably result in the display of one or more analog circuit error codes. The test equipment setup for troubleshooting the A12 PCB is provided in Figure 7-16; the troubleshooting flowchart is provided in Figure 7-18.

Signature analysis is the recommended method for troubleshooting A12 circuits. In addition to a free-run mode (explained in HP Application Note 222-2), the A12 PCB also has a service mode. In this mode, routines stored in ROM U5 provide two methods for isolating to faulty components.

The first method uses a "loop-on-fail" technique (Figure 7-17) that allows the signature analyzer to quickly isolate to a malfunctioning RAM or ROM circuit. In this method the signature analyzer will display one of seven characteristic (Vcc) signatures, depending on which loop is being executed. If no errors are found, a specific signature is displayed. An error in the RAM provides a different signature. And an error in the ROM provides one of five different signatures, depending upon which chip (U5-U9) is at fault.

The second service-mode method, a routine which writes to the output ports and 8279 Keyboard/Display Interface IC, provides for signature analysis of these components. Thus, signature analysis can be used to verify whether a selected analog-PCB-mounted output port is being enabled. It can also be used to test whether the 8279 will respond to selected front panel pushbuttons. These tests are contained in Tables 7-5 and 7-6 respectively. Note that the Table 7-5 signatures are dependent on the software version contained in ROM. The software-version number (e.g. 1.7, 3.2, 4.0 etc.) momentarily appears on a front panel display at the beginning of self test. It also appears on a label affixed to ROMs U5-U9.

For free-run signature analysis, two tables of signatures are provided. Tables 7-3 and 7-4 respectively provide signatures for the microprocessor's read and write spaces. Both of these tables provide test and signature analyzer setup conditions. When these conditions are met, a characteristic (Vcc) signature will be displayed; the microprocessor circuit may then be accurately tested.

In addition to signatures, the 5004A Signature Analyzer data probe may be used like a logic probe. When a circuit node is touched, the probe tip will either flash, light steadily, or not be lit. A steadily lit probe indicates a logic 1 or Vcc. An unlit probe indicates a logic 0 or ground. And a flashing probe usually indicates pulses; however, it can also indicate noise. A noise indication sometimes occurs when the probe is touched to an open node, or when it is touched to a tri-state-buffer node where the buffer is in its off state. When testing such nodes, the 5004A will read the Vcc signature when its RESET button is pressed. To help minimize probe noise pickup, ground the probe at the same point the test pod is grounded.

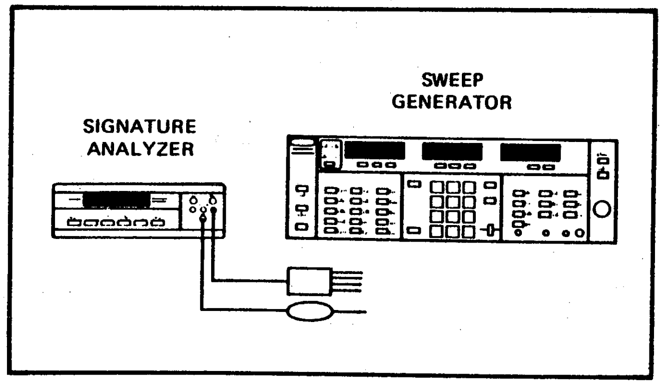


Figure 7-16. Test Setup for Troubleshooting A12 PCB

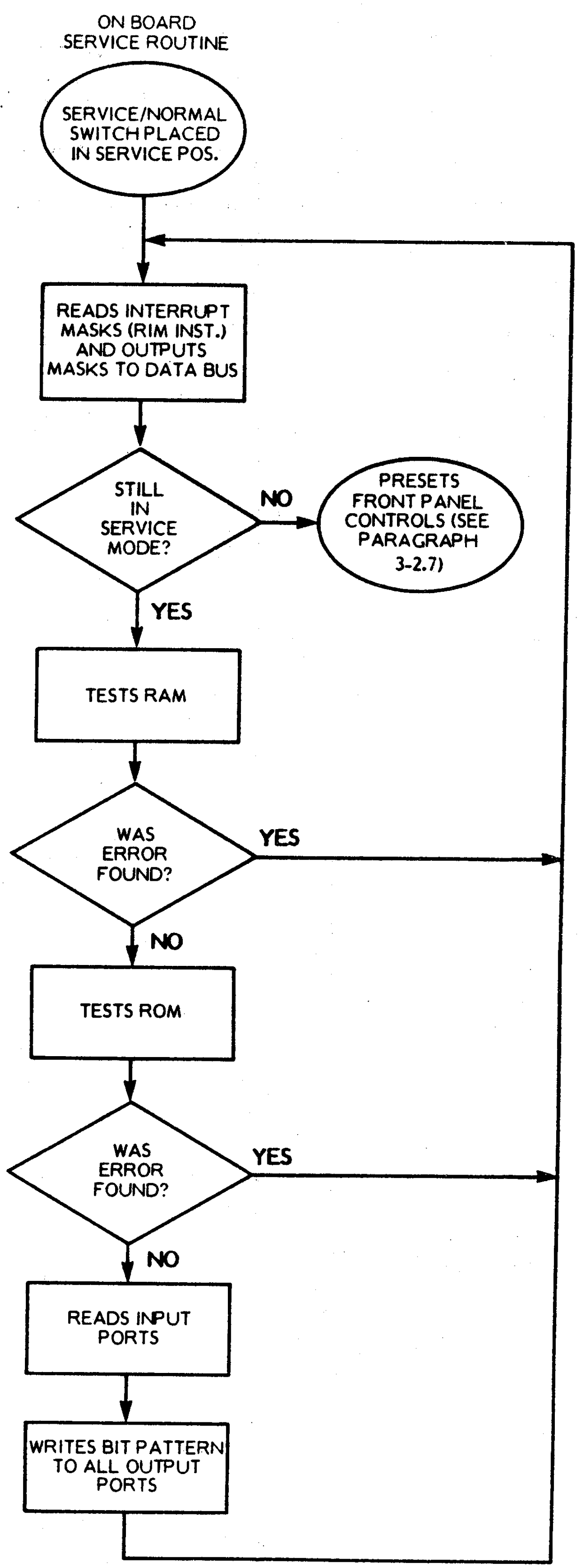


Figure 7-17. A12 PCB On-Board Service Routine

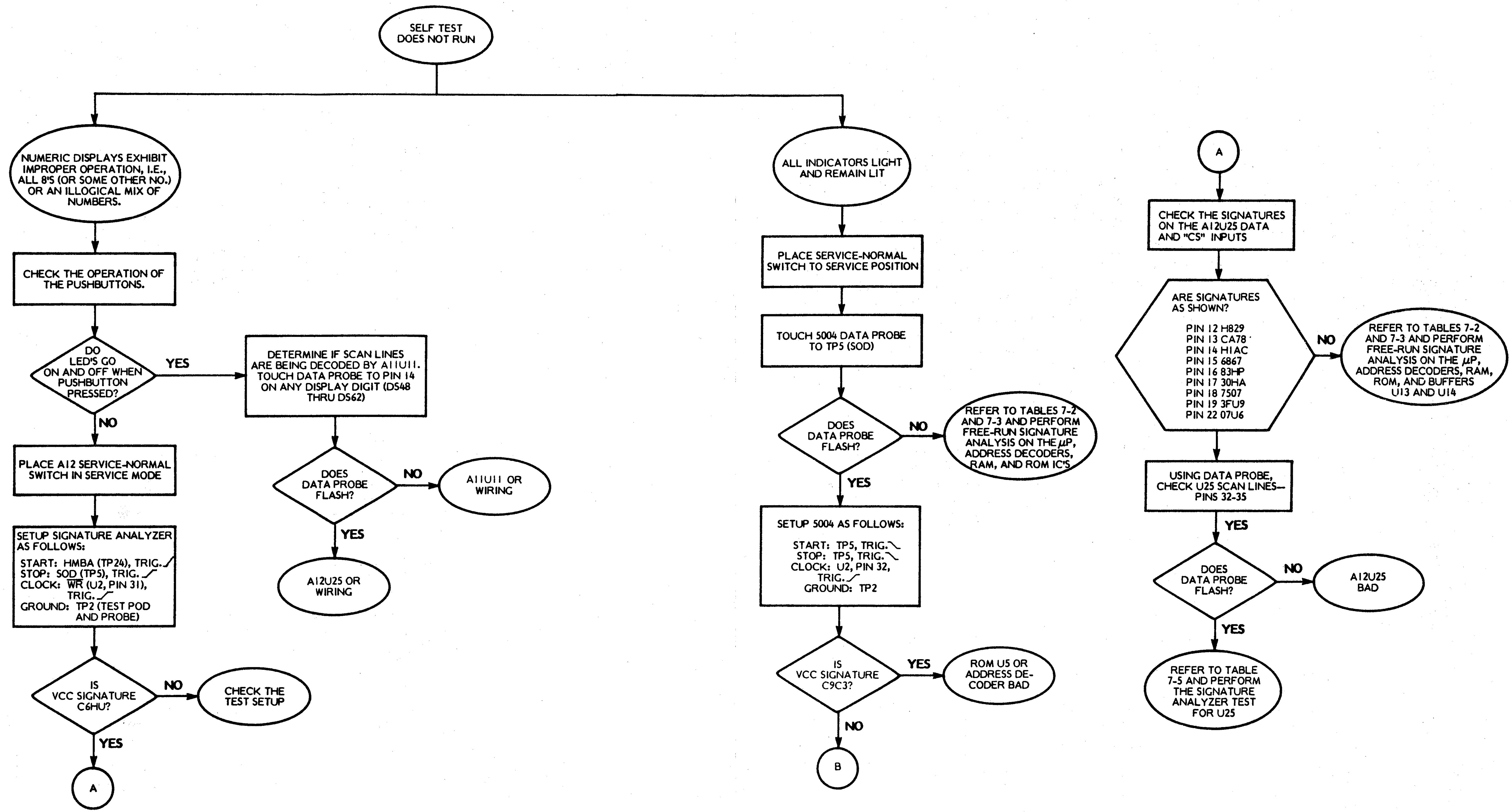


Figure 7-18. A12 PCB Troubleshooting Flowchart (Sheet 1 of 2)

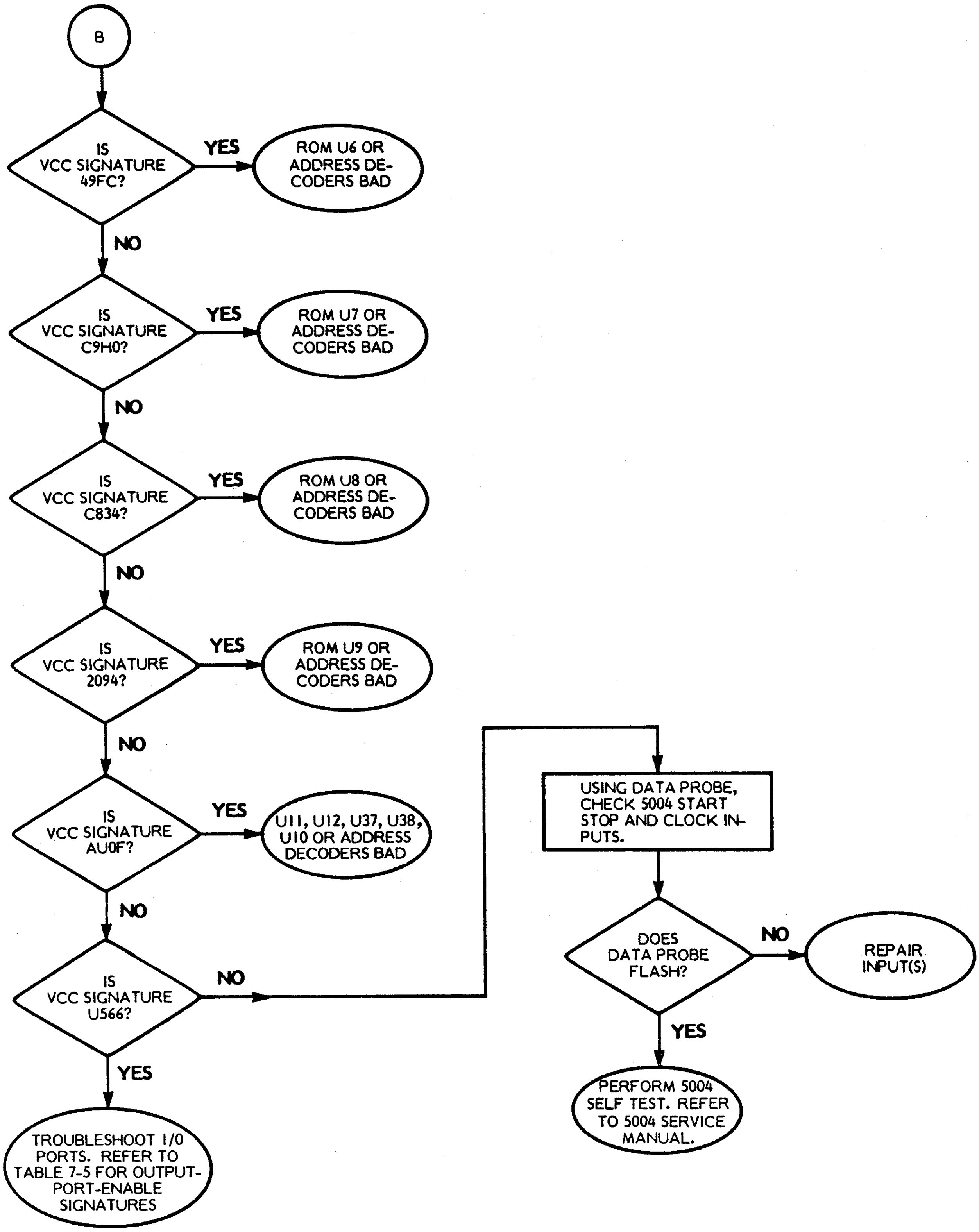


Figure 7-18. A12 PCB Troubleshooting Flowchart (Sheet 2 of 2)

Table 7-3. A12 PCB Free-run Mode Signatures – Read Space Test

GENERAL:

Test Conditions: TEST-NORMAL Switch in NORMAL.
Free-run jumper J9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP7), Trigger ╲ (Button In)

STOP: Bit A15 (TP7), Trigger ╱ (Button Out)

CLOCK: $\overline{RD}$ (U2, Pin 32), Trigger ╱ (Button Out)

Vcc Signature: 755U

NOTES

[1] Test probe flashes.
[2] Signature may be unstable.
[3] May have to press RESET on probe.

IC	PIN NO.	SIGNATURE
U1	1	755U
	2	755U
	3	755U
	4	0000
	5	0000
	6	0000
	7	0000
	8	755U
U2	1	0000[1]
	2	755U[1]
	3	0000
	4	0000
	5	0000
	6	0000
	7	0000
	8	0000
	9	0000
	10	0000
	11	755U
	12	755U[1]
	13	755U[1]
	14	755U[1]
	15	755U[1]
	16	755U[1]
	17	755U[1]
	18	755U[1]
	19	0000[1]
	20	0000
	21	7707
	22	577A
	23	HH86
	24	89F1
	25	AC99
	26	PCF3
	27	1180
	28	0000[1]
	29	755U
	30	0000[1]
	31	755U

IC	PIN NO.	SIGNATURE
U2	32	0000[1]
	33	755U
	34	0000
	35	755U
	36	755U
	37	755U[1]
	38	0000
	39	0000
	40	755U
U3	1	0000
	2	H335
	3	755U[1]
	4	755U[1]
	5	C113
	6	7050
	7	755U[1]
	8	755U[1]
	9	0772
	10	0000
	11	0000[1]
	12	C4C3
	13	755U[1]
	14	755U[1]
	15	AA08
	16	7211
	17	755U[1]
	18	0000[1]
	19	A3C1
	20	755U
U4	1	89F1
	2	AC99
	3	PCF3
	4	1180
	5	0000
	6	755U
	7	6F7P
	8	0000
	9	F615
	10	2F25

IC	PIN NO.	SIGNATURE
U4	11	8UH9
	12	340A
	13	P352
	14	U1U2
	15	4CP2
	16	755U
U5	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	4CP2
	19	HH86
	20	0000[1]
	21	755U
	22	577A
	23	7707
	24	755U
U6	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	U1U2
	19	HH86
	20	0000[1]
	21	755U
	22	577A
	23	7707
	24	755U

IC	PIN NO.	SIGNATURE
U7	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	P352
	19	HH86
	20	0000[1]
	21	755U
	22	577A
	23	7707
	24	755U
U8	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	340A
	19	HH86
	20	0000[1]
	21	755U
	22	577A
	23	7707
	24	755U
U9	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050

IC	PIN NO.	SIGNATURE
U9	7	C113
	8	H335
	12	0000
	18	8UH9
	19	HH86
	20	0000
	21	755U
	22	577A
	23	7707
	24	755U
U18	1	0772
	2	C4C3
	3	AA08
	4	7211
	5	A3C1
	6	0000
	7	755U
	8	0000
	9	755U
	10	755U
	11	755U
	12	755U
	13	755U
	14	755U
U19	1	H335
	2	C113
	3	7050
	4	755U
	5	755U
	6	755U
	7	755U
	8	0000
	9	755U
	10	755U

Table 7-4. A12 PCB Free-run-Mode Signatures – Address Space Test (Sheet 1 of 2)

Test Conditions: SERVICE-NORMAL switch is NORMAL.
Free-run jumper J9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP7), Trigger ⏷ (Button In)

STOP: Bit A15 (TP7), Trigger ⏶ (Button Out)

CLOCK: ALE (TP27), Trigger ⏷ (Button In)

GROUND: TP2 (Test Pod and Probe)

Vcc Signature: 755U

NOTES

1 Test probe flashes.
2 Signature may be unstable.
3 May have to press RESET on probe.

IC	PIN NO.	SIGNATURE
U1	1	755U
	2	755U
	3	755U
	4	0000
	5	0000
	6	755U[3]
	7	755U
	8	755U
U2	1	0000[1]
	2	0000[1]
	3	0000
	4	0000
	5	755U
	6	755U
	7	0000
	8	0000
	9	0000
	10	0000
	11	755U
	12	H335
	13	C113
	14	7050
	15	0772
	16	C4C3
	17	AA08
	18	7211
	19	A3C1
	20	0000
	21	7707
	22	577A
	23	HH86
	24	89F1
	25	AC99
	26	PCF3
	27	1180

IC	PIN NO.	SIGNATURE
U2	28	0000[1]
	29	755U
	30	755U
	31	755U
	32	755U[1]
	33	755U
	34	0000
	35	755U
	36	755U
	37	755U[1]
	38	0000
	39	0000
	40	755U
U3	1	0000
	2	H335
	3	H335
	4	C113
	5	C113
	6	7050
	7	7050
	8	0772
	9	0772
	10	0000
	11	755U[1]
	12	C4C3
	13	C4C3
	14	AA08
	15	AA08
	16	7211
	17	7211
	18	A3C1
	19	A3C1
	20	755U

IC	PIN NO.	SIGNATURE
U4	1	89F1
	2	AC99
	3	PCF3
	4	1180
	5	0000
	6	755U
	7	6F7P
	8	0000
	9	F615
	10	2F25
	11	8UH9
	12	340A
	13	P352
	14	U1U2
	15	4CP2
	16	755U
U5	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	4CP2
	19	HH86
	20	755U[1]
	21	755U
	22	577A
	23	7707
	24	755U

IC	PIN NO.	SIGNATURE
U6	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	U1U2
	19	HH86
	20	755U[1]
	21	755U
	22	577A
	23	7707
	24	755U
U7	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	P352
	19	HH86
	20	755U[1]
	21	755U
	22	577A
	23	7707
	24	755U

IC	PIN NO.	SIGNATURE
U8	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	18	340A
	19	HH86
	20	755U[1]
	21	755U
	22	577A
	23	7707
	24	755U
U9	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	12	0000
	19	HH86
	20	755U[1]
	21	755U
	22	577A
	23	7707
	24	755U

Table 7-4. A12 PCB Free-run-Mode Signatures – Address Space Test (Sheet 2 of 2)

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U15	1	0000	U16	1	A3C1	U18	1	0772	U19	1	H335
	2	755U		2	755U		2	C4C3		2	C113
	3	755U		3	0000[1]		3	AA08		3	7050
	4	0000		4	0000		4	7211		4	755U
	5	755U		5	755U		5	A3C1		5	755U
	6	0000		6	755U		6	0000		6	755U
	7	0000		7	0000		7	755U		7	755U
	8	755U		8	755U		8	0000		8	0000
	9	0000		9	755U		9	755U		9	755U
	10	755U		10	0000		10	755U		10	755U
	11	0000		11	0000		11	755U			
	12	0000[1]		12	755U		12	755U			
	13	755U[1]		13	755U		13	755U			
	14	755U		14	755U		14	755U			
							15	755U			
							16	755U			

Table 7-5. A12 PCB Output-Port-Enable Lines Test

Purpose: This test checks whether the output ports, located on individual A1 thru A5 PCBs, are being enabled. The signatures are read on A14P3. Each P3 pin shows the corresponding A12 PCB IC and pin number.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode. Free-run jumper J9 installed.

Signature Analyzer Setup:

START: HMBA (TP24), Trigger _/‾ (Button Out)

STOP: SOD (TP5), Trigger _/‾ (Button Out)

CLOCK: $\overline{WR}$ (U2, pin 31), Trigger _/‾ (Button Out)

GROUND: TP2 (Test Pod and Probe)

Vcc Signature: C6HU

PIN	MNE-MONIC	A12 IC & PIN	SIGNATURE	PIN	MNE-MONIC	A12 IC & PIN	SIGNATURE
1	SP13	U20-10	P946	14	SP14	U20-9	7326
2	SP11	U20-12	2U87	15	SP12	U20-11	4U4A
3	SP9	U20-14	PPFU	16	SP10	U20-13	235P
4	SP5	U21-10	4659	17	SP15	U20-7	7A80
5	SP8	U20-15	37HO	18	SP7	U21-7	A62U
6	SP6	U21-9	C9H7	19	SP4	U21-4	CPC4
7	SP3	U21-12	3069	20	SP2	U21-13	HHC2
8	SP1	U21-14	0004	21	SP0	U21-15	HC6U
9	B0	TP15	C6HU	22	B1	TP16	3227
10	B2	TP17	3227	23	B3	TP18	3227
11	B4	TP19	3227	24	B5	TP20	3227
12	B6	TP21	3227	25	B7	TP22	3227
13	GND	TP2	0000	26	+5V	TP1	C6HU

Table 7-6. Service Mode Signature Analysis of A12U25

Purpose: This table provides a means of testing the 8279 Keyboard/Display Interface IC. This IC can be tested in a limited fashion by verifying that the signatures at selected A12 data-bus test points (TP15-22) change when certain front panel pushbuttons are pressed.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper J9 installed.

Signature Analyzer Setup:

START: ROM 5 line (TP9), Trigger ⟋ (Button Out).

STOP: SOD (TP5), Trigger ⟋ (Button Out).

CLOCK: $\overline{RD}$ (U2, Pin 32), Trigger ⟋ (Button Out).

GND: A12TP2 (Test pod and probe)

Vcc Signature: 9FUF

NOTE

- The A2 Ramp Generator PCB causes unstable signatures. Remove this PCB before making a signature analysis of the 8279.
- The 555 Timer circuit (A12U27, U28) causes the the signatures on data-bus bit D1 (Figure 7-15) to be unstable. Disable U27 by grounding its threshold input, pin 6.

Procedure: When activated, each of the front panel pushbuttons causes a unique keycode to be sent over the data bus (Table 7-7). This keycode can be used to verify operation of the 8279, as follows:

1. Set up the Signature Analyzer as shown above.
2. Select a testpoint for monitoring that has a binary weight (8, 4, 2, 1) large enough to provide a stable signature (such as TP18, 19, or 20).
3. Read the signature at the testpoint and verify it is stable.
4. While monitoring this stable signature, press a pushbutton that will cause the logic state of the monitored data-bus line to change, see the test points at the bottom of Table 7-7.
5. Verify that the signature either changed or became unstable when the selected pushbutton was pressed. For example: Monitor TP20 and, after ensuring a stable signature, alternately press CW F1 and ΔF F1. The signature should be unstable during operation of the two pushbuttons.

Table 7-7. Front Panel Keycode Chart

FRONT PANEL PUSHBUTTON	Decimal	FRONT PANEL KEYCODE (Binary)							
		MS Byte				LS Byte			
		8	4	2	1	8	4	2	1
0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	1
2	2	0	0	0	0	0	0	1	0
3	3	0	0	0	0	0	0	1	1
4	4	0	0	0	0	0	1	0	0
5	5	0	0	0	0	0	1	0	1
6	6	0	0	0	0	0	1	1	0
7	7	0	0	0	0	0	1	1	1
8	8	0	0	0	0	1	0	0	0
9	9	0	0	0	0	1	0	0	1
Decimal Point (.)	10	0	0	0	0	1	0	1	0
Minus Sign (-)	11	0	0	0	0	1	0	1	1
F1	12	0	0	0	0	1	1	0	0
F0	13	0	0	0	0	1	1	0	1
M1	14	0	0	0	0	1	1	1	0
F2	15	0	0	0	0	1	1	1	1
ΔF	16	0	0	0	1	0	0	0	0
M2	17	0	0	0	1	0	0	0	1
LEVEL	18	0	0	0	1	0	0	1	0
SWEEP TIME	19	0	0	0	1	0	0	1	1
	20	0	0	0	1	0	1	0	0
	21	0	0	0	1	0	1	0	1
GHz/dBm/Sec	22	0	0	0	1	0	1	1	0
MHz/dB/mS	23	0	0	0	1	0	1	1	1
CLEAR ENTRY	24	0	0	0	1	1	0	0	0
SHIFT	25	0	0	0	1	1	0	0	1
	26	0	0	0	1	1	0	1	0
F1-F2	27	0	0	0	1	1	0	1	1
M1-M2	28	0	0	0	1	1	1	0	0
FULL	29	0	0	0	1	1	1	0	1
ΔF F0	30	0	0	0	1	1	1	1	0
ΔF F1	31	0	0	0	1	1	1	1	1
CW F1	32	0	0	1	0	0	0	0	0
CW F0	33	0	0	1	0	0	0	0	1
CW M1	34	0	0	1	0	0	0	1	0
CW F2	35	0	0	1	0	0	0	1	1
CW M2	36	0	0	1	0	0	1	0	0
INCREASE (F. Ver.)	37	0	0	1	0	0	1	0	1
DECREASE (F. Ver.)	38	0	0	1	0	0	1	1	0
OFF (F. Ver.)	39	0	0	1	0	0	1	1	1
	40	0	0	1	0	1	0	0	0
STEP SWEEP (GPIB)	41	0	0	1	0	1	0	0	1
MANUAL SWEEP	42	0	0	1	0	1	0	1	0
AUTO TRIGGER	43	0	0	1	0	1	0	1	1
LINE TRIGGER	44	0	0	1	0	1	1	0	0
EXT OR SINGLE SWEEP	45	0	0	1	0	1	1	0	1
VIDEO MARKER	46	0	0	1	0	1	1	1	0
RF MARKER	47	0	0	1	0	1	1	1	1
INTENSITY MARKER	48	0	0	1	1	0	0	0	0
INTERNAL LEVELING	49	0	0	1	1	0	0	0	1
POWER METER LEVELING	50	0	0	1	1	0	0	1	0
DETECTOR LEVELING	51	0	0	1	1	0	0	1	1
RF ON	52	0	0	1	1	0	1	0	0
RETRACE RF - ON	53	0	0	1	1	0	1	0	1
SELF TEST	54	0	0	1	1	0	1	1	0
RETURN TO LOCAL	55	0	0	1	1	0	1	1	1
FM AND PHASELOCK	56	0	0	1	1	1	0	0	0
DATA BUS TEST POINTS		TP 22	TP 21	TP 20	TP 19	TP 18	TP 17	TP 16	TP 15

7-7 A11 FRONT PANEL PCB

7-7.1 A11 Front Panel PCB, Circuit Description

The A11 Front Panel PCB is the mounting plane for the front panel pushbuttons, indicators, and numeric displays. A block diagram of the A11 PCB circuitry is shown in Figure 7-19. A parts locator diagram is provided in Figure 7-20. A diagram of the front panel, showing switch and LED numbering, is provided in Figure 7-21. And the A11 PCB schematic (2 sheets) is provided in Figure 7-22.

The A11 PCB (Figure 7-19) is functionally divided into three circuits: display, switch, and LED. The display circuitry consists of the 3-to-16 Decoder (U11), the Current Source circuit (Q1-Q15), the Numeric Display digits (DS48-DS62), and the Current Sink circuit (U8, U10). The inputs to the display circuitry are scan data via the **SL0-SL3&LCAD Bus** and display-segment data via the **NA0-NA3/NB0-NB3 Bus;** both buses are from the 8279 Keyboard/Display Interface integrated circuit (A12U25). The scan data, when decoded, causes the display digits to be scanned; the segment data causes the selected segment to be lit.

The switch circuitry is divided into two groups of switches. The main switch group consists of the 3-to-8 Decoder (U7) and the 8x8 Switch Matrix (S1-S19, S22-S25, S27-S39, S42-S56, S58). The inputs to this switch circuit are the **SL0-SL3** scan bus lines from A12U25. These lines, after being decoded, sequentially scan the 8 rows of switch-matrix switches; key status is sent back to A12U25 via the 8-bit **COL1-COL8 Bus.**

The second group of switches consists of:

- SELF TEST, which causes a microprocessor interrupt when momentarily depressed, and
- F0, M1, M2, and FREQUENCY VERNIER-INCREASE and -DECREASE, which communicate information when held depressed (paragraphs 3-2.4 and 3-2.2c respectively).

These switches have two sets of contacts – the ones shown here and another set located in the switch matrix.

The LED circuitry consists of three groups of LEDs: GPIB LEDs, LEDs that flash, and LEDs that light steadily. The GPIB LEDs are the REMOTE, LOCAL LOCKOUT, TALK, LISTEN, and SRQ indicators. The flashing LEDs are the UNLEVELED, RF OFF, SWEEPING, and EXTERNAL ALC GAIN CAL (ALC CAL) indicators. Both the GPIB and the flashing LEDs are directly controlled by lines from the A12 PCB. Except for those LEDs mentioned, all of the other front panel LEDs are non-flashing types. These non-flashing LEDs are controlled by the microprocessor via the LED Latches (U1-U6). Latches U1 thru U6 are respectively clocked by select-port lines **SP16-SP21**.

7-7.2 A11 Front Panel PCB, Troubleshooting Information

There is no error code for the A11 Front Panel PCB. Malfunctions occurring on this PCB should be observable from the front panel. Use the circuit description in paragraph 7-7.1 and the block diagram in Figure 7-19 to aid in troubleshooting the A11 PCB.

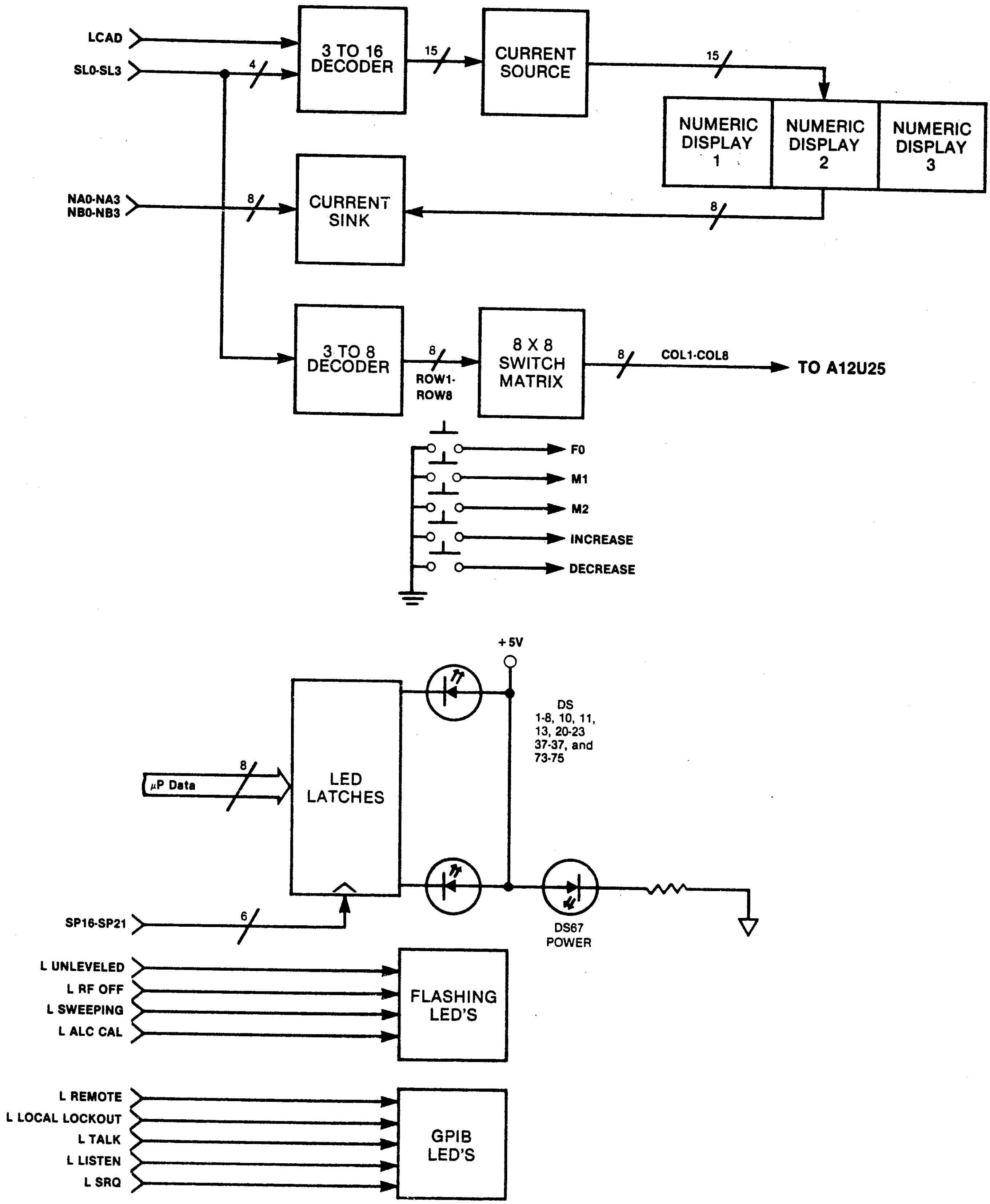
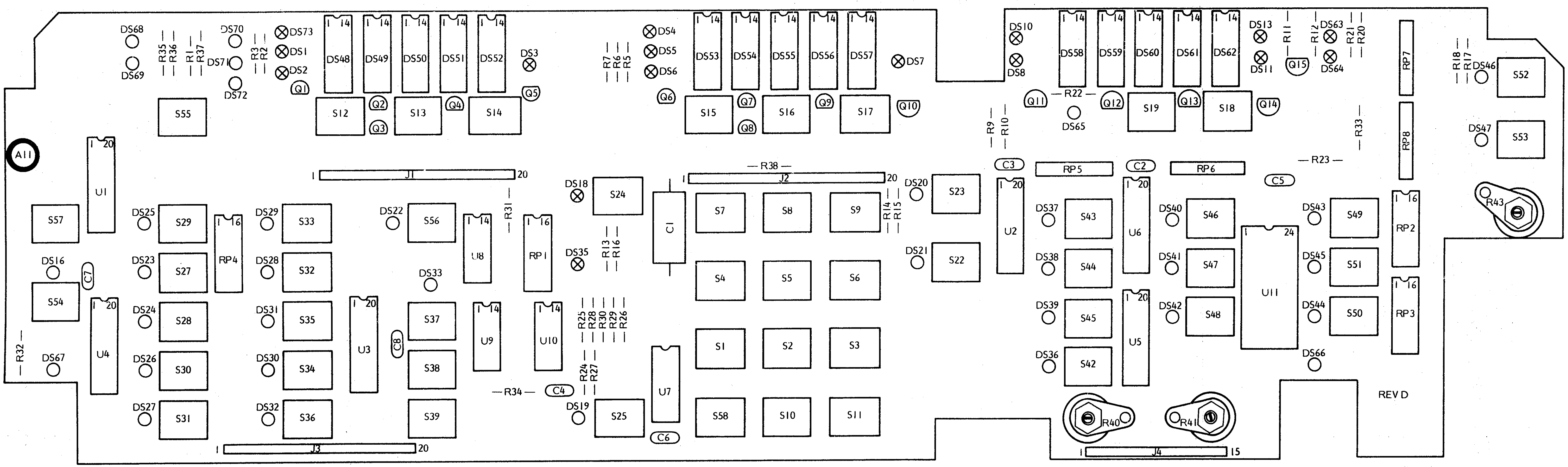


Figure 7-19. A11 Front Panel PCB, Block Diagram



NOTES:

○ DENOTES YELLOW LED

⊗ DENOTES RED LED

Figue 7-20. A11 Front Panel PCB Parts Locator Diagram

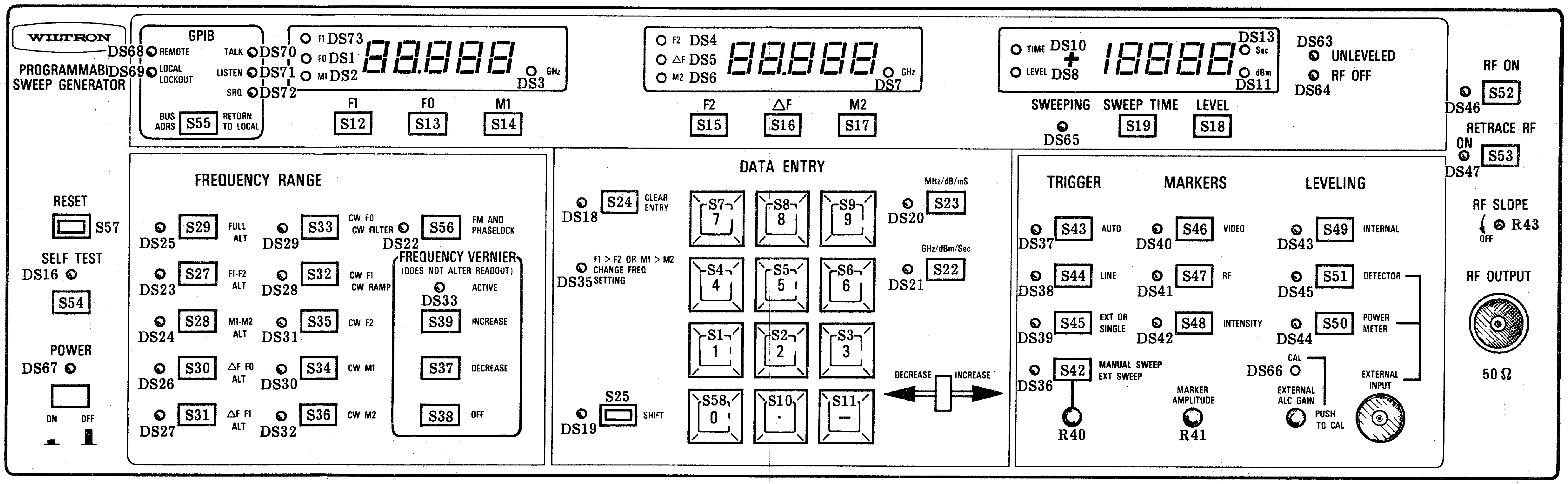


Figure 7-21. 6600A Series Front Panel, Showing Reference Designators for LEDs, Displays, Switches, and Controls

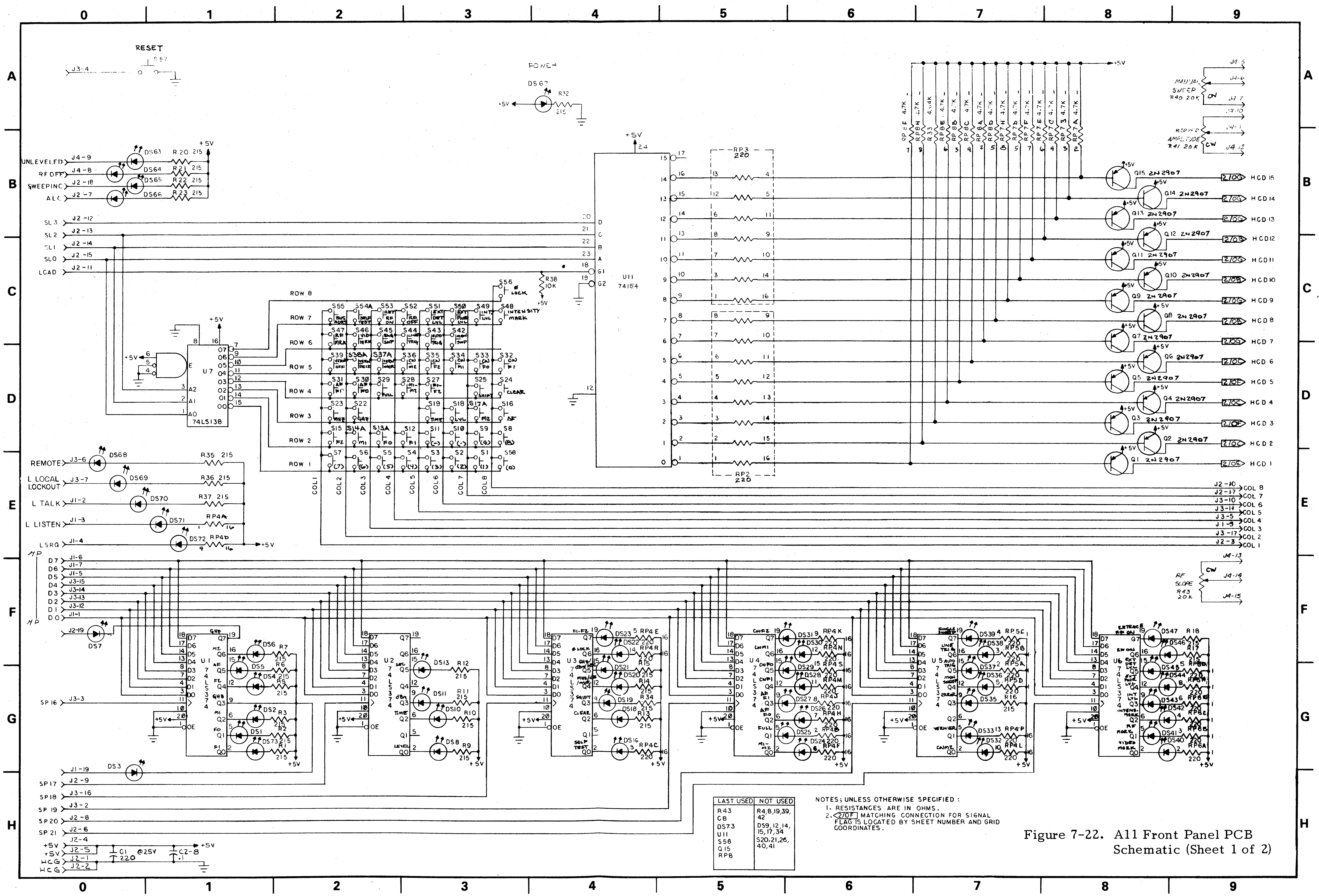


Figure 7-22. A11 Front Panel PCB Schematic (Sheet 1 of 2)

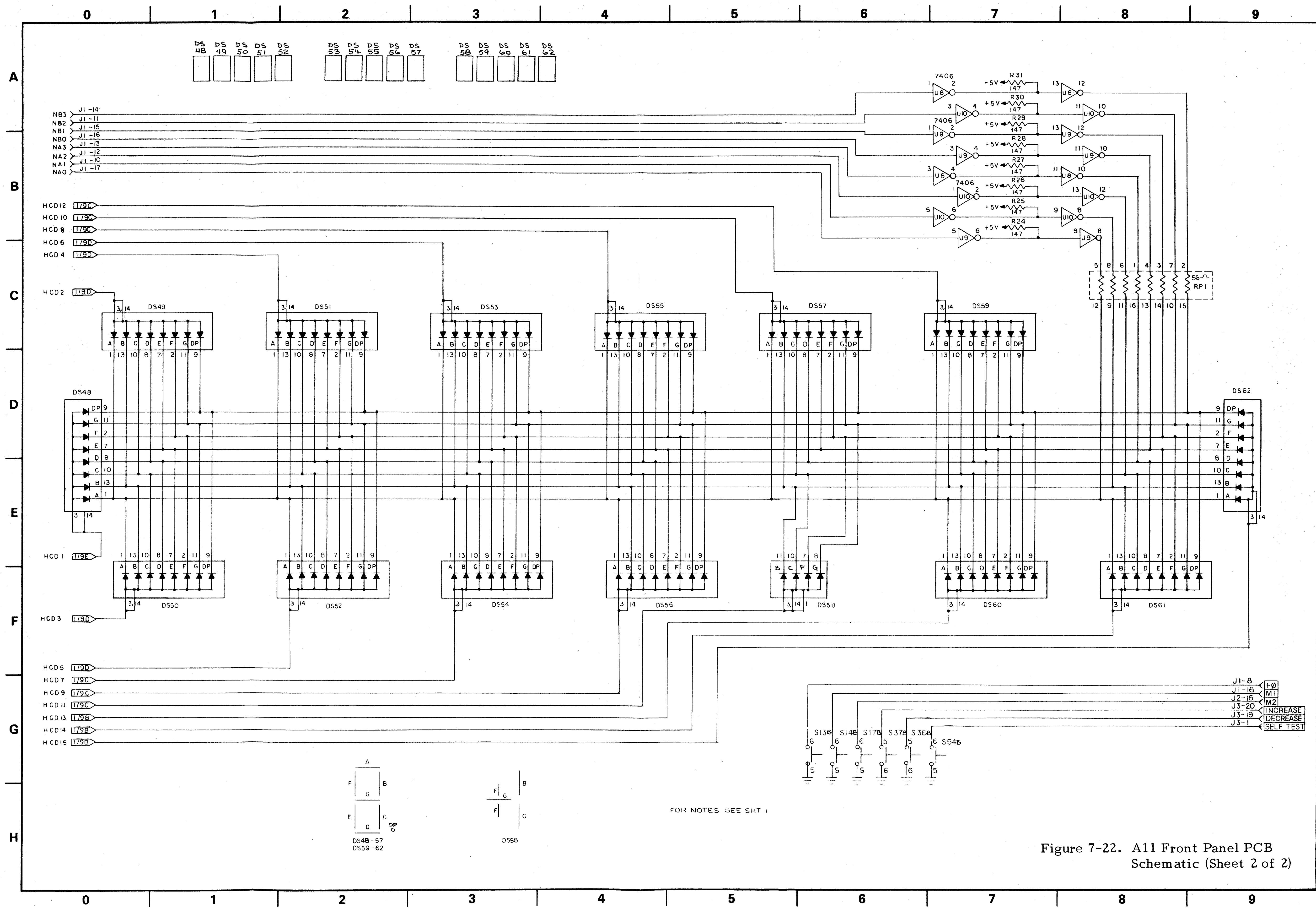


Figure 7-22. A11 Front Panel PCB Schematic (Sheet 2 of 2)

7-8 A1 GPIB INTERFACE PCB

7-8.1 A1 GPIB Interface PCB, Circuit Description

The A1 PCB provides the interface between the sweep generator and the IEEE-488 GPIB. The A1 PCB is microprocessor-controlled, and contains an on-board 8085 Microproc-essor IC and an 8291 GPIB Interface IC. The 8085 provides (1) control for the 8291 and other on-board circuits, and (2) communications between the A1 PCB and the A12 Microproc-essor PCB. The 8291 provides communica-tions between the sweep generator and the GPIB. Its capabilities include the following:

- Data transfer
- Handshake protocol
- Talker/listener addressing procedures
- Device clearing and triggering
- Service request (SRQ) control
- Serial and parallel-poll servicing

A functional block diagram of the A1 PCB is shown in Figure 7-23, the power-up opera-tional program flowchart is shown in Figure 7-24, and the schematic (3 sheets) is con-tained in Figure 7-25.

As shown in Figure 7-23, the A1 PCB is composed of the following major circuits:

a. 6600 Analog Interface Circuits. These circuits provide the interface between the analog circuits in the sweep generator that can cause an SRQ (service request) and the GPIB microprocessor. The Analog Interface circuits are composed of the following ICs: U10C, U23A, U23B, U25D, U10A, U25A, U25B, U25C, U20B, U20A, U10D, and U16 (Figure 7-25, Sheet 2).

b. GPIB Address Switches Input Port. This circuit is the A1 PCB microprocessor in-put port for the rear panel GPIB address and data delimiter (CR/CR-LF) switches. The circuit is composed of U15 and its associated resistors (Figure 7-25, Sheet 2).

c. LED Drivers. These circuits drive the REMOTE, LOCAL LOCKOUT, TALK, LISTEN, and SRQ front panel GPIB LED indicators. The circuits are composed of the following components: Q1, U11D, U14A, U14B (Figure 7-25, Sheet 2), U13A, and U13B (Figure 7-25, Sheet 1).

d. 6600 µP Interface. These circuits provide interface between the A1 PCB circuits and the A12 Microprocessor PCB. The circuits are composed of the following ICs: U21A, U21B, U22, and U24 (Figure 7-25, Sheet 2).

e. ROM 2716. The ROM (read-only memory) contains the A1 PCB operational program that is flowcharted in Figure 7-24. Read-only memory consists of U4 and U5 (Fig-ure 7-25, Sheet 1).

f. RAM 2111. The RAM (random-access memory) is the "scratchpad memory" for temporarily storing the received GPIB commands. Random-access memory con-sists of U2 and U3 (Figure 7-25, Sheet 1).

g. Free-Run Circuit. This circuit consists of the 18-pin jumper DIP socket U9 and its associated gates and resistors. Socket U9 is used for testing purposes – the removal of U9 causes a no-operation ("NOP") in-struction to be forced into the micro-processor, causing it to free-run.

h. Address Decoder. This circuit decodes the microprocessor address bus. The out-puts from this circuit are (1) active-low CE (chip enable) lines for the RAM, ROM, 8255, and 8291 ICs and (2) enable inputs for the U13A and U13B TALK and LISTEN indicator drivers.

i. Option Interface 8255. This circuit, con-sisting of the 8255 Microprocessor Inter-face IC (U1), is used with the Option 14 AUX I/O DATA connector.

j. Microprocessor 8085 and GPIB Interface IC 8291. These two circuits are described in the opening paragraph under the A1 PCB Circuit Description heading.

k. SERVICE-NORMAL Switch (S1). In the SERVICE position, S1 interrupts the mi-croprocessor and causes it to run a stimu-lus routine for signature-analysis testing.

When the front panel POWER switch is depressed and ac power is turned on, the A1 PCB goes into the flowcharted routine of Figure 7-24. The A1 PCB remains in this looping routine until the ac power is turned off.

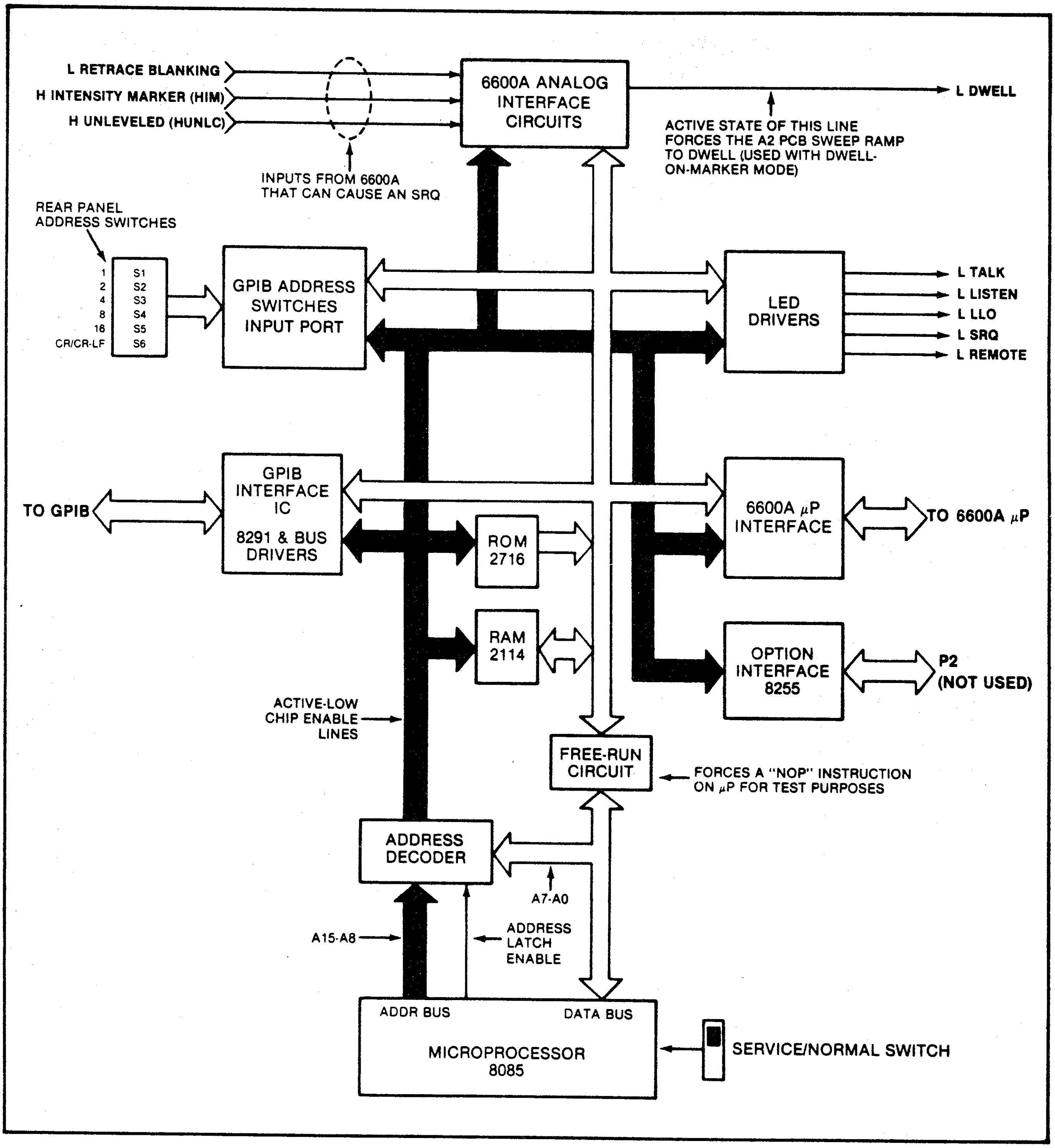


Figure 7-23. A1 GPIB Interface PCB, Overall Block Diagram

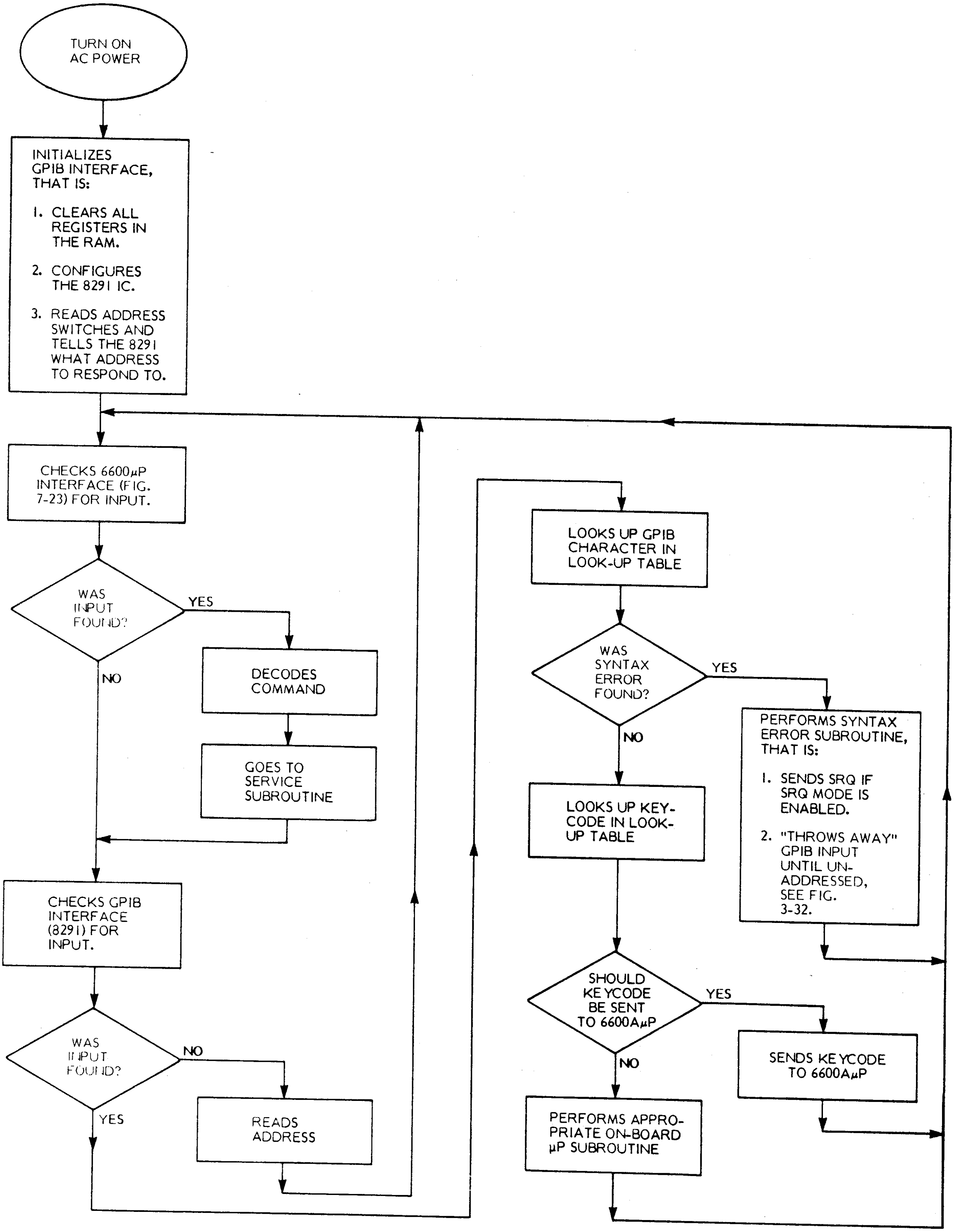
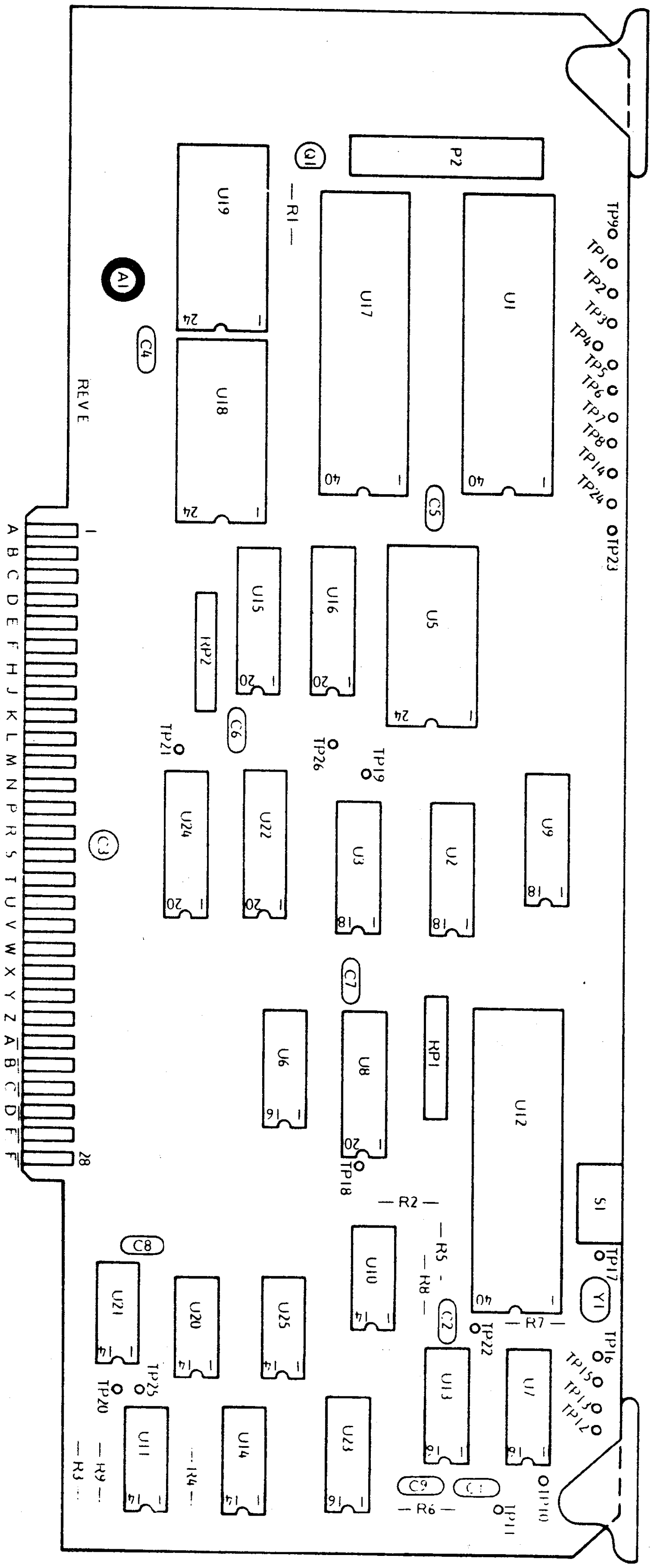


Figure 7-24. A1 PCB, AC Power-On Operational Flowchart



A1 GPIB Interface PCB Parts Locator Diagram

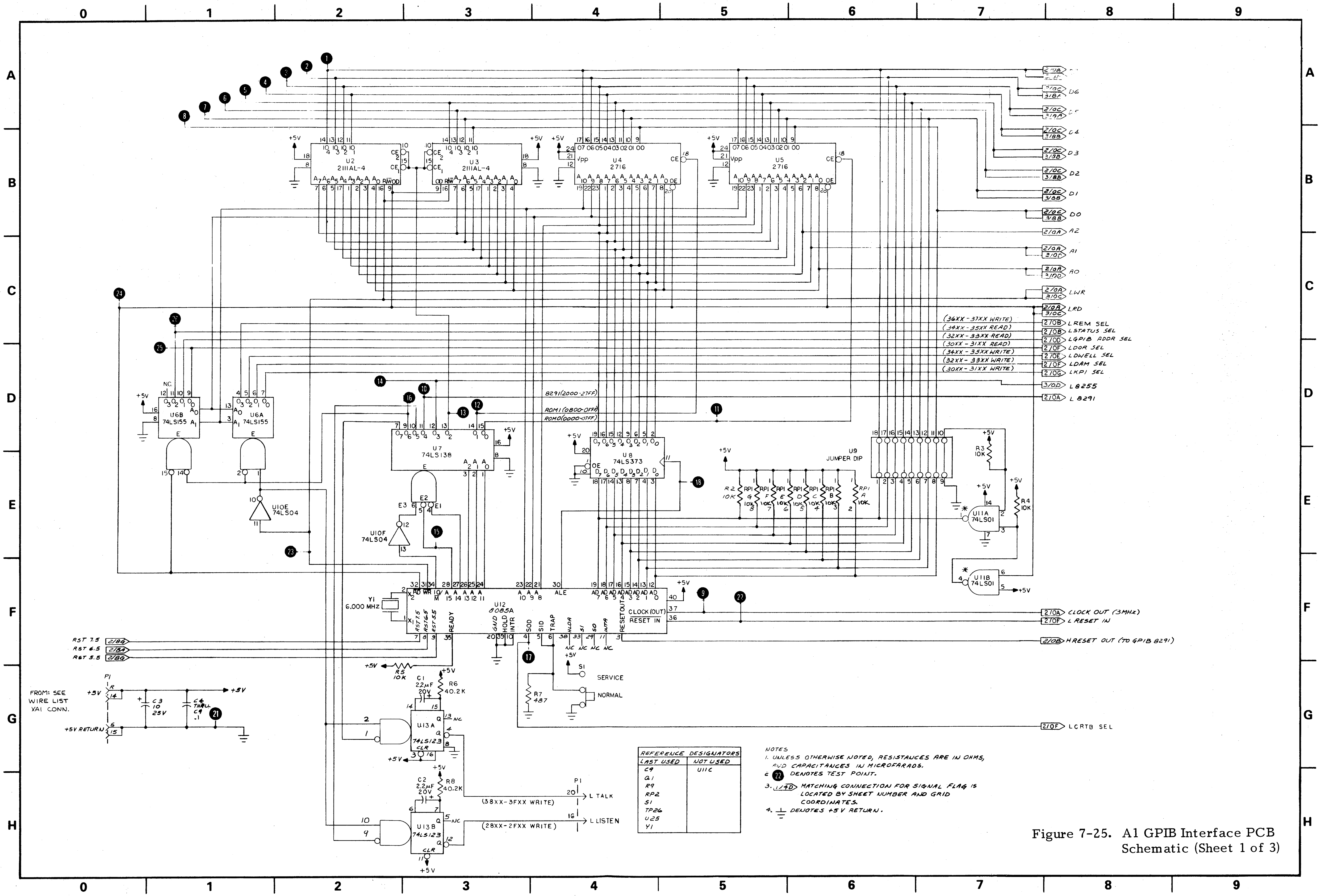


Figure 7-25. A1 GPIB Interface PCB Schematic (Sheet 1 of 3)

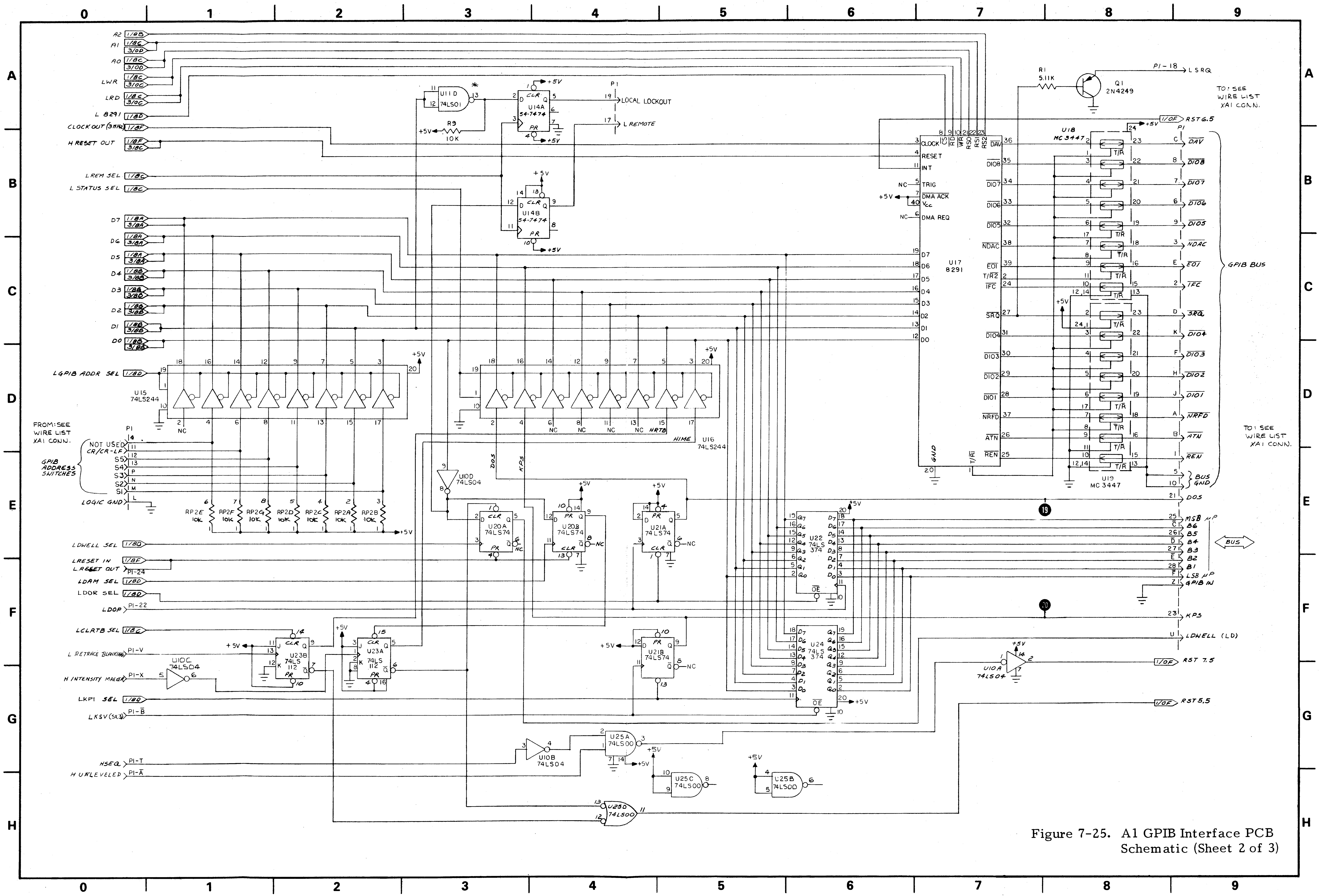
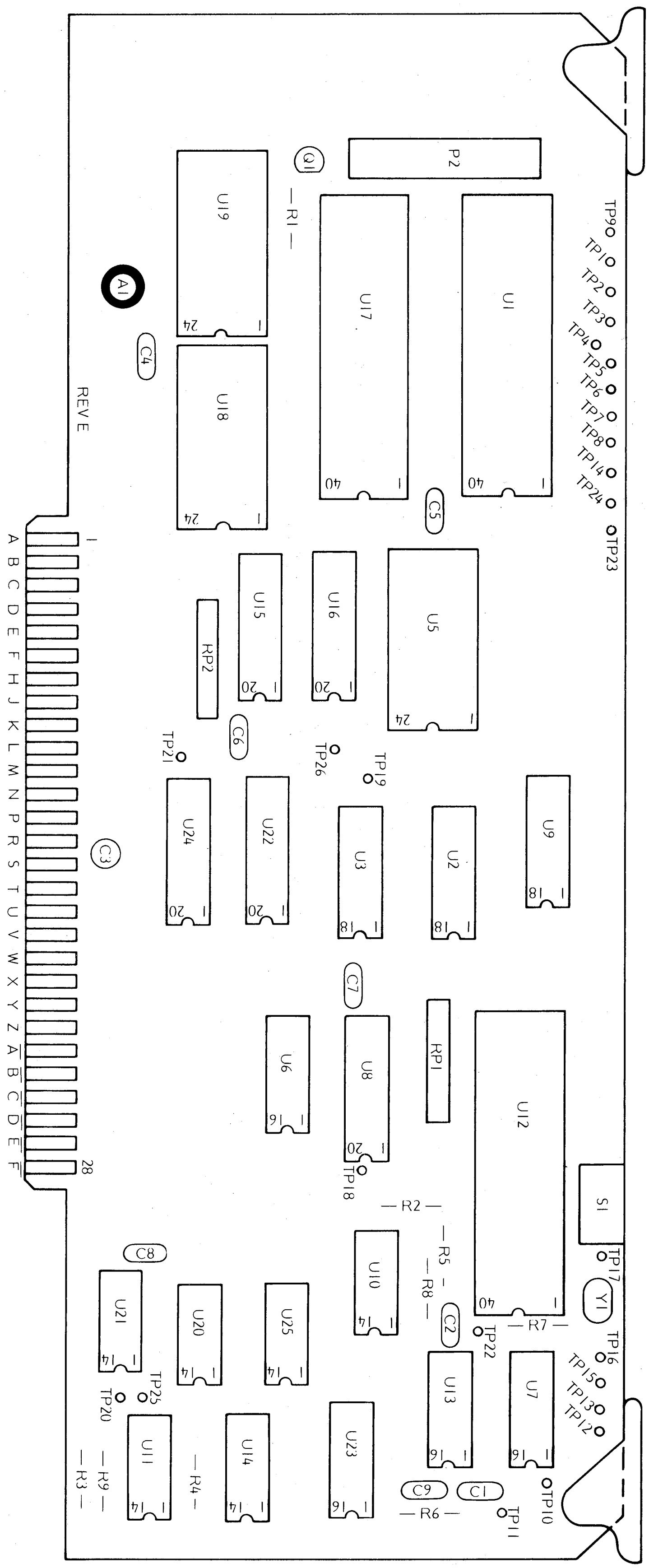


Figure 7-25. A1 GPIB Interface PCB Schematic (Sheet 2 of 3)



A1 PCB Parts Locator Diagram

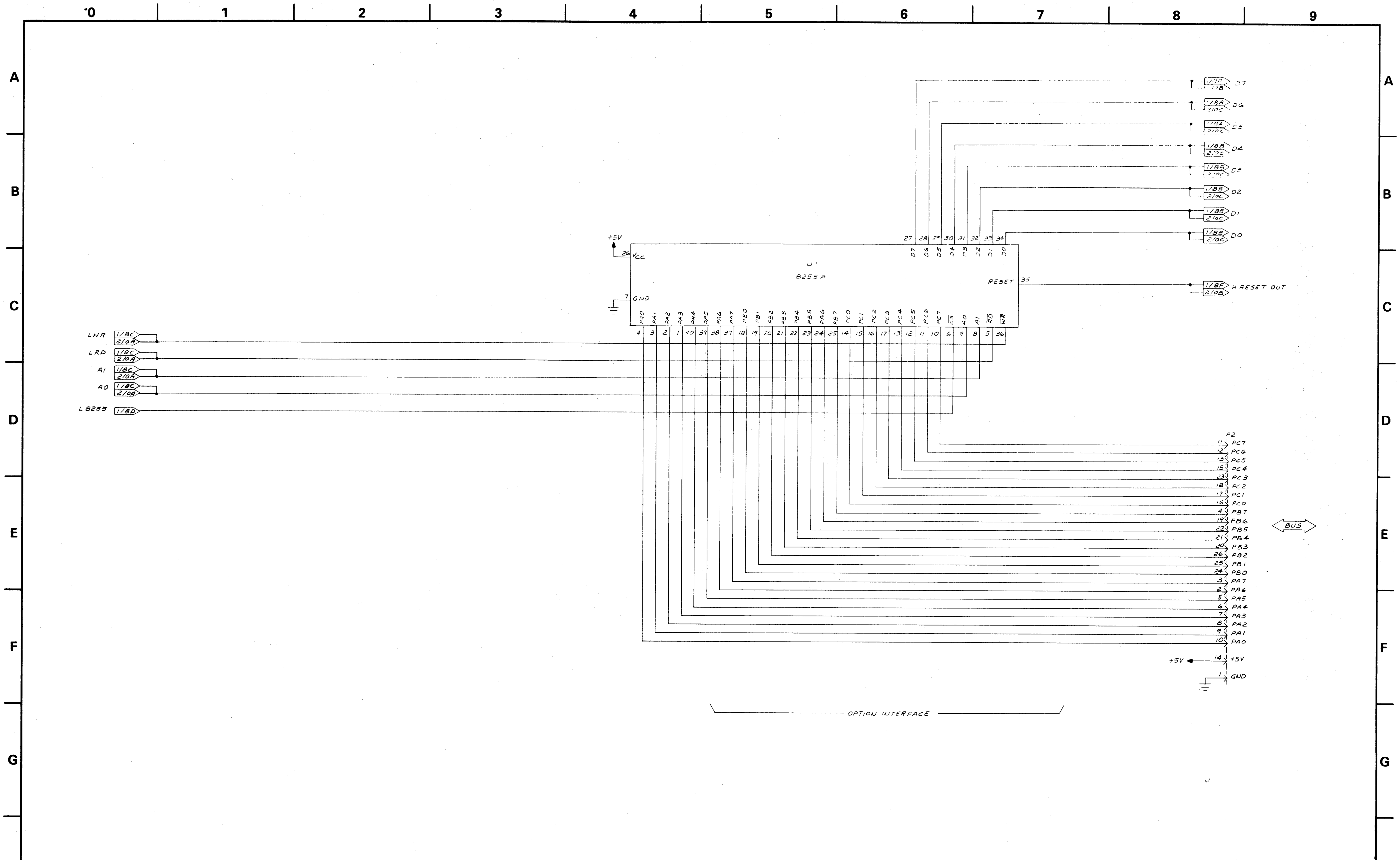


Figure 7-25. A1 GPIB Interface PCB Schematic (Sheet 3 of 3)

:or Diagram

parts locator

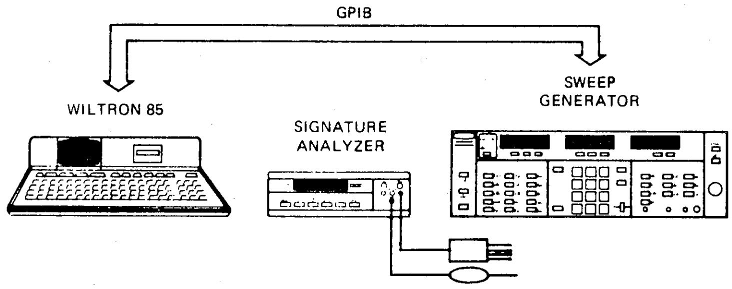


Figure 7-26. Test Equipment Setup for Troubleshooting Error Code 24

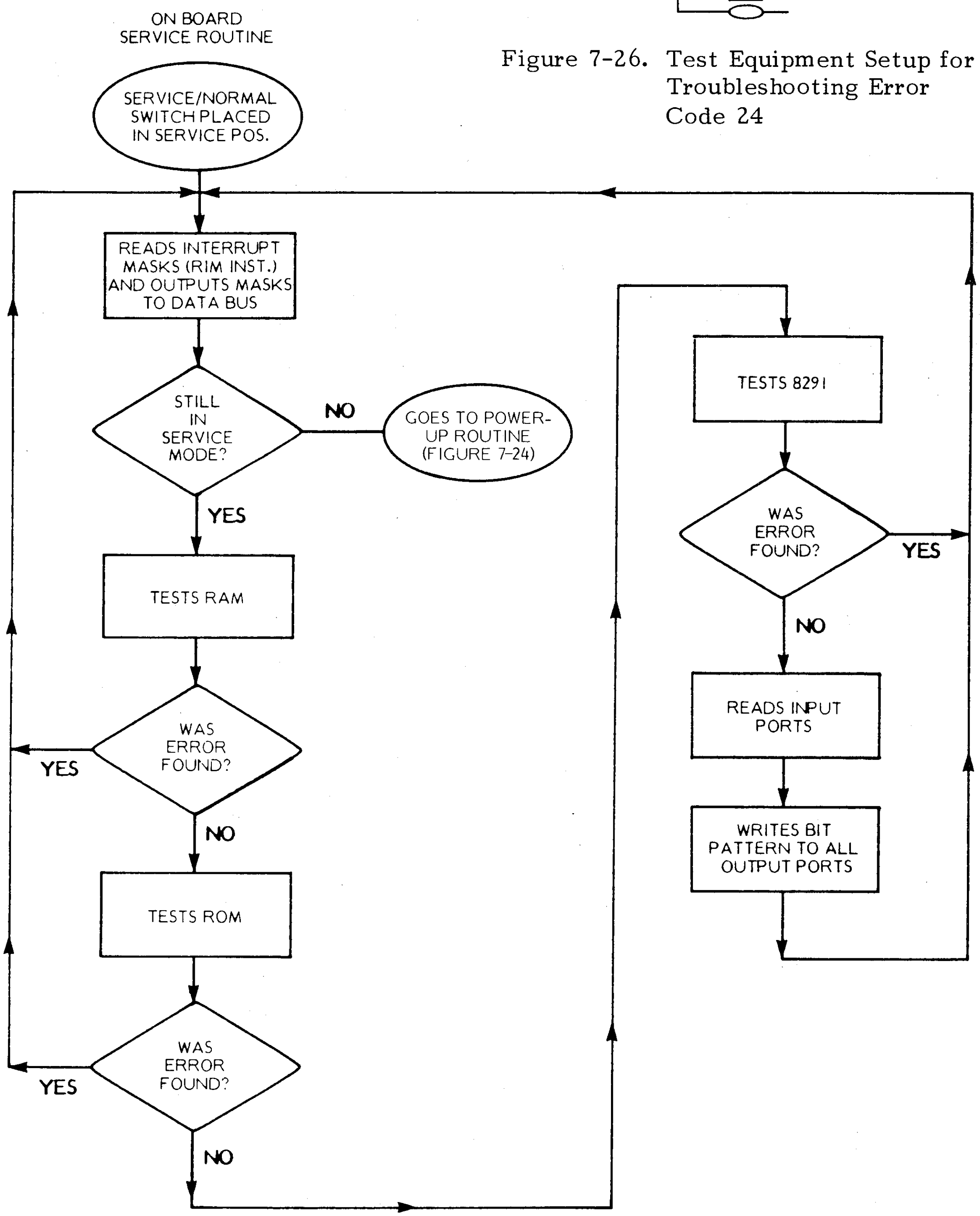
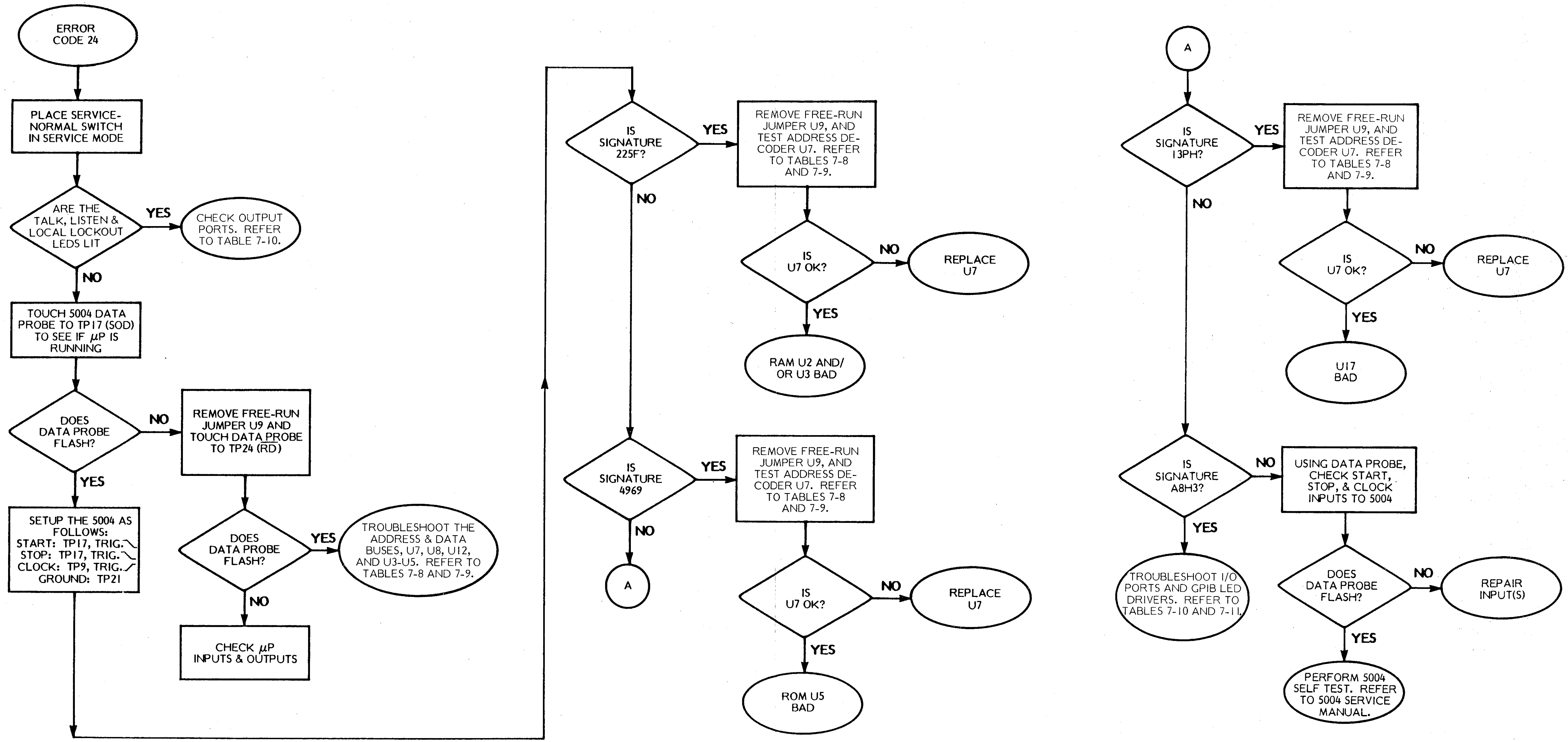


Figure 7-27. A1 PCB On-Board Service Routine



ard Service

Figure 7-28. Error Code 24 Troubleshooting Flowhcart

Figures 7-26 & 7-27

7-8.2 A1 GPIB Interface PCB, Troubleshooting Information and Data

Error Code 24 reports on the status of the A1 GPIB Interface PCB. The microprocessor routine associated with this error code initiates a subroutine (Figure 7-29) that tests the A1 RAM, ROM, and 8291 circuits. The test equipment setup for troubleshooting Error Code 24 is provided in Figure 7-26 (facing page); the troubleshooting flowchart is provided in Figure 7-28.

Signature analysis is the recommended method for troubleshooting A1 circuits. In addition to a free-run mode (explained in HP Application Note 222-2), the A1 PCB also has a service mode. In this mode, routines stored in ROM U5 provide two methods for isolating to faulty components.

The first method uses a "loop-on-fail" technique (Figure 7-27) that allows the signature analyzer to quickly isolate a malfunctioning RAM, ROM, or 8291 GPIB Interface IC circuit. In this method, the signature analyzer will display one of four characteristic (Vcc) signatures, depending on which loop is being executed. If no faults are found, a specific signature is displayed. A fault in either the RAM, ROM, or 8291 provides a signature that is different for each.

The second service-mode method, a routine which writes to the output ports, input ports, and retrace-blanking flip flop, provides for signature analysis of these components. These tests are contained in Tables 7-10 thru 7-12 respectively.

For free-run signature analysis, two tables of signatures are provided. Tables 7-8 and 7-9 respectively provide signatures for the microprocessor's read and write spaces. Both of these tables provide test and signature analyzer setup conditions. When these conditions are met, a characteristic (Vcc) signature will be displayed; the microprocessor circuit may then be accurately tested.

In addition to signatures, the 5004A Signature Analyzer data probe may be used like a logic probe. When a circuit node is touched, the

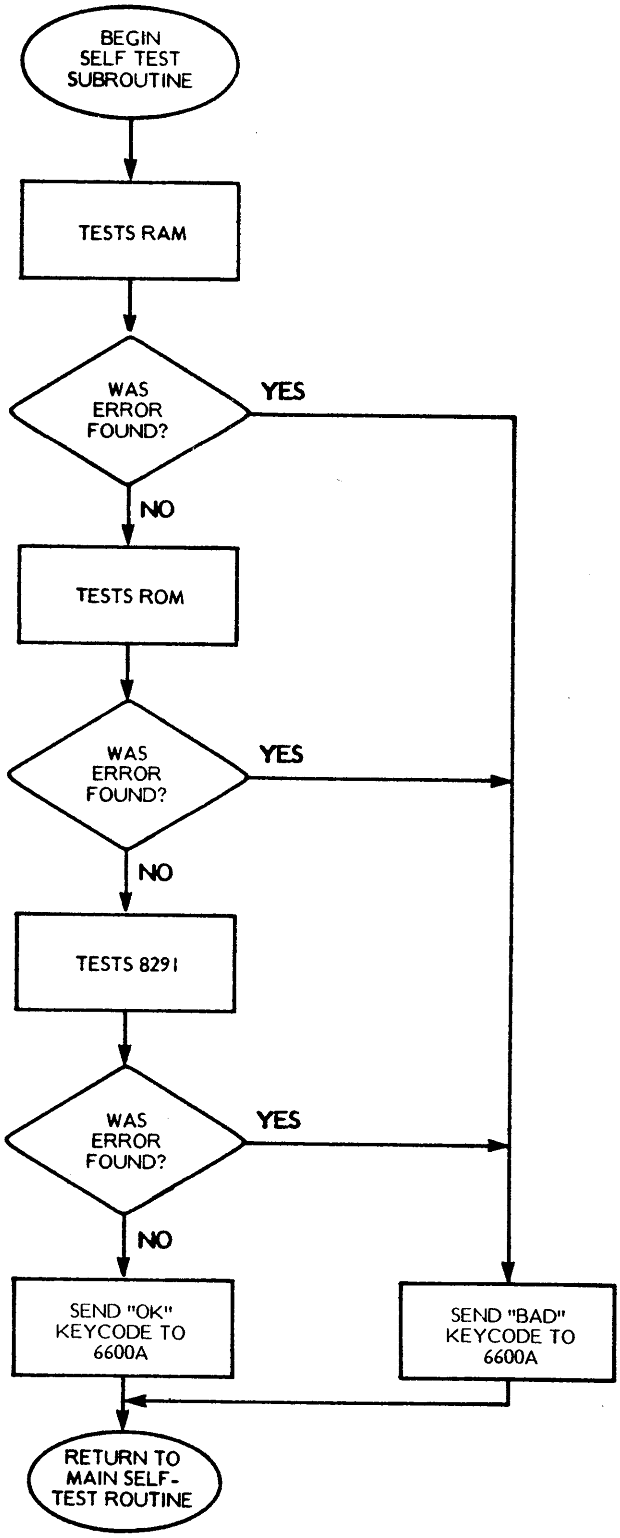


Figure 7-29. A1 PCB Self-Test Subroutine

probe tip will either flash, light steadily, or not be lit. A steadily-lit probe indicates a logic 1 or Vcc. An unlit probe indicates a logic 0 or ground. And a flashing probe usually indicates pulses; however, it can also indicate noise. A noise indication sometimes occurs when the probe is touched to an open node, or when it is touched to a tri-state-buffer node where the buffer is in its off state. When testing such nodes, the 5004A will read the Vcc signature when its RESET button is pressed. To help minimize probe noise pickup, ground the probe at the same point the test pod is grounded.

Table 7-8. A1 PCB Free-Run Mode Signatures – Read Space Test

Test Conditions: SERVICE-NORMAL switch in NORMAL.
Free-run jumper U9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP15), Trigger ↘ (Button In)

STOP: Bit A15 (TP15), Trigger ↘ (Button Out)

CLOCK: $\overline{RD}$ (TP24), Trigger ↗ (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: 755U

NOTES

[1] Test probe flashes.
[2] Signature may be unstable.
[3] May have to press RESET on probe.

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U2	1	0772	U5	19	HH86	U8	1	0000		20	0000		10	0000
	2	7050		20	0000[1]		2	H335		21	7707		11	755U
	3	C113		21	755U		3	755U[1]		22	577A		13	755U
	4	H335		22	577A		4	755U[1]		23	HH86		15	0000
	5	AA08		23	7707		5	C113		24	89F1		17	0000
	6	7211		24	755U		6	7050		25	AC99		19	9181
	7	A3C1					7	755U[1]		26	PCF3		20	755U
	8	0000	U6	1	0000		8	755U[1]		27	1180			
	9	0000		2	F615		9	0772		28	0000[1]	U17	1	755U
	10	P352		3	HH86		10	0000		29	755U		2	755U
	15	P352		4	755U		11	0000[1]		30	0000[1]		3	755U[1]
	16	755U		5	755U		12	C4C3		31	755U		4	0000
	17	C4C3		6	755U		13	755U[1]		32	0000[1]		5	0000
	18	755U		7	755U		14	755U[1]		33	755U		6	755U
				8	755U		15	AA08		34	0000		7	755U
U3	1	0772		9	2HU0		16	7211		35	755U		8	8UH9
	2	7050		10	CF3F		17	755U[1]		36	755U		9	0000[1]
	3	C113		11	9181		18	0000[1]		37	755U[1]		10	755U
	4	H335		12	C307		19	A3C1		38	0000		11	0000[1]
	5	AA08		13	577A		20	755U		39	0000		20	0000
	6	7211		14	F615					40	755U		21	H335[2]
	7	A3C1		15	0000[1]	U12	1	755U[1]					22	C113[2]
	8	0000		16	755U		2	0000[1]	U15	1	CF3F		23	7050
	9	0000					3	0000		2	755U[1]		24	755U
	10	P352	U7	1	89F1		4	755U		4	755U		25	755U
	15	P352		2	AC99		5	0000		6	755U		26	755U
	16	755U		3	PCF3		6	0000		8	755U		27	0000
	17	C4C3		4	1180		7	0000		10	0000		28	0000
	18	755U		5	0000[1]		8	0000		11	755U		29	0000
				6	755U		9	0000		13	755U		30	0000
U5	1	A3C1		7	6F7P		10	0000		15	755U		31	755U
	2	7211		8	0000		11	755U		17	755U		32	755U
	3	AA08		9	F615		12	755U[1]		19	CF3F		33	0000
	4	C4C3		10	2F25		13	755U[1]		20	755U		34	0000
	5	0772		11	8UH9		14	755U[1]					35	755U
	6	7050		12	340A		15	755U[1]	U16	1	9181		36	755U
	7	C113		13	P352		16	755U[1]		2	0000		37	755U
	8	H335		14	U1U2		17	755U[1]		4	755U		38	755U
	12	0000		15	4CP2		18	755U[1]		6	755U[3]		39	755U
	18	4CP2		16	755U		19	0000[1]		8	755U[1]		40	755U

Table 7-9. A1 PCB Free-Run Mode Signatures – Address Space Test

Test Conditions: SERVICE-NORMAL switch in NORMAL.
Free-run jumper U9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP15), Trigger ⎺\⎽ (Button In)

STOP: Bit A15 (TP15), Trigger ⎽/⎺ (Button Out)

CLOCK: ALE (TP18), Trigger ⎺\⎽ (Button In)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: 755U

NOTES

[1] Test probe flashes.
[2] Signature may be unstable.
[3] May have to press RESET on probe.

IC	PIN NO.	SIGNATURE
U2	1	0772
	2	7050
	3	C113
	4	H335
	5	AA08
	6	7211
	7	A3C1
	8	0000
	9	755U[1]
	10	P352
	11	755U[2]
	12	755U[2]
	13	755U[2]
	14	Unstable
	15	P352
	16	755U
	17	C4C3
	18	755U
U3	1	0772
	2	7050
	3	C113
	4	H335
	5	AA08
	6	7211
	7	A3C1
	8	0000
	9	755U[1]
	10	P352
	11	755U[2]
	12	755U[2]
	13	755U[2]
	14	Unstable
	15	P352
	16	755U
	17	C4C3
	18	755U
U5	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113
	8	H335
	9	755U[1]
	10	755U[1]
	11	755U[1]

IC	PIN NO.	SIGNATURE
U5	12	0000
	13	755U[2]
	14	755U[2]
	15	755U[2]
	16	Unstable
	17	Unstable
	18	4CP2
	19	HH86
	20	755U[1]
	21	755U
	22	577A
	23	7707
	24	755U
U6	1	0000
	2	F615
	3	HH86
	4	755U
	5	755U
	6	755U
	7	755U
	8	0000
	9	755U[1]
	10	755U[1]
	11	755U[1]
	12	755U[1]
	13	577A
	14	F615
	15	755U[1]
	16	755U
U7	1	89F1
	2	AC99
	3	PCF3
	4	1180
	5	0000[1]
	6	755U
	7	6F7P
	8	0000
	9	F615
	10	2F25
	11	8UH9
	12	340A
	13	P352
	14	U1U2
	15	4CP2
	16	755U

IC	PIN NO.	SIGNATURE
U8	1	0000
	2	H335
	3	H335
	4	C113
	5	C113
	6	7050
	7	7050
	8	0772
	9	0772
	10	0000
	11	755U[1]
	12	C4C3
	13	C4C3
	14	AA08
	15	AA08
	16	7211
	17	7211
	18	A3C1
	19	A3C1
	20	755U
U12	1	755U[1]
	2	0000[1]
	3	0000
	4	755U
	5	0000
	6	0000
	7	0000
	8	0000
	9	0000
	10	0000
	11	755U
	12	H335
	13	C113
	14	7050
	15	0772
	16	C4C3
	17	AA08
	18	7211
	19	A3C1
	20	0000
	21	7707
	22	577A
	23	HH86
	24	89F1
	25	AC99
	26	PCF3
	27	1180
	28	0000[1]

IC	PIN NO.	SIGNATURE
U12	29	755U
	30	755U[1]
	31	755U
	32	755U[1]
	33	755U
	34	0000
	35	755U
	36	755U
	37	755U[1]
	38	0000
	39	0000
	40	755U
U15	1	755U[1]
	2	755U[1]
	3	755U[2]
	4	755U
	5	755U[2]
	6	755U
	7	755U[2]
	8	755U
	9	Unstable
	10	0000
	11	755U
	12	755U[1]
	13	755U
	14	755U[1]
	15	755U
	16	755U[1]
	17	755U
	18	Unstable
	19	755U[1]
	20	755U
U16	1	755U[1]
	2	0000
	3	755U[2]
	4	755U
	5	755U[2]
	6	755U
	7	755U[2]
	8	755U[1]
	9	Unstable
	10	0000
	11	755U
	12	755U
	13	755U
	14	755U
	15	0000

IC	PIN NO.	SIGNATURE
U16	16	755U
	17	0000
	18	Unstable
	19	755U[1]
	20	755U
U17	1	755U
	2	755U
	3	755U[1]
	4	0000
	5	0000
	6	0000
	7	755U
	8	8UH9
	9	755U[1]
	10	755U
	11	0000
	12	755U[2]
	13	755U[2]
	14	755U[2]
	15	Unstable
	16	755U[2]
	17	755U[2]
	18	755U[2]
	19	Unstable
	20	0000
	21	H335
	22	C113
	23	7050
	24	755U
	25	755U
	26	755U
	27	0000
	28	0000
	29	0000
	30	0000
	31	755U
	32	0000
	33	0000
	34	0000
	35	755U
	36	755U
	37	755U
	38	755U
	39	755U
	40	755U

Table 7-10. A1 PCB Output-Port Test

Purpose: This test verifies whether the A1 PCB is outputting data to the A12 Microprocessor.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper U9 installed.

Signature Analyzer Setup:

START: U7, Pin 9 (TP16), Trigger _/¯ (Button Out)

STOP: SOD (TP17), Trigger _/¯ (Button Out)

CLOCK: $\overline{WR}$ (TP23), Trigger _/¯ (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: C637

NOTE

If the 5004 reads identical signatures (other than Vcc) on successive IC pins, or if the probe does not flash when a signature (other than Vcc) is read, check the front panel GPIB indicators. Correct status is: TALK, LISTEN, and LOCAL LOCKOUT brightly lit; SRQ and REMOTE dimly lit. If this is not the case, recycle both the A1 and A12 SERVICE-NORMAL switches.

IC	PIN NO.	SIGNATURE	IC	NO.	PIN SIGNATURE	IC	PIN NO.	SIGNATURE
U22	1	C637*	U22	15	29F0	U24	8	29F0
	2	9UU5	(Cont'd)	16	9UU4		9	0000*
	3	C637*		17	0000*		10	0000
	4	C637*		18	C637*		11	51P2
	5	29F1		19	29F1		12	C637
	6	9UU5		20	C637		13	9UU4
	7	C637*					14	29F0
	8	C637*	U24	1	C637*		15	C637
	9	29F0		2	C637*		16	C637
	10	0000		3	9UU5		17	9UU4
	11	C637*		4	29F1		18	29F1
	12	9UU4		5	C637*		19	C637*
	13	0000		6	C637*		20	C637
	14	C637*		7	9UU5			

* Logic Probe flashes.

Table 7-11. A1 PCB Input Port Test

Purpose: This test can be used to check whether the A1 PCB is responding to inputs from the GPIB.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper U9 installed.

Signature Analyzer Setup:

START: LDOR SEL (TP25), Trigger ↘ (Button In)

STOP: L STATUS SEL (TP26), Trigger ↗ (Button Out)

CLOCK: $\overline{RD}$ (TP24), Trigger ↗ (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: 72A2

NOTE

If the 5004 reads identical signatures (other than Vcc) on successive IC pins, or if the probe does not flash when a signature (other than Vcc) is read, check the front panel GPIB indicators. Correct status is: TALK, LISTEN, and LOCAL LOCKOUT brightly lit; SRQ and REMOTE dimly lit. If this is not the case, recycle both the A1 and A12 SERVICE-NORMAL switches.

Procedure:

1. Set up test equipment as shown in Figure 7-26.
2. Sequentially touch the data probe to TP1 thru TP7; verify that each test point exhibits a stable signature.
3. Using controller, send the following statements over the bus:

```
10 OUTPUT 705 ;"FUL"
20 GOTO 10
30 END
```

4. Recheck the above test points and verify that TP2 thru TP7 exhibit unstable signatures.

Table 7-12. A1 PCB Retrace Blanking Flip-Flop Test

Purpose: This test verifies whether the Retrace Blanking FF (U23) is working properly.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode. Free-run jumper U9 installed.

Signature Analyzer Setup:

START: SOD (TP17), Trigger (Button In)

STOP: SOD (TP17), Trigger (Button In)

CLOCK: CLOCK (OUT) (TP9), Trigger (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: A8H3

NOTE

If the 5004 reads identical signatures (other than Vcc) on successive IC pins, or if the probe does not flash when a signature (other than Vcc) is read, check the front panel GPIB indicators. Correct status is: TALK, LISTEN, and LOCAL LOCKOUT brightly lit; SRQ and REMOTE dimly lit. If this is not the case, recycle both the A1 and A12 SERVICE-NORMAL switches.

IC	PIN NO	SIGNATURE	IC	PIN NO.	SIGNATURE
U23	1	0000	U23	9	6725
	2	0000		10	A8H3
	3	A8H3		11	A8H3
	4	A8H3		12	0000
	5	0000		13	A8H3
	6	0000		14	OFHP
	7	FU56		15	89C8
	8	0000		16	A8H3

* Logic Probe LED flashes.

7-9 A2 RAMP GENERATOR PCB

7-9.1 A2 Ramp Generator PCB, Circuit Description

The A2 Ramp Generator PCB generates one of the voltage-tuning signals used to produce the sweep generator's sweep-frequency output. The PCB also generates the **RETRACE BLANKING (+), (-); BANDSWITCH BLANKING (+), (-);** and **SEQ SYNC** signals that are output to the respective rear panel connectors. A functional block diagram of this PCB is shown in Figure 7-32; the schematic diagram (3 sheets) is shown in Figure 7-33. The A2 PCB consists of three functional blocks (Figure 7-32), which are described below.

a. Ramp Generator. This functional block produces the PCB sweep ramp output signal and the two retrace blanking pulses that are supplied to the RETRACE BLANKING (+) and (-) rear panel connectors. The block also provides control for the relay connected to the rear panel PENLIFT OUTPUT connector. The input to this functional block is the front panel SWEEP TIME control group from the A12 Microprocessor PCB. Eight bits of this nine-bit group are latched into the digital-to-analog converter (DAC) circuit (U15) when the microprocessor clocks **SP13** HIGH. The DAC output is a negative voltage that causes the Sweep Ramp Integrator (U20B) to integrate in the positive direction. When the sweep ramp reaches 10 volts, the 10V Compare circuit (U25B, U25C) causes the Sweep Direction and Dwell Gating circuit (U24A, U24B, U2A, U2B, U17C) to open Switch A and close Switch B. This switching action causes the integrator to then integrate in the negative direction (retrace). When this negative-going ramp reaches 0 volts, the 0V Compare circuit (U25D, U25A) then causes Switch B to open and Switch A to close – a switch arrangement that reconfigures the integrator to again integrate in the positive direction. A typical sweep ramp waveform is shown in Figure 7-30.

The **1 SECOND CONTROL** bit (the ninth bit in the SWEEP TIME group) is a >1- or <1-second flag bit. For sweep speeds between 1 and 99 seconds, this bit is HIGH. This HIGH causes the Sweep Ramp Integrator to integrate at the slower sweep-time rate.

The Retrace Blanking Logic circuit (Q2, U10C) causes both a plus (+) and a minus (-) 5 volt pulse to be generated during sweep retrace. The same signal that opens Switch A initiates these retrace blanking pulses.

The **H SWP** bit goes TRUE (high) to indicate when a forward sweep is in progress. This bit is supplied to the A12 Microprocessor, where it causes the front panel SWEEPING indicator to light.

The Activate Relay Logic circuit (Q3) controls relay A14K1, which is the relay that connects to the rear panel PENLIFT OUTPUT connector. This circuit has two purposes. First it activates A14K1, thus causing the XY recorder's pen to drop, when (1) the sweep generator is in the EXT OR SINGLE sweep mode, (2) sweep speed is greater than 1 second, and (3) a forward sweep occurs (**H SWP** line goes TRUE). Second it deactivates A14K1, thus causing penlift to occur, when the single-sweep ramp is interrupted and reset. To accomplish the first purpose, the circuit holds the relay deactivated (NO contacts open and NC contacts closed) when any of the following occur:

1. The **1 SECOND CONTROL** bit is LOW (sweep speeds between 10 ms and 1 s).

2. The **H SWP** bit is false (forward sweep not in progress).

3. The **H RESET** bit is TRUE (single-sweep is reset, subparagraph c below).

4. THE TRIGGER **EXT OR SINGLE SWEEP** control-word bit is not HIGH (subparagraph c below).

To accomplish the second purpose, a flip-flop circuit (U27A, U26A, U26B) deactivates the relay when reset occurs while a forward sweep is in progress (**L 10V COMPARE** line is FALSE).

b. Sweep Dwell and Related Circuits. The sweep dwell circuit causes the sweep ramp to dwell when:

1. The end of an oscillator band (EOB) is reached (bandswitch point).
2. An intensity marker command is received.
3. The top of the sweep ramp (10V) is reached.
4. The bottom of the sweep ramp (0V) is reached.

When any one of the above dwell conditions is detected, the Initiate Dwell circuit (U16B, U17A, U22A, U22B, U23A) sets the **H DWELL** line TRUE. When TRUE, **H DWELL** causes the following:

(a) The Sweep Direction and Dwell Gating circuit (U24A, U24B, U2A, U2B, U17C, U10E) to open Switch A and Switch B. Opening these switches causes voltage integration of the sweep ramp to halt;

(b) The 4 kHz clock in the Dwell Timing circuit (U3) to run at 144 kHz; thereby initiating a timing sequence.

The timing sequence initiated by the speeded-up clock consists of two timing

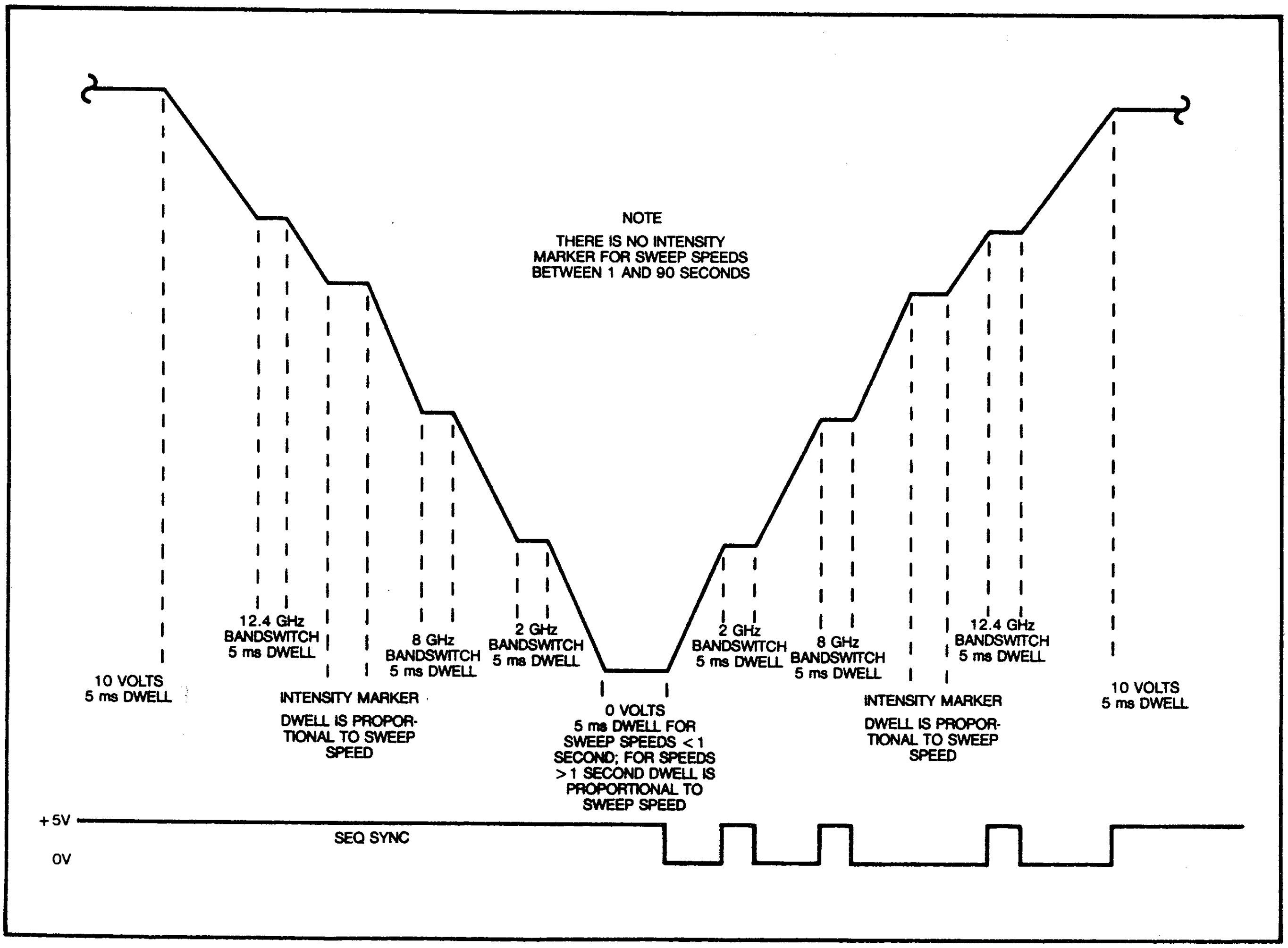


Figure 7-30. A2 PCB Sweep Ramp and Sequential Sync Pulse

pulses: **TP2** and **TP4.** The first-occurring pulse, **TP2,** loads the dwell word (described below) into the Down Counter (U9, U13). And the second-occurring pulse, **TP4,** both resets the clock to 4 kHz and enables the Down Counter. When enabled, the Down Counter sequentially counts down each time it is clocked. When a zero count is reached, the **U11 CLOCK** line is gated HIGH, which clocks the **L STRB** output from the Ext Sweep Logic circuit (U11A) TRUE. This **L STRB** output is applied to the Sweep Trigger Control Decoder circuit (U19) (subparagraph c below). Refer to Figure 7-31 for a simplified schematic and description of the Dwell-Timing circuit.

The dwell word that **TP2** loads into the Down Counter is either of two values, as determined by the Sel Logic circuit (U26C, U26D). If either (1) the sweep ramp is at 0V and the sweep time is greater than 1 second or (2) an intensity marker has been commanded, the dwell word's value represents the sweep time. Otherwise, the dwell word's value is 5 ms.

The related circuits in this block are the Level Dip circuit (U1A), the Seq Sync Logic (U23B, U5D, Q4), and the Bandswitch Blanking (Q5, Q6) circuits. The Level Dip circuit outputs a LOW when clocked by an **EOB** pulse. This LOW causes the A4 PCB to "dip" the RF output power during oscillator bandswitch.

The Seq Sync Logic circuit outputs a +5V pulse (Figure 7-30) during oscillator bandswitch, 0- and 10-volt dwell periods, and sweep ramp retrace. This pulse goes to the A1 PCB (**H SEQ**) and to the rear panel SEQ SYNC connector.

The Retrace Blanking circuit outputs plus and minus (+, -) 5V pulses during sweep ramp retrace. These pulses go to the respective rear panel connectors.

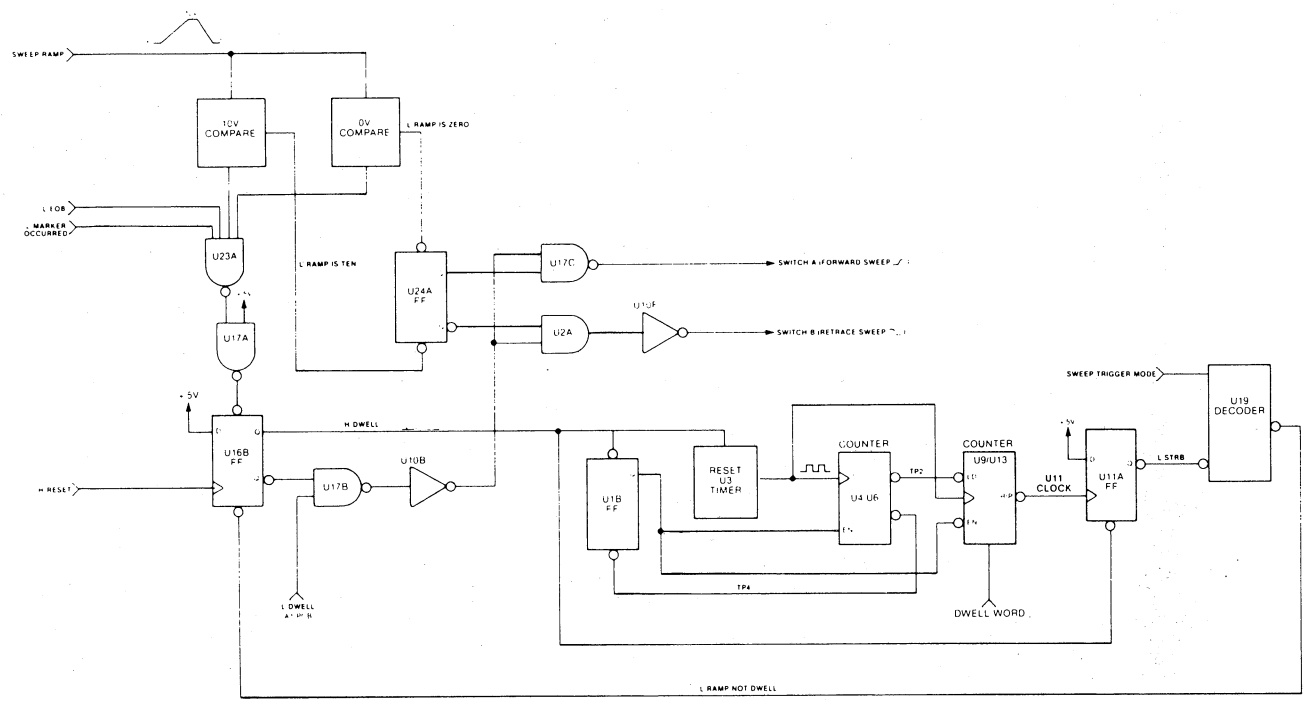
c. Sweep Trigger Control. This functional block controls the recurrence of the A2 PCB sweep ramp. The input to this block is an 8-bit control group from the A12 Microprocessor PCB. This word is latched into the Control Word Latch and Logic circuit (U14, U2C, U5F) when the microprocessor clocks **SP14** HIGH. Of these eight bits, five comprise the TRIGGER group (AUTO, LINE, or EXT OR SINGLE), one is the **1 SECOND CONTROL** bit (subparagraph b above), one is the **SEQ SYNC DISABLE** bit, and one is the **EXT FM DISABLE** bit. The **EXT FM DISABLE** bit is not used on this PCB; it is decoded here and sent to the A10 PCB. The **SEQ SYNC DISABLE** bit is used to activate the Seq Sync Disable Logic circuit (Q7). Three bits of the 5-bit control group go to the Decoder (U19), where they are used to control the trigger source. These 3 control-group bits are decoded by U19 when the **L STRB** line goes TRUE (low) (subparagraph b above). Once enabled by the **L STRB** line, U19 is controlled by the **H RAMP IS TEN** line. When TRUE, this line signals that the sweep ramp has reached its top end (10 volts). A chart showing the logic state of the **RAMP NOT DWELL** line for the various input-signal logic states is given in Table 7-13.

The remaining signal in this block is **H RESET.** This signal line pulses TRUE when the EXT OR SINGLE pushbutton is pressed while a sweep is in progress. When TRUE, **H RESET** initiates a dwell and, when the dwell period is finished, causes Switch A to close. When Switch A closes, the sweep ramp starts climbing toward 10 volts at a fast rate. When the ramp reaches 10 volts, the **L RAMP IS TEN** line enables a new sweep to be initiated when the EXT OR SINGLE pushbutton is again pressed.

Table 7-13. L RAMP NOT DWELL Logic States

STROBE U19-7	RAMP IS TEN U19-9	AUTO U19-15	LINE U19-10	EXT OR SINGLE U19-A	RAMP NOT DWELL U19-6
1	X*	X	X	X	1
0	0	X	X	X	0
0	1	1	0	0	0
0	1	X	1	0	0 Only when triggered by Line Trigger Pulse Generator. (U19-13 = 1)
0	1	X	0	1	0 Only when Single Sweep Logic circuit (U17D) has detected one of the following: a. An external trigger pulse from the rear panel. (U17D-12 = 0) b. An activate single-sweep logic level from the front panel, via the microprocessor. (U17D-13 = 0)

* = Don't Care



As an example to aid in tracing the logic of the Dwell Timing circuit, the following narrative describes circuit operation for a 10V dwell command.

The 10V Compare circuit senses when the sweep ramp reaches its upper limit of 10 volts. When this occurs the circuit outputs a LOW to U24A and U23A. This LOW clears the U24A "Q-bubble" output HIGH, and, via U23A and U17A, it presets the U16B "Q" output HIGH and "Q-bubble" output LOW. The LOW from U16B, via U17B and U10B, inhibits gates U2A and U17C. When inhibited these two gates cause both Switch A and Switch B to open, thus halting the sweep ramp.

The HIGH signal from U16B, **H DWELL,** is applied to U1B, U3, and U11A. At U3, it resets the Timer and causes it to output pulses. These pulses initiate a timing sequence. The first pulse in this sequence, TP2, loads the dwell word into downcounters U9 and U13. The second pulse, TP4, clears the U1B "Q" output LOW. This LOW enables the counter, which starts it counting down. when the countdown is complete, the U9/U13 "RIP" output goes LOW and clocks U11A. When clocked U11A outputs a LOW that enables U19 to decode the microprocessor-supplied sweep-trigger-mode data. If the sweep mode permits (Table 7-13), U19 sets the L RAMP NOT DWELL line TRUE. When TRUE this line clears U16B, thus setting the "Q-bubble" output HIGH and the "Q" output LOW. The HIGH enables U2A, allowing previously set HIGH on the U24A "Q-bubble" output to close Switch B. When closed Switch B causes the ramp to retrace toward zero volts.

Figure 7-31. Dwell-Timing Circuit, Simplified Schematic and Description

iate a
in this
rd into
second
output
ounter,
ien the
J9/U13
U11A.
W that
the
rigger-
permits
P NOT
E this
he "Q-
output
llowing
A "Q-
When
mp to

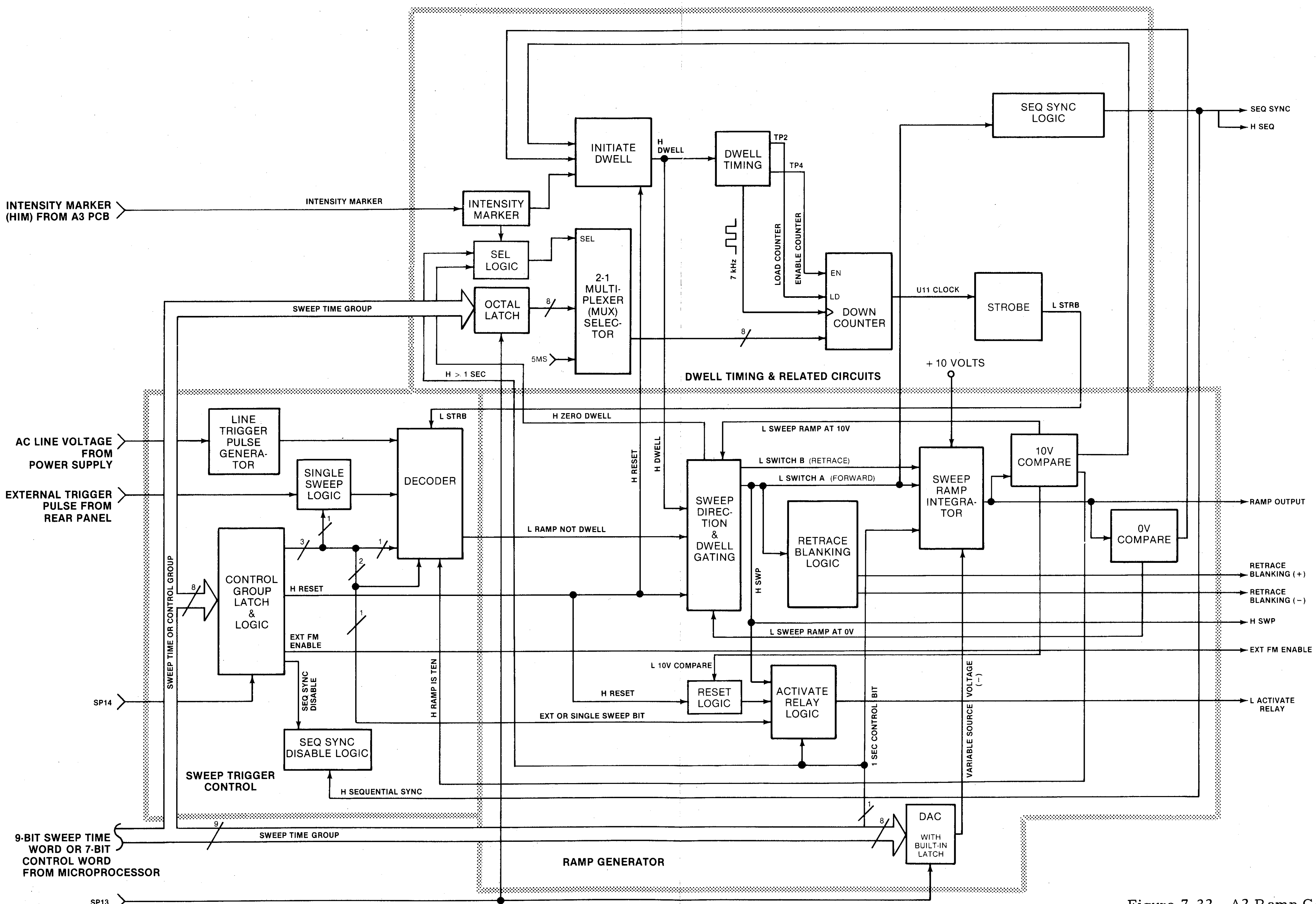


Figure 7-32. A2 Ramp Generator Functional Block Diagram

Figure 7-31

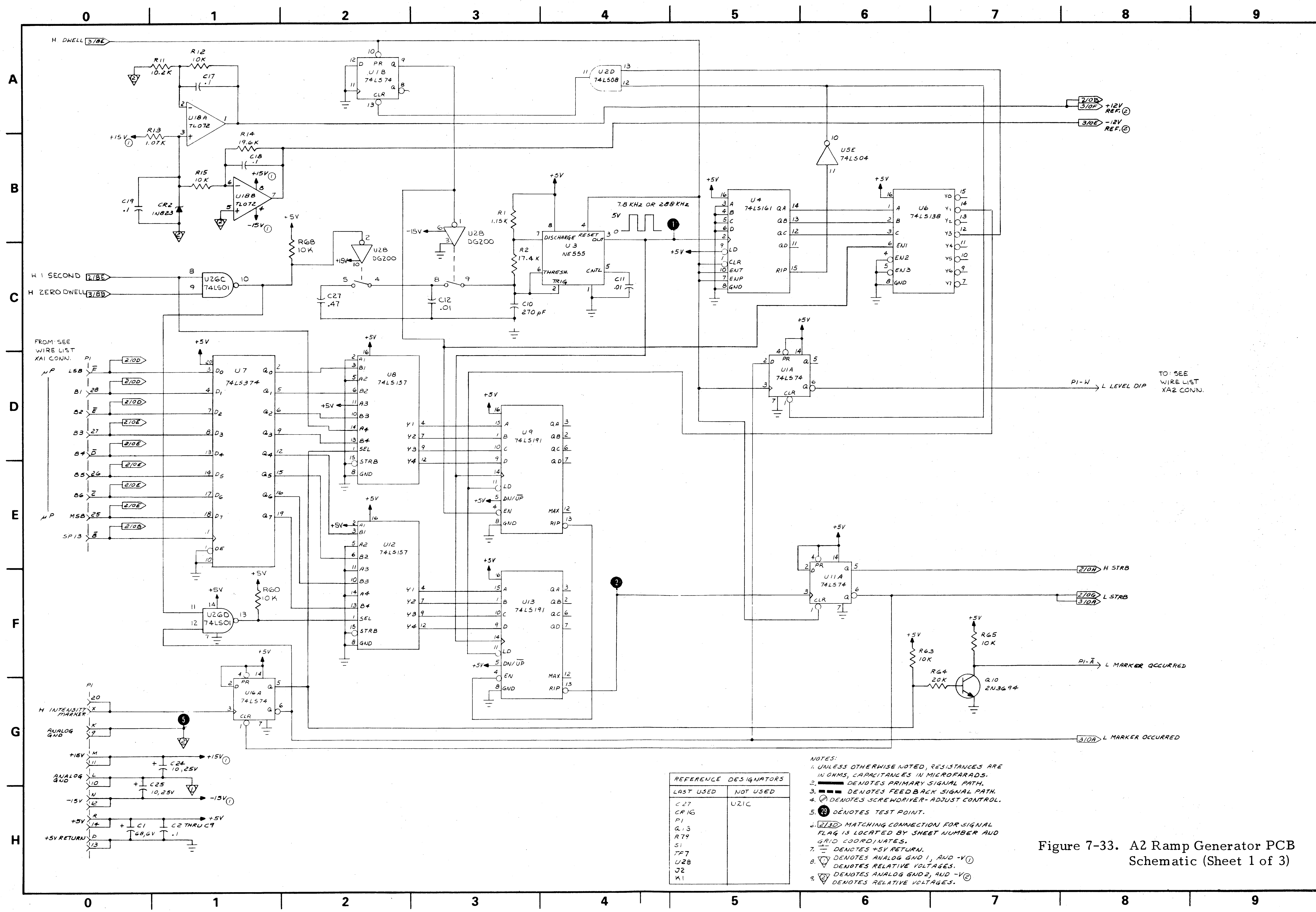
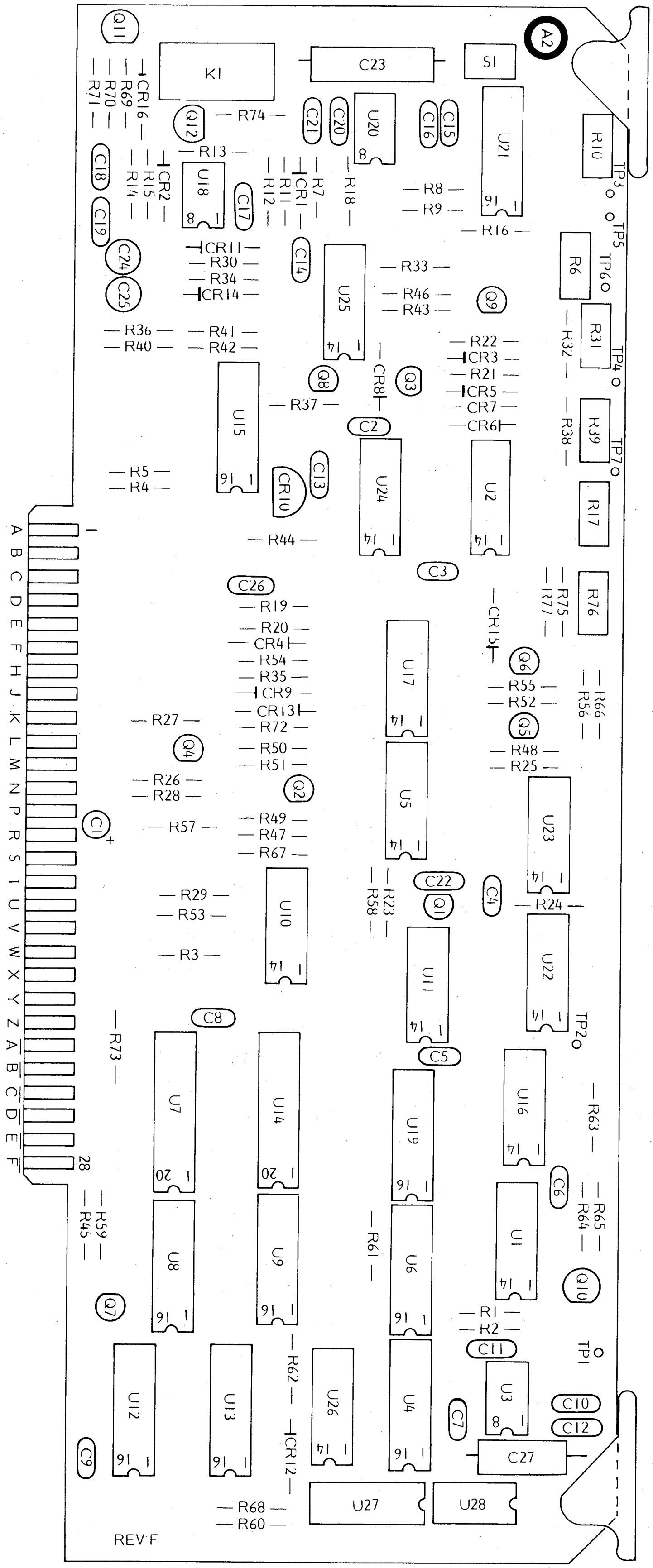


Figure 7-33. A2 Ramp Generator PCB Schematic (Sheet 1 of 3)



A2 PCB Parts Locator Diagram

Figure 7-33
(Sheet 1 of 3)

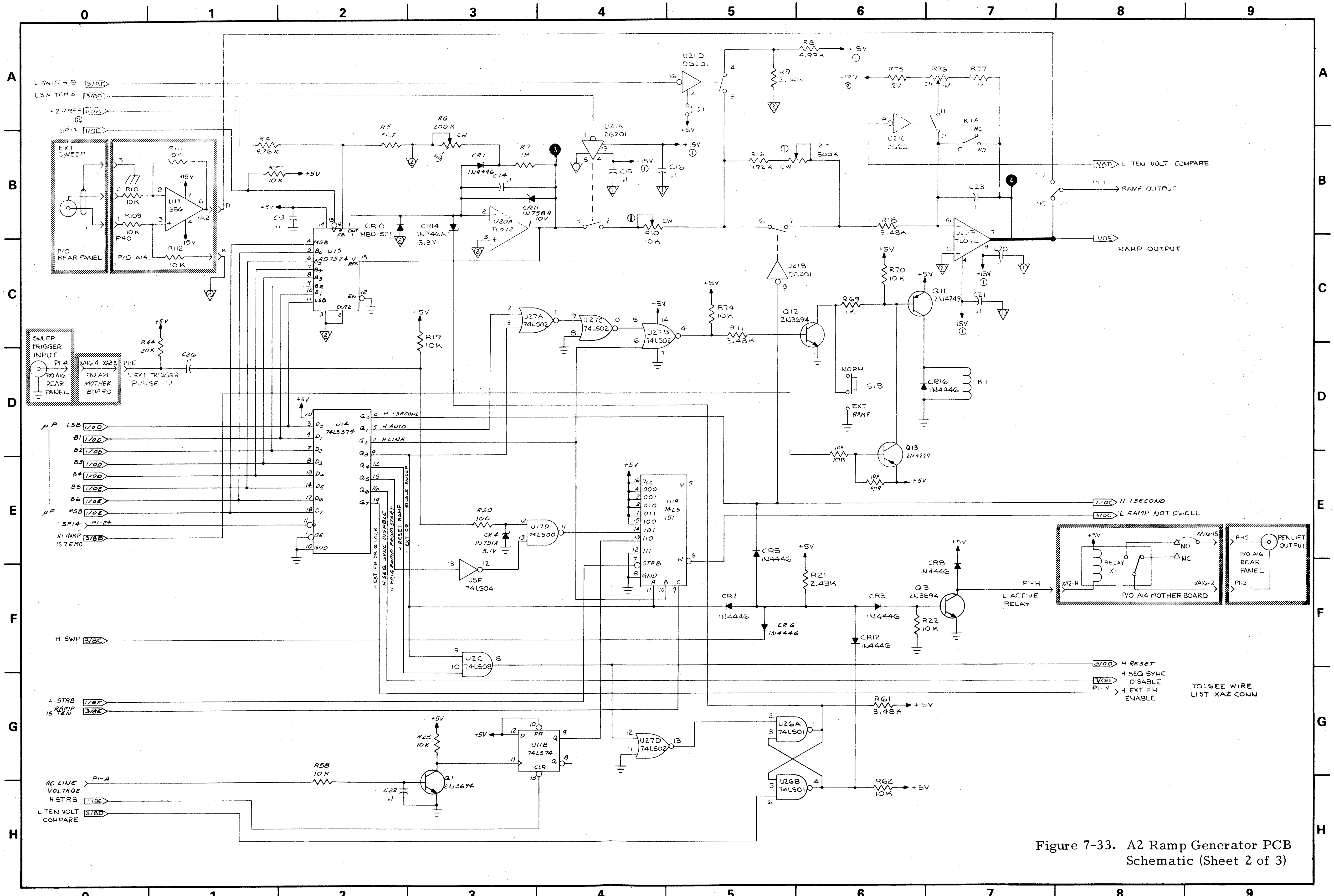


Figure 7-33. A2 Ramp Generator PCB Schematic (Sheet 2 of 3)

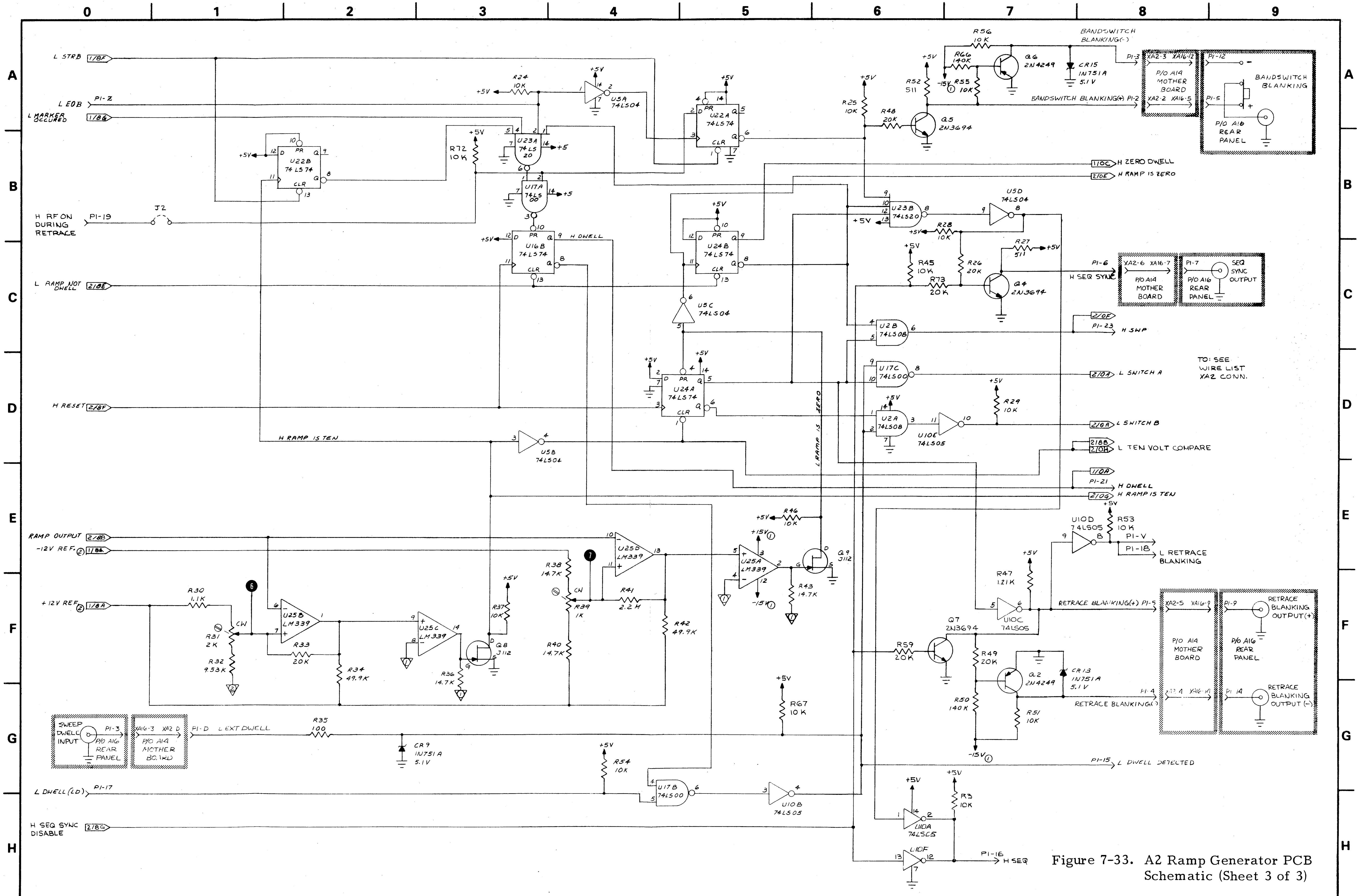
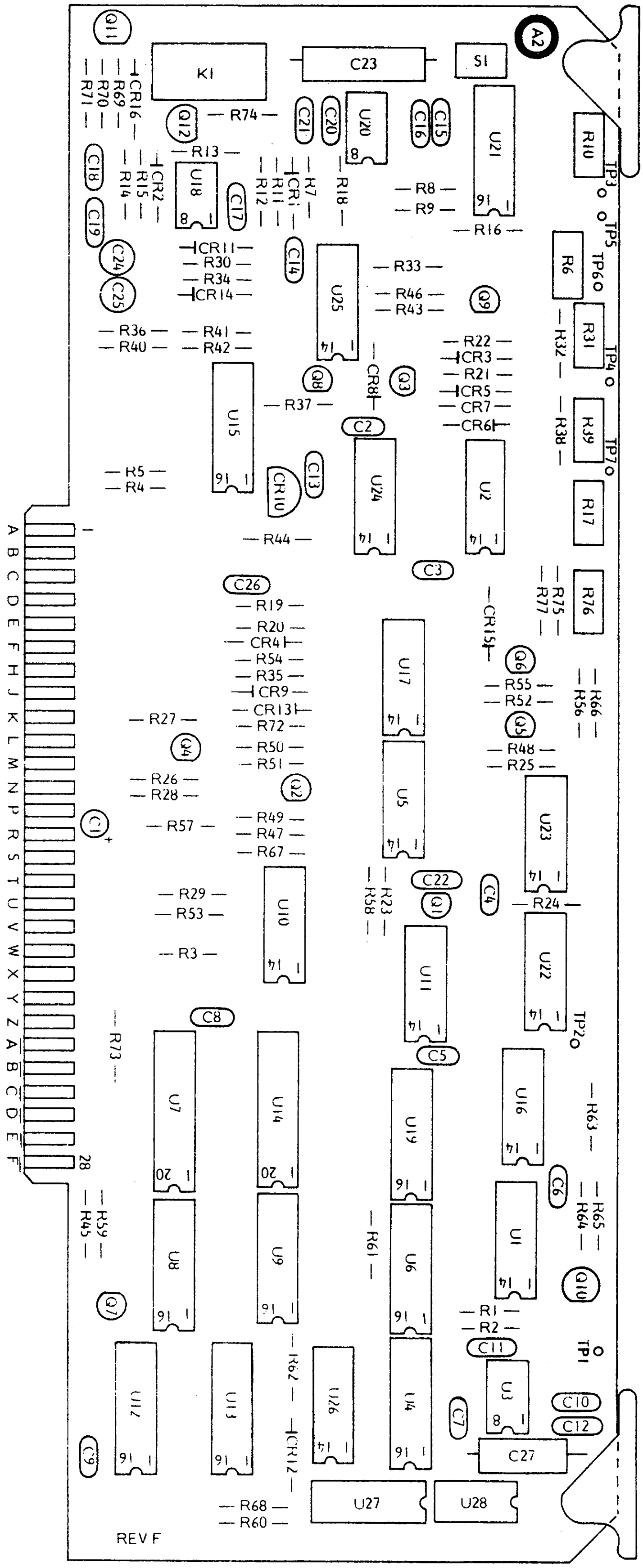


Figure 7-33. A2 Ramp Generator PCB Schematic (Sheet 3 of 3)

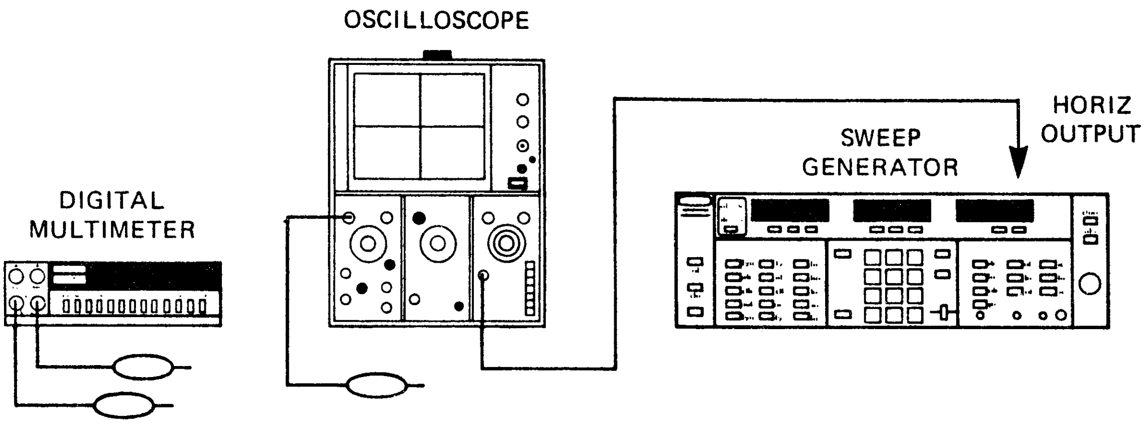


A2 PCB Parts Locator Diagram

7-9.2 A2 Ramp Generator PCB, Troubleshooting Information and Data

Error code 21 reports on the status of the A2 Ramp Generator PCB. The microprocessor routine associated with this error code starts a sweep ramp, and then verifies that the ramp has occurred. The routine accomplishes this by starting an 8 ms ramp, and then – after a microprocessor-determined time – checking the **H SWP** and **L DWELL DETECTED** control lines. If the **H SWP** line has toggled from HIGH to LOW, a forward sweep has occurred. And if the **L DWELL DETECTED** line has toggled from LOW to HIGH, a retrace sweep has occurred.

The test setup for troubleshooting Error Code 21 is provided in Figure 7-34; the troubleshooting flowchart (2 sheets) is provided in Figure 7-35.



SWEEP GENERATOR CONTROL SETTINGS

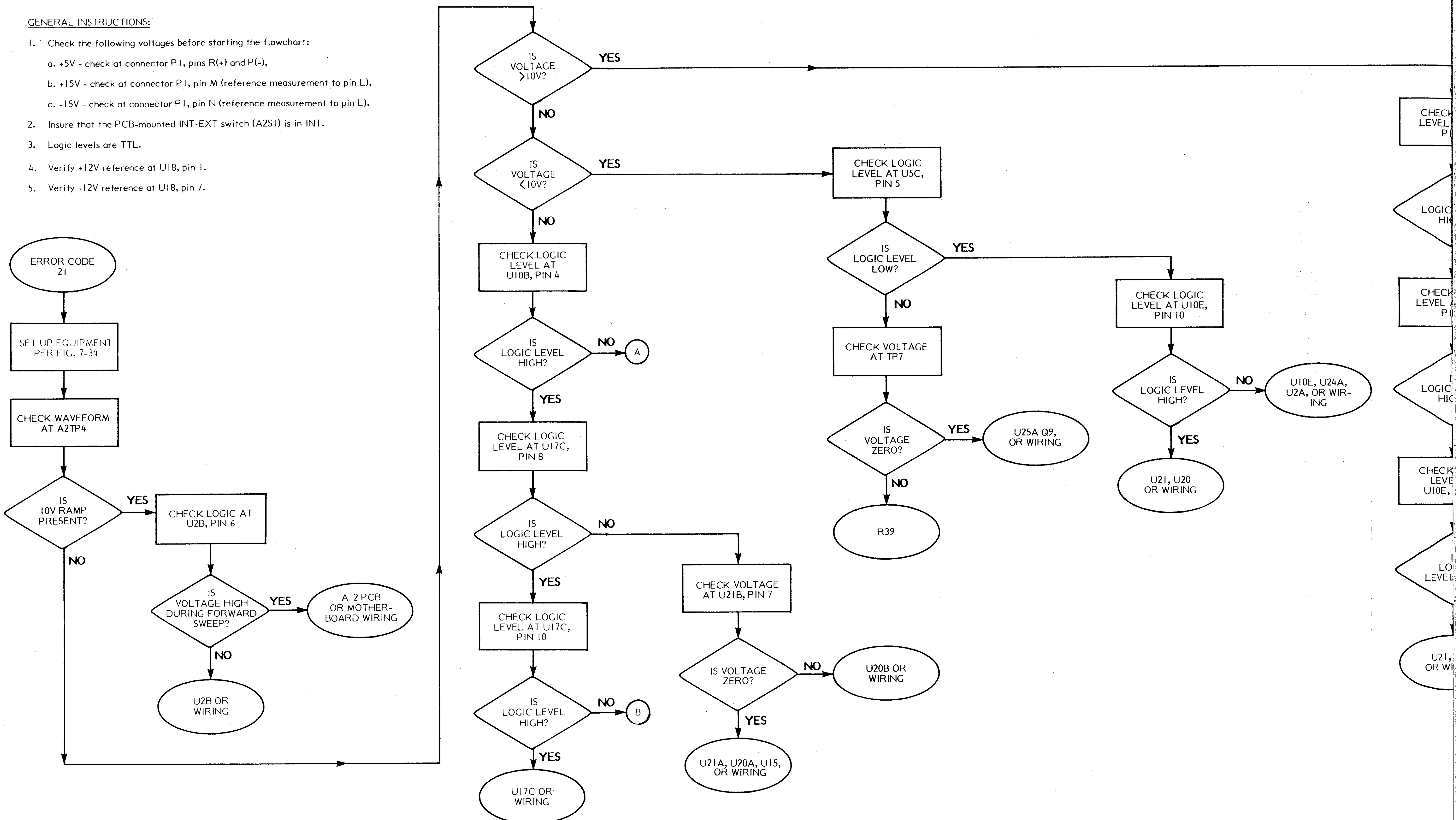
FREQUENCY RANGE: FULL
TRIGGER: AUTO
MARKERS: VIDEO
LEVELING: INTERNAL
RETRACE RF: ON
RF: ON

RF SLOPE: OFF
LEVEL: 0 dBm
SWEEP TIME: 10 ms

Figure 7-34. Test Equipment Setup for Troubleshooting Error Code 21

GENERAL INSTRUCTIONS:

1. Check the following voltages before starting the flowchart:
   a. +5V - check at connector P1, pins R(+) and P(-),
   b. +15V - check at connector P1, pin M (reference measurement to pin L),
   c. -15V - check at connector P1, pin N (reference measurement to pin L).
2. Insure that the PCB-mounted INT-EXT switch (A2S1) is in INT.
3. Logic levels are TTL.
4. Verify +12V reference at U18, pin 1.
5. Verify -12V reference at U18, pin 7.



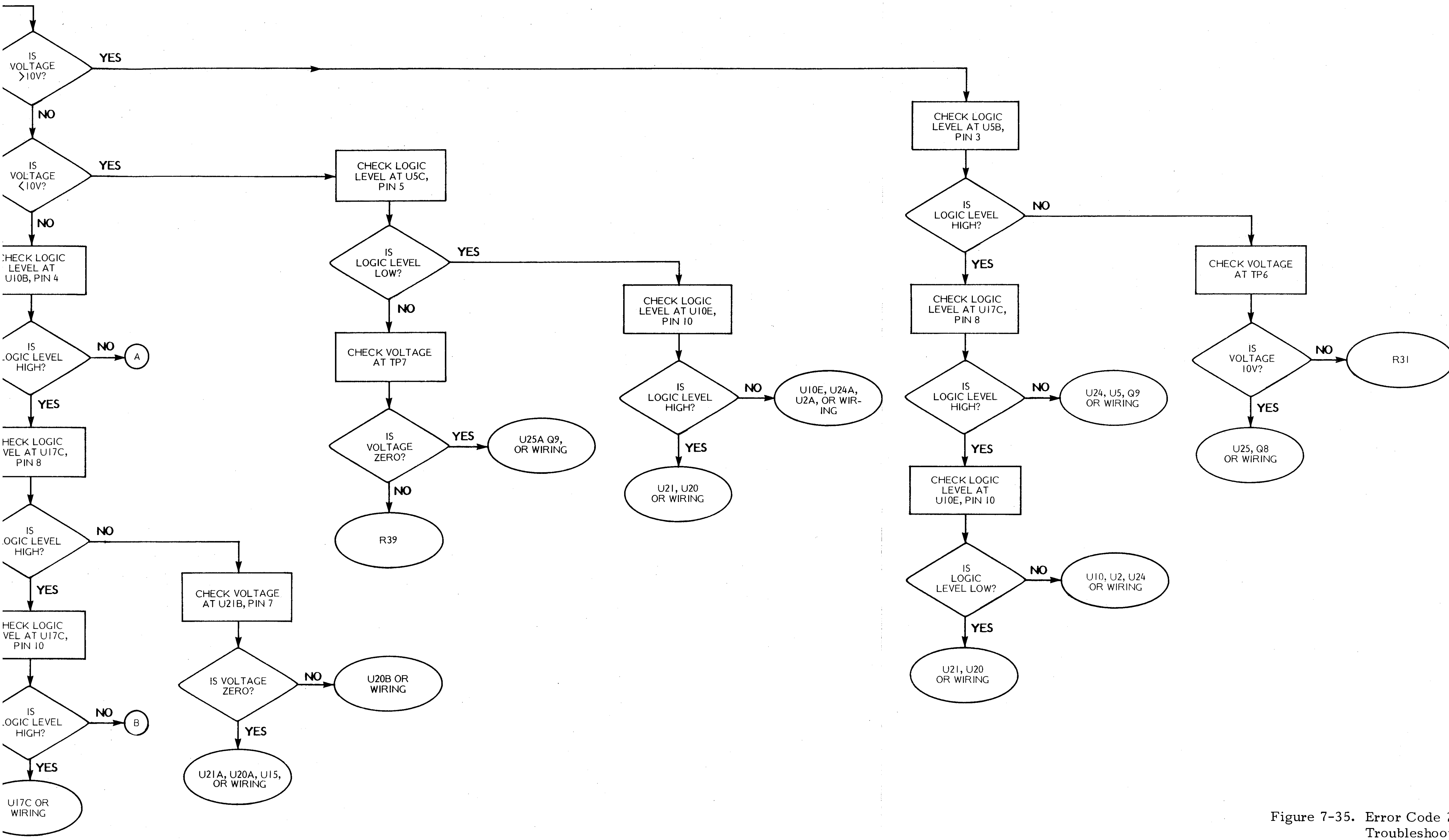
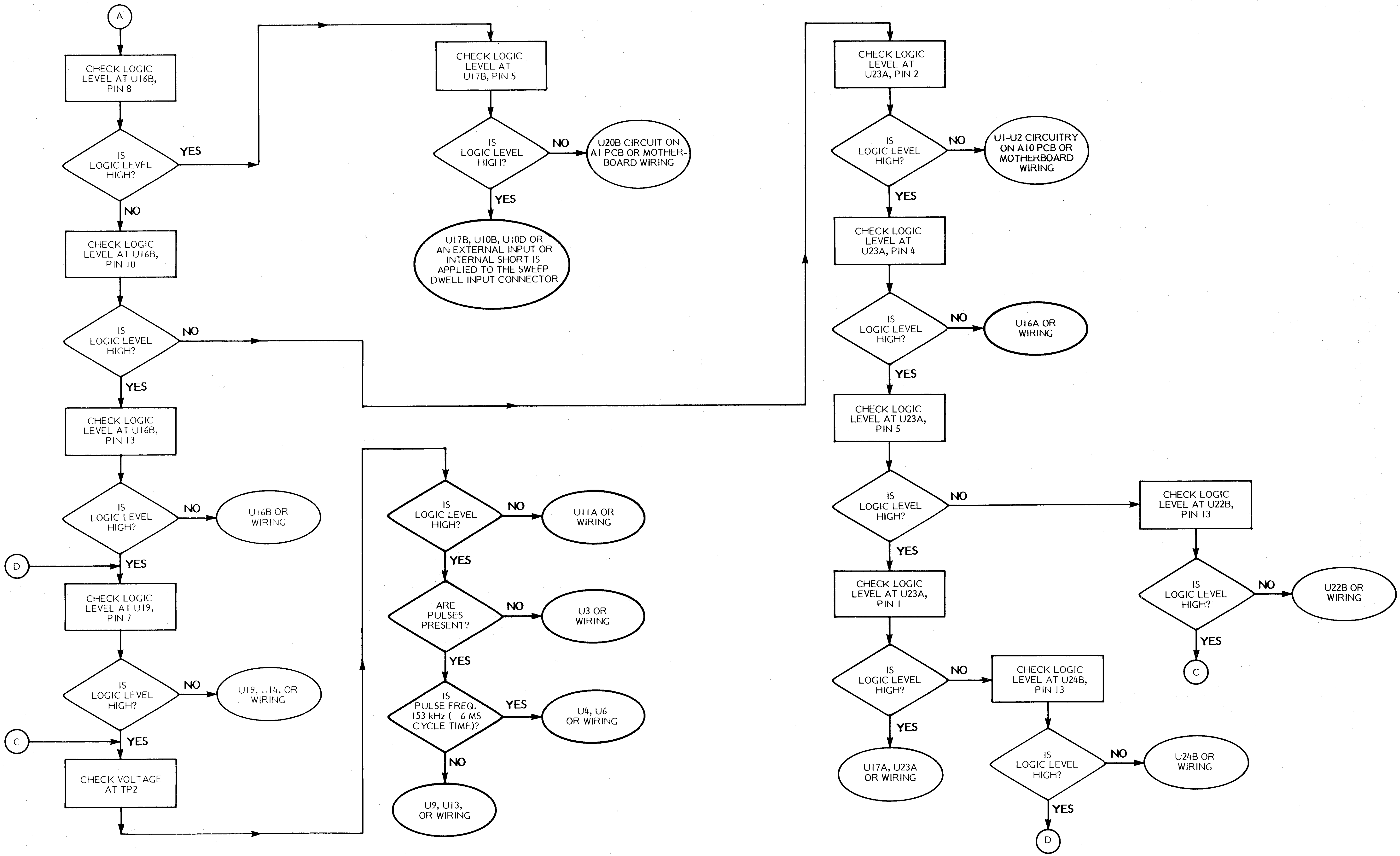


Figure 7-35. Error Code 21 Troubleshooting Flowchart (Sheet 1 of 2)


A
CHECK LOGIC LEVEL AT U16B, PIN 8
IS LOGIC LEVEL HIGH?
YES
NO
CHECK LOGIC LEVEL AT U16B, PIN 10
IS LOGIC LEVEL HIGH?
NO
YES
CHECK LOGIC LEVEL AT U16B, PIN 13
IS LOGIC LEVEL HIGH?
NO
U16B OR WIRING
D
YES
CHECK LOGIC LEVEL AT U19, PIN 7
IS LOGIC LEVEL HIGH?
NO
U19, U14, OR WIRING
C
YES
CHECK VOLTAGE AT TP2
CHECK LOGIC LEVEL AT U17B, PIN 5
IS LOGIC LEVEL HIGH?
NO
U20B CIRCUIT ON A1 PCB OR MOTHER-BOARD WIRING
YES
U17B, U10B, U10D OR AN EXTERNAL INPUT OR INTERNAL SHORT IS APPLIED TO THE SWEEP DWELL INPUT CONNECTOR
IS LOGIC LEVEL HIGH?
NO
U11A OR WIRING
YES
ARE PULSES PRESENT?
NO
U3 OR WIRING
YES
IS PULSE FREQ. 153 kHz (6 MS CYCLE TIME)?
YES
U4, U6 OR WIRING
NO
U9, U13, OR WIRING
CHECK LOGIC LEVEL AT U23A, PIN 2
IS LOGIC LEVEL HIGH?
NO
U1-U2 CIRCUITRY ON A10 PCB OR MOTHERBOARD WIRING
YES
CHECK LOGIC LEVEL AT U23A, PIN 4
IS LOGIC LEVEL HIGH?
NO
U16A OR WIRING
YES
CHECK LOGIC LEVEL AT U23A, PIN 5
IS LOGIC LEVEL HIGH?
NO
CHECK LOGIC LEVEL AT U22B, PIN 13
IS LOGIC LEVEL HIGH?
NO
U22B OR WIRING
YES
C
YES
CHECK LOGIC LEVEL AT U23A, PIN 1
IS LOGIC LEVEL HIGH?
NO
CHECK LOGIC LEVEL AT U24B, PIN 13
IS LOGIC LEVEL HIGH?
NO
U24B OR WIRING
YES
D
YES
U17A, U23A OR WIRING

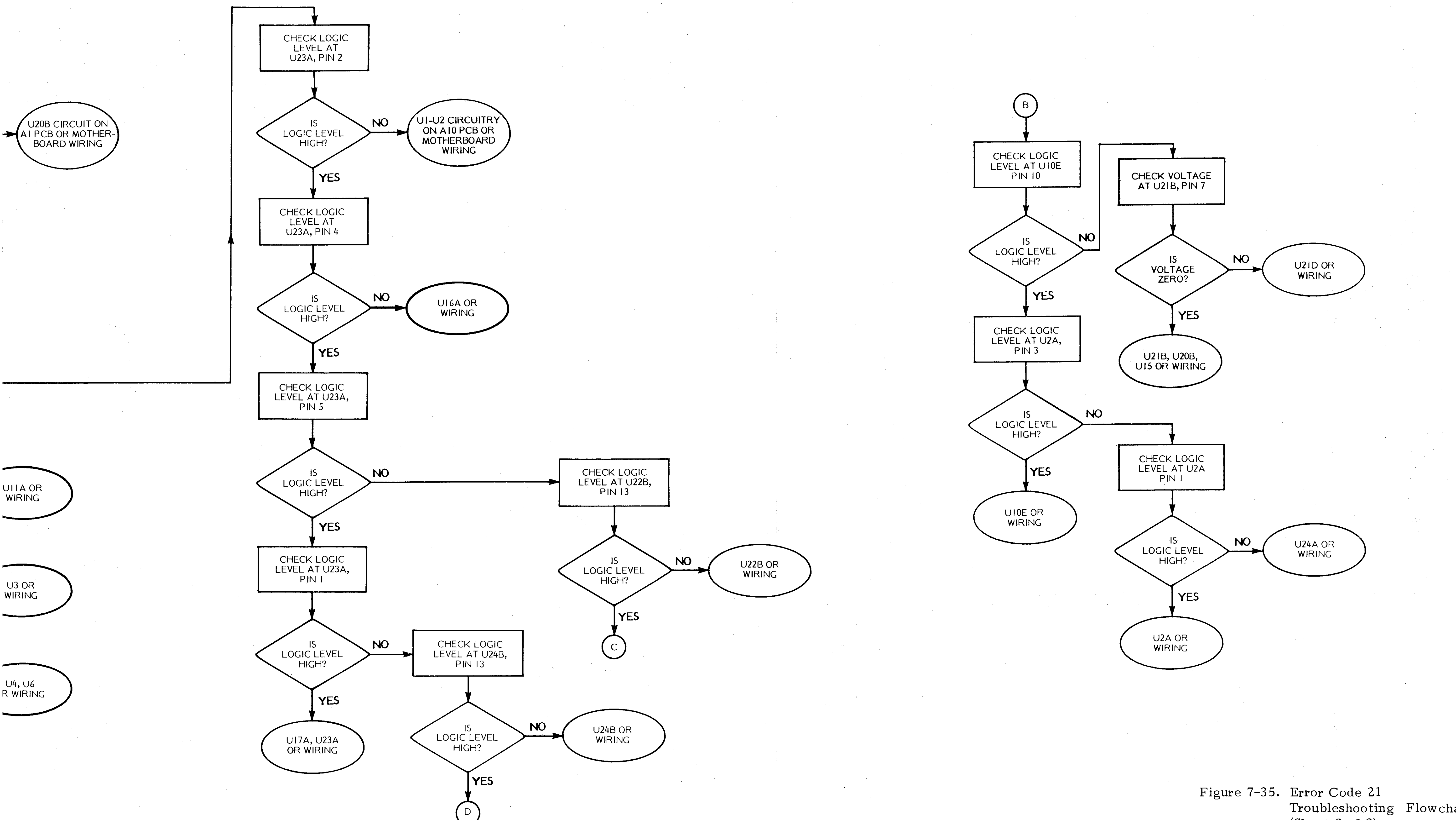


Figure 7-35. Error Code 21 Troubleshooting Flowchart (Sheet 2 of 2)

Figure 7-35(A).

7-10 A3 MARKER GENERATOR PCB

7-10.1 A3 Marker Generator PCB, Circuit Description

The A3 Marker Generator PCB generates the RF, Video, and Intensity markers. In addition, the PCB also contains the logic circuitry associated with the front panel INCREASE/DECREASE lever. A functional diagram of the marker generator circuitry is shown in Figure 7-36, and a similar diagram for the INCREASE/DECREASE lever logic circuitry is shown in Figure 7-37. The A3 PCB schematic diagram (4 sheets) is contained in Figure 7-38, and the circuits are described below.

a. Marker Generator Circuits. As shown in Figure 7-36, the inputs to the Marker Generator are a 0-10V sweep ramp from the A5 PCB and the retrace blanking control line from the A2 PCB, plus the data bus and several control lines from the A12 PCB. The 0-10V sweep ramp (**RAMP, 0-10V**) may be either the **RAMP OUT** signal from the A2 PCB, the **MAN SWEEP INPUT** from the front panel, or the Step Freq DAC signal (paragraph 3-7.2) from the A5 PCB. The inputs from the A12 PCB are as follows:

1. three marker-frequency (F0, M1, M2), 8-bit digital groups
2. a 3-bit marker mode and a 3-bit marker-frequency-disable control group
3. four latch-clock control bits (SP9, SP10, SP11, SP12)
4. three marker-identify control bits.

The three marker-frequency digital groups represent either the preset marker frequencies (paragraph 3-2.7) or the marker frequencies selected using the front panel controls (paragraph 3-2.4).

The three digital groups provide the inputs for the three digital-to-analog converter circuits (DACs) (U5-U8A, U6-U9A, U7-U10A). These DAC circuits have built-in latches. When the microprocessor clocks these DAC latches HIGH, the marker-frequency words are loaded and subsequently converted to discrete voltages between 0 and 10 volts. These voltages represent the marker's relative position within the band of frequencies being swept. For example, 3 volts would indicate that the marker frequency is located approximately 1/3 of the way between the low and high ends of the band; 5 volts would indicate that the marker frequency is located in the middle of the band; and 10 volts would indicate that the marker frequency is located at the high end of the band. These marker-frequency voltages are applied to the Marker Comparator circuits.

The Marker Comparator circuits (U8D, U9D, U10D) effectively compare the marker-frequency voltages with the **RAMP, 0-10V** signal. The output of each comparator is a steeply sloping ramp with voltage excursions between -13.5 and +13.5 volts. The midpoints (0V) on these ramps are the comparison points, that is, the points at which the instantaneous voltages of the sweep ramps equal the marker-frequency voltages from the DACs. The **F0**, **M1**, and **M2** ramps are applied to the Absolute Value circuits.

The Absolute Value circuits (U10C, U9B, U10B) change the **F0**, **M1**, and **M2** ramps into triangular waveforms, the apexes of which represent the respective marker's location. The usable portion of these waveforms, after being offset, varies between 0 and +5 volts. The 0-5V signals are applied to the marker output circuits, via the marker-frequency disable logic circuits (Q4, Q5, Q6).

The marker-frequency-disable logic circuits are controlled respectively by the **H F0 DISABLE**, **H M1 DISABLE**, and **H M2 DISABLE** control lines. These control lines come from the Marker Select and Control latch and logic circuits (U1, U2D, U2C, U2B). If the microprocessor disables a marker or if a marker-frequency front panel pushbutton (F0, M1, M2) is pressed, the respective marker-disable control line is set TRUE (high). When TRUE, these lines cause their respective marker's Absolute Value circuit output to be shunted to ground.

The 0-5V signals from the Absolute Value circuits are applied, via the MARKER AMPLITUDE control to the RF and Video Marker Output circuits. The control inputs to these output circuits are the **H RF MARKER ENABLE** and the **H VIDEO MARKER ENABLE** lines from the Mode Enable Logic circuits (U11C, U11D). If the MARKERS - RF pushbutton is engaged and a forward frequency sweep is in progress (**L RETRACE BLANKING** is FALSE), the **H RF MARKER ENABLE** line will be TRUE. When this line is TRUE, the output of the RF Marker Output circuit (U8B) will be a 0-5V analog signal. The actual amplitude of this signal will depend on the MARKER AMPLITUDE control setting. This 0-5V signal is applied to the A4 Automatic Level Control PCB, where it causes a "dip" in the RF output power level. If the MARKERS - VIDEO pushbutton is engaged, the Video Marker Output circuit (U9C) operation is the same as described for RF. The output of the video marker circuit is applied to the rear panel MARKER OUTPUT connector.

The 0-5V signals from the Absolute Value circuits are also applied directly to the Intensity Marker Output circuit (U12). The operation of the Intensity Marker Output circuit is similar to that described for the RF marker circuit, above. If MARKERS - INTENSITY is engaged and a forward sweep is in progress, the output of the intensity marker circuit will go HIGH when a marker is encountered. This HIGH is applied to the A2 Ramp Generator PCB, where it causes the A2-generated sweep ramp to dwell.

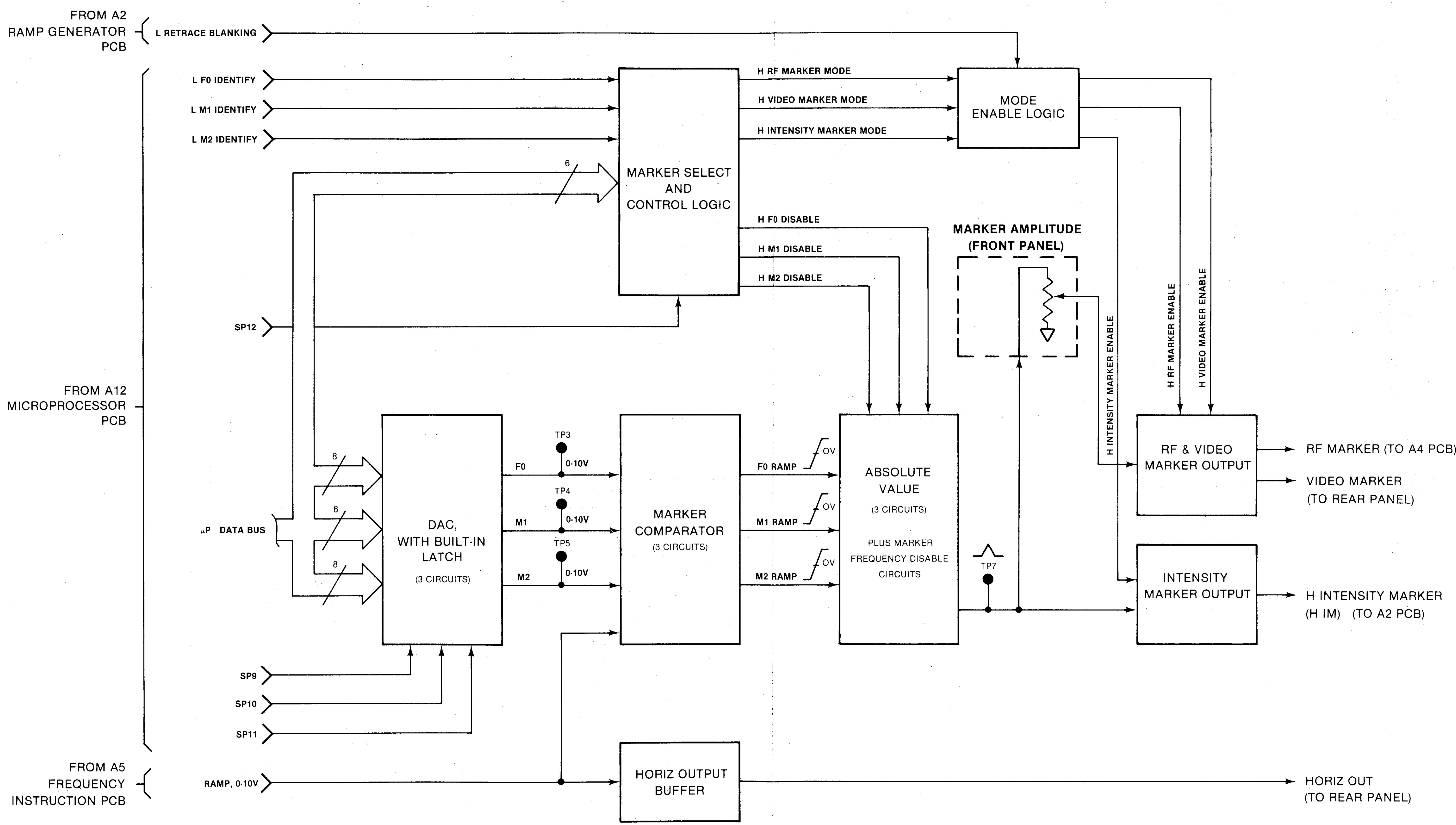


Figure 7-36. A3 PCB Marker Generator
Functional Block Diagram

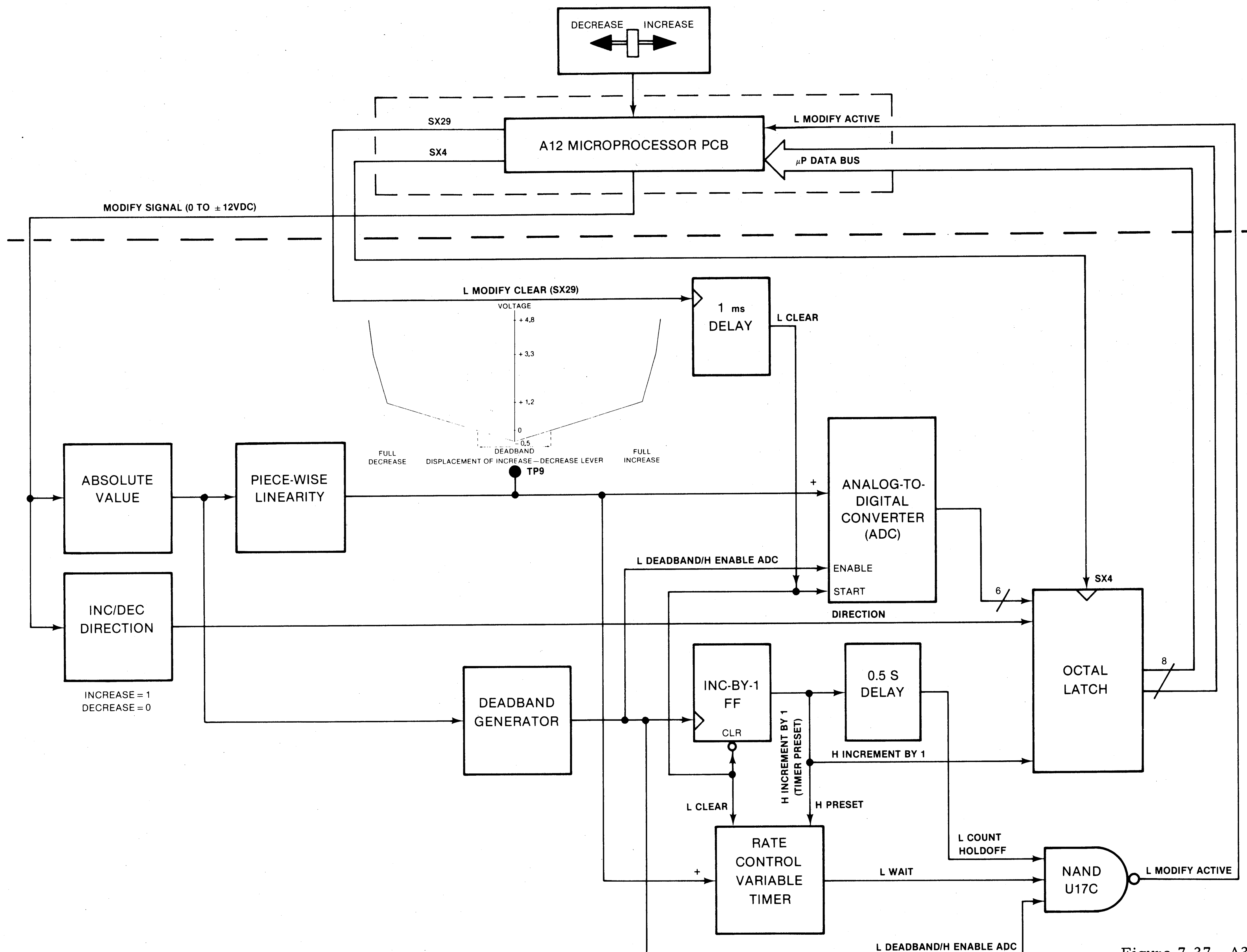


Figure 7-37. A3 PCB INCREASE/ DECREASE Logic Circuit Functional Block Diagram

b. INCREASE/DECREASE Lever Logic Circuitry. This circuitry performs two distinct functions, as follows:

1. When the INCREASE/DECREASE lever is "tapped," the circuit causes the microprocessor to increase or decrease the value of the selected parameter (paragraph 3-2.1a) in one-increment steps.

2. When the INCREASE/DECREASE lever is moved to either side from center, the circuit causes the microprocessor to increase or decrease the value of the selected parameter at a variable rate. This rate depends upon lever displacement.

The first function the circuit performs is to increase or decrease the selected parameter's value in one-increment steps. As shown in Figure 7-37, the INCREASE/DECREASE lever logic circuitry is connected in a control loop with the A12 Microprocessor PCB. The INCREASE/DECREASE lever itself is connected to the A12 PCB. This lever controls, via circuitry on the A12 PCB, the voltage level of the **MODIFY SIGNAL** input line to the A3 PCB. When the lever is moved from its center position, the **MODIFY SIGNAL** line's voltage value is between either 0 and -12 Vdc or 0 and +12 Vdc. The voltage's polarity and value depend on the direction and length of INCREASE/DECREASE lever displacement. Displacement in the DECREASE direction yields a positive voltage, and displacement in the INCREASE direction yields a negative voltage. This 0 to ±12 Vdc voltage goes to two places on the A3 PCB: the Absolute Value and the Inc/Dec Direction circuits.

At the Inc/Dec Direction circuit (U14B, Q2), the 0 to ±12 Vdc signal is translated into either a logic 1 or a logic 0, depending upon the voltage's polarity. If its polarity is negative, the logic level is a 1; if positive, the logic level is a 0. The output of this circuit (**DIRECTION** signal line) is applied to the Octal Latch (U19), where it waits to be clocked out to the microprocessor.

At the Absolute Value circuit (U13A), the 0 to ±12 Vdc signal is changed to a positive voltage when the INCREASE/DECREASE lever is moved either direction from center. (The circuit-output voltage is slightly negative when the lever is at its center (rest) position.) One portion of this signal goes to the Piece-Wise Linearity circuit; the other goes to the Deadband Generator circuit.

The purpose of the Deadband Generator circuit (U14A, Q1) is to keep the logic circuitry inactive when the INCREASE/DECREASE lever is in its center position. When the lever is moved from center, the positive output of the Absolute Value circuit causes the **L DEADBAND/H ENABLE ADC** control line to go HIGH. This control line serves the following purposes:

- When the **L DEADBAND/H ENABLE ADC** line transitions from LOW to HIGH, it clocks the **H INCREMENT BY 1 (TIMER PRESET)** control line HIGH. When HIGH, this line presets the Rate Control Variable Timer circuit (U13B, U14D, U14C, Q3), which sets the **L WAIT** control line HIGH. Also, the HIGH state of the **H INCREMENT BY 1** control line provides the logic input for the most-significant bit (MSB) of the Octal Latch.

- When the **L DEADBAND/H ENABLE ADC** line goes HIGH, it provides an enabling logic level to the Analog-to-Digital Converter (ADC) circuit (U18, U17A, U17B); it also enables one "leg" of NAND gate U17C.

The U17C NAND gate has three inputs: **L WAIT**, **L DEADBAND/H ENABLE ADC**, and **L COUNT HOLDOFF**. As already described, the first two inputs have been set HIGH; the third input, **L COUNT HOLDOFF**, is normally HIGH. Now, with all three U17C inputs HIGH, the **L MODIFY ACTIVE** line goes LOW (true). When the microprocessor senses that **L**

Figure 7-37

MODIFY ACTIVE is LOW, it uses **SX4** to clock the Octal Latch. When clocked, the Octal Latch outputs an 8-bit digital word. If the MSB of this word is a 1, the microprocessor increases or decreases (depending on the **DIRECTION** bit) the selected parameter by 1 increment. After performing this incremental function, the microprocessor uses **SX29** to clear the logic circuitry by clocking the 1 ms Delay circuit.

The 1 ms Delay circuit (U16B) generates the 1 ms L **CLEAR** pulse. This pulse goes several places. At the ADC circuit, the L **CLEAR** pulse is inverted and then ANDed with the L **DEADBAND/H ENABLE ADC** logic level. The signal resulting from this ANDing process starts the ADC voltage-conversion cycle. Once a conversion is done, U18 pin 5 goes LOW and triggers another conversion cycle. This repetitive triggering process keeps the ADC free-running as long as the **L DEADBAND/H ENABLE ADC** line stays HIGH. And this line will stay HIGH until the INCREASE/DECREASE lever is returned to its center position.

In addition to getting an ADC conversion started, the L **CLEAR** pulse has two other functions: it resets the Inc-by-1 FF, and it clears the Rate Control Variable Timer circuit.

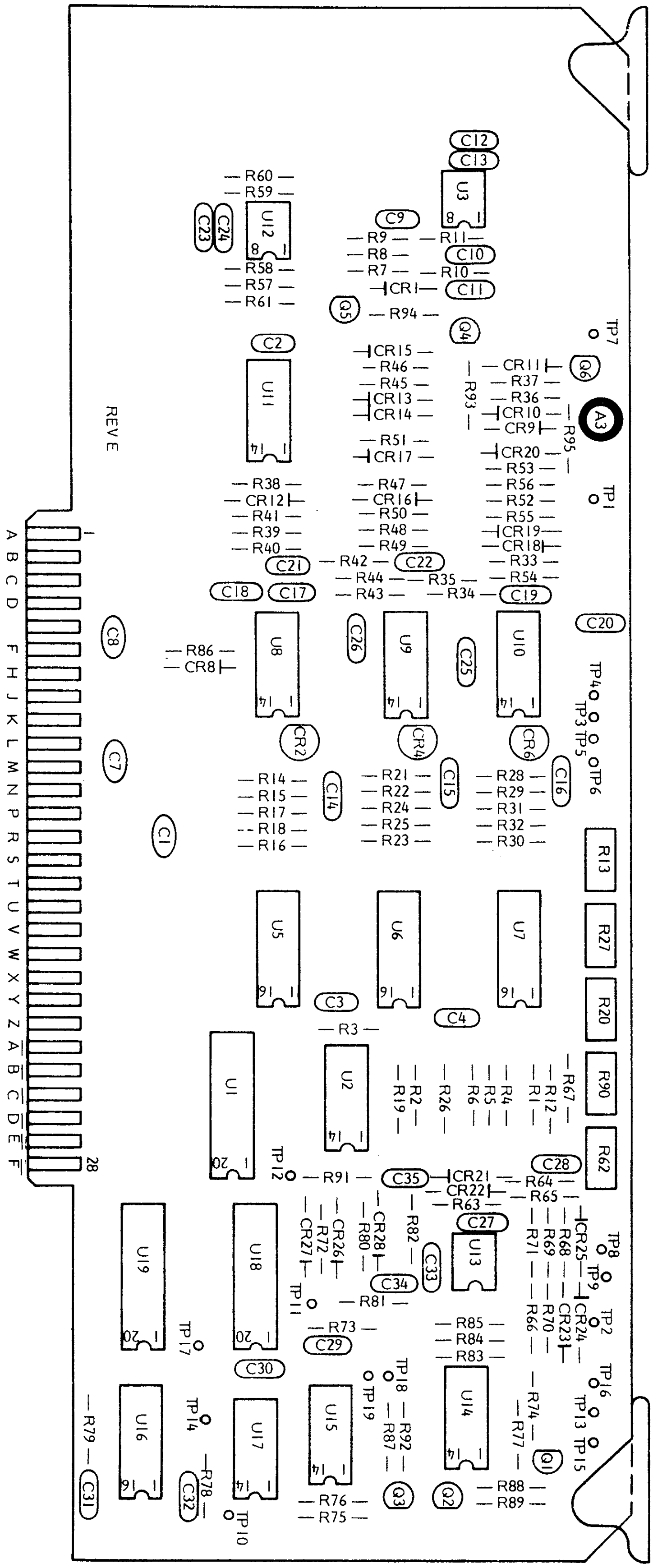
When reset, the HIGH-to-LOW transition of the Inc-By-1 FF Q-output clocks the L **COUNT HOLDOFF** control line TRUE. The TRUE state of this line causes the L **MODIFY ACTIVE** line to go FALSE and stay that way for about 0.5 seconds.

When cleared, the Rate Control Variable Timer circuit returns the L **WAIT** control line to its TRUE state. The increment-by-1 function is thus completed. Now, if the INCREASE/DECREASE lever has been moved and held rather than just "tapped," the circuit is primed for its second (variable rate) function.

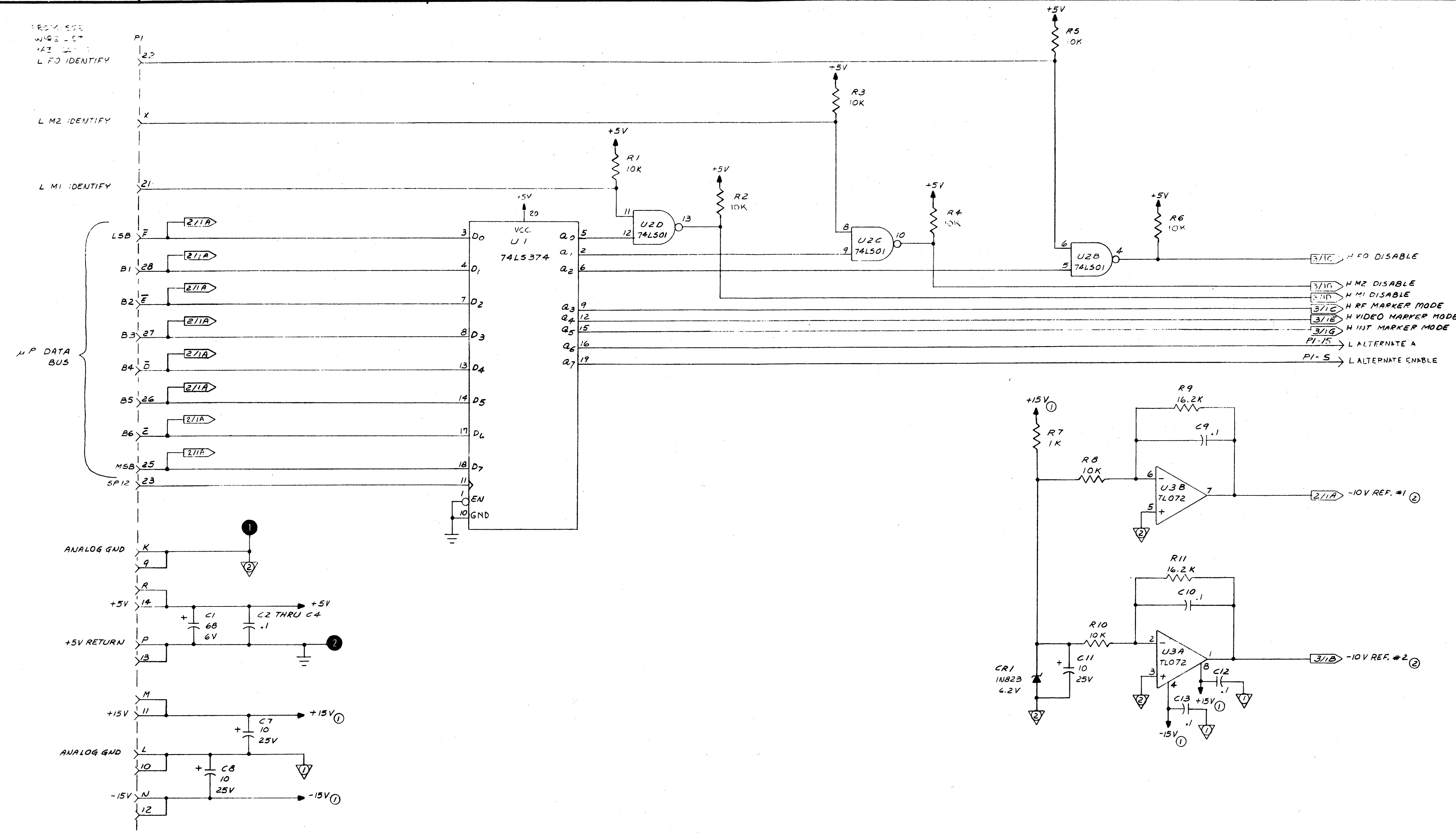
To begin the discussion of the second function, go back to the Absolute Value circuit. As mentioned earlier, a portion of this circuit's output voltage goes to the Piece-Wise Linearity circuit (R70, CR24-CR25-R69, CR23-R68, R71). This circuit is a three-piece voltage divider. The circuit provides the velocity breakpoints that can be observed as the lever is moved. These breakpoints (+1.2, +3.3, and +4.8 volts) are shown in the voltage/lever-displacement diagram above TP9. Although not drawn to scale horizontally, this diagram suggests the relationship that exists between the displacement of the lever and the speed with which the selected parameter increases or decreases.

The voltage at TP9 provides both the input for the ADC circuit, and the input for the Rate Control Variable Timer circuit.

The purpose of the Rate Control Variable Timer circuit is to slow down the count when the INCREASE/DECREASE lever is moved by only a small amount. The timer circuit uses a voltage-integrator RC (resistor-capacitor) network to form a timing ramp. When the velocity voltage at TP9 is low, the RC network capacitor takes a long time to charge; hence, the circuit produces a long time-delay. As the voltage at TP9 increases, the capacitor charges more quickly and the timer-circuit delay time becomes shorter.



A3 PCB Parts Locator Diagram



REFERENCE DESIGNATORS	
LAST USED	NOT USED
C35	U4
CR28	U15B
P1	C5, C6
Q6	CR3,5,7
R95	
TP19	
U19	

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. DENOTES SCREWDRIVER-ADJUST CONTROL.
3. DENOTES TEST POINT.
4. 2/1D MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. DENOTES PRIMARY SIGNAL PATH.
6. DENOTES FEEDBACK SIGNAL PATH
7. UNLESS OTHERWISE NOTES ALL DIODES ARE 1N4446.
8. DENOTES +5V RETURN.
9. DENOTES ANALOG GROUND 1, AND $-V_{(1)}$ DENOTES RELATIVE VOLTAGES
10. DENOTES ANALOG GROUND 2, AND $-V_{(2)}$ DENOTES RELATIVE VOLTAGES.

Figure 7-38. A3 Marker Generator PCB Schematic (Sheet 1 of 4)

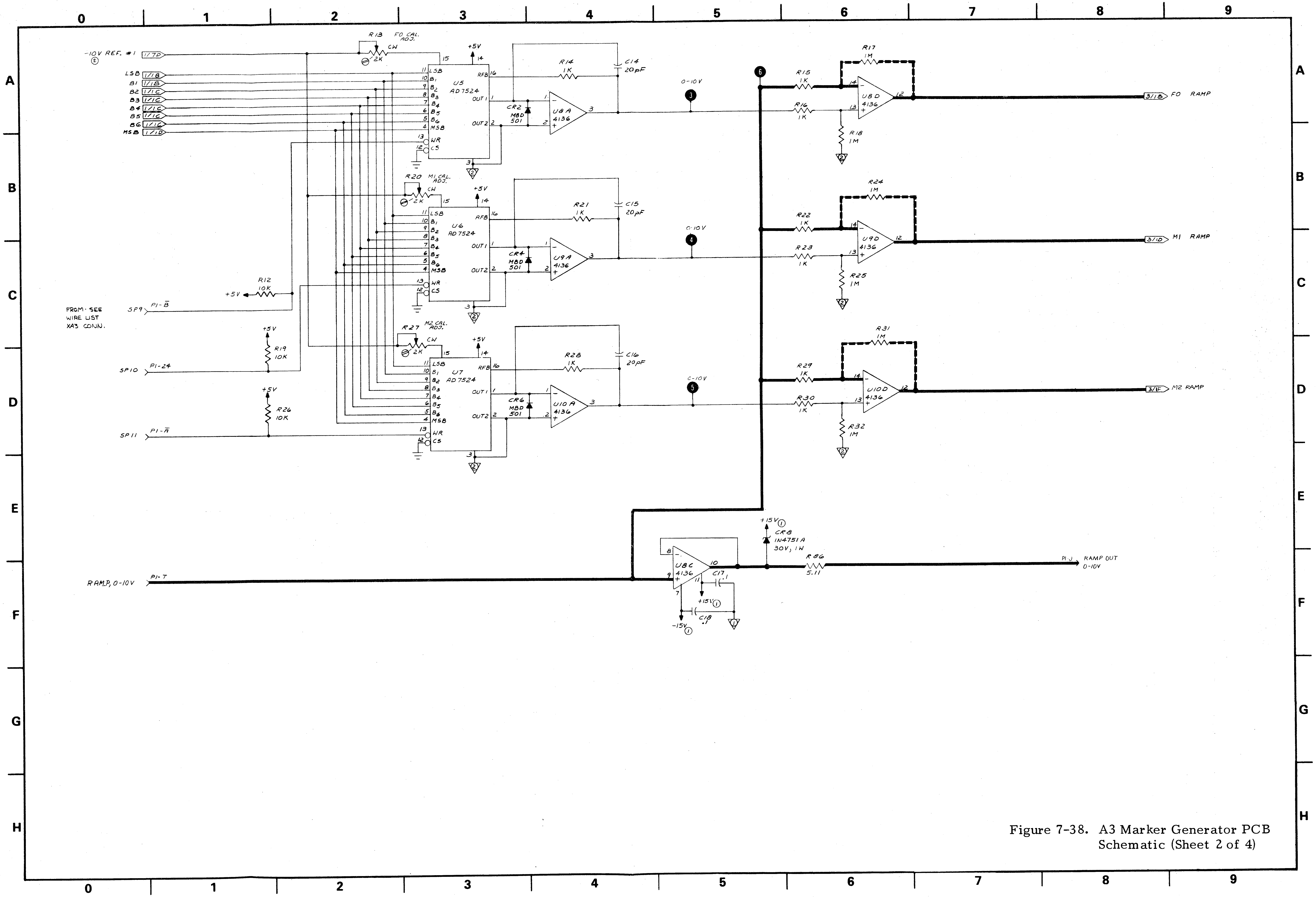


Figure 7-38. A3 Marker Generator PCB Schematic (Sheet 2 of 4)

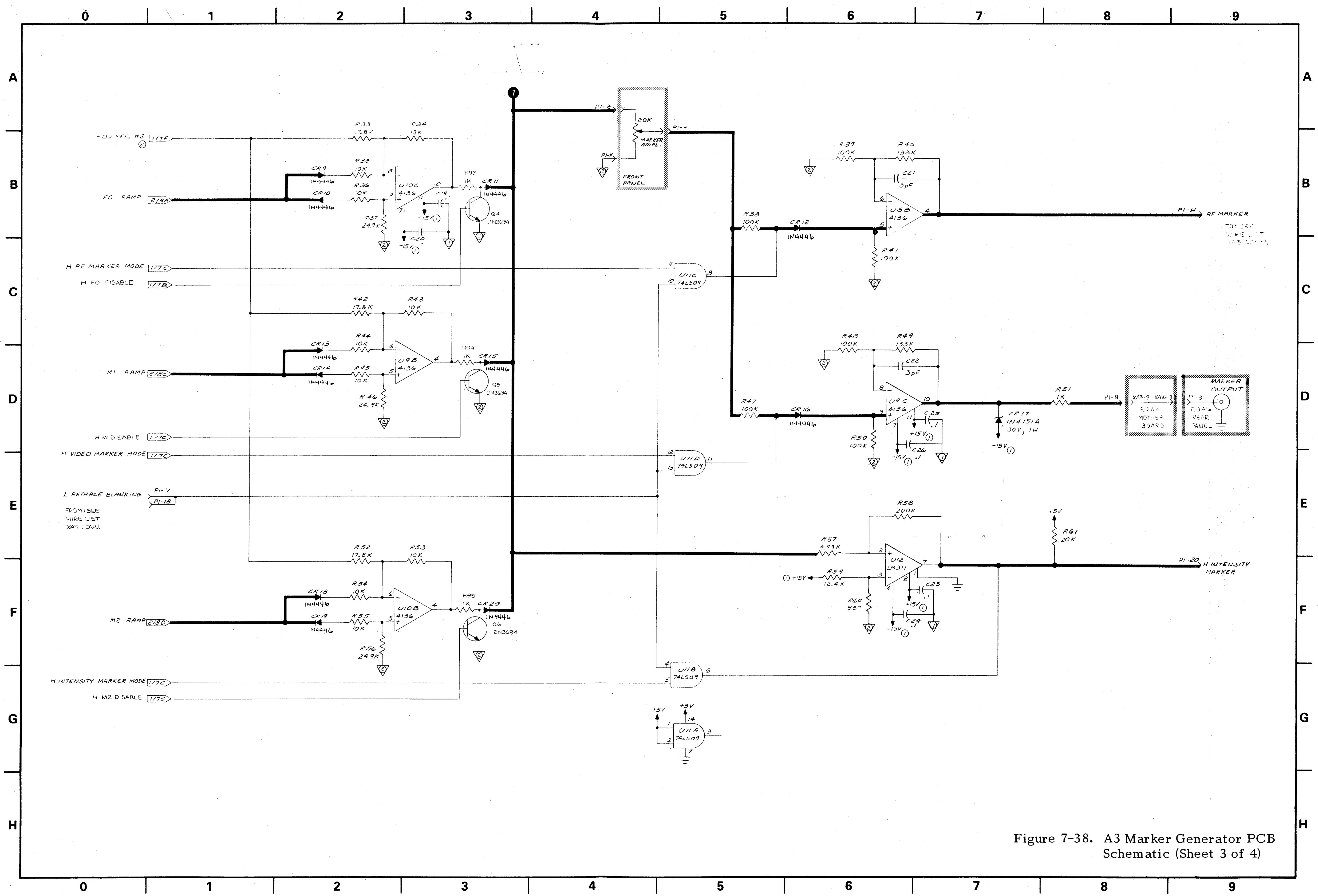


Figure 7-38. A3 Marker Generator PCB Schematic (Sheet 3 of 4)

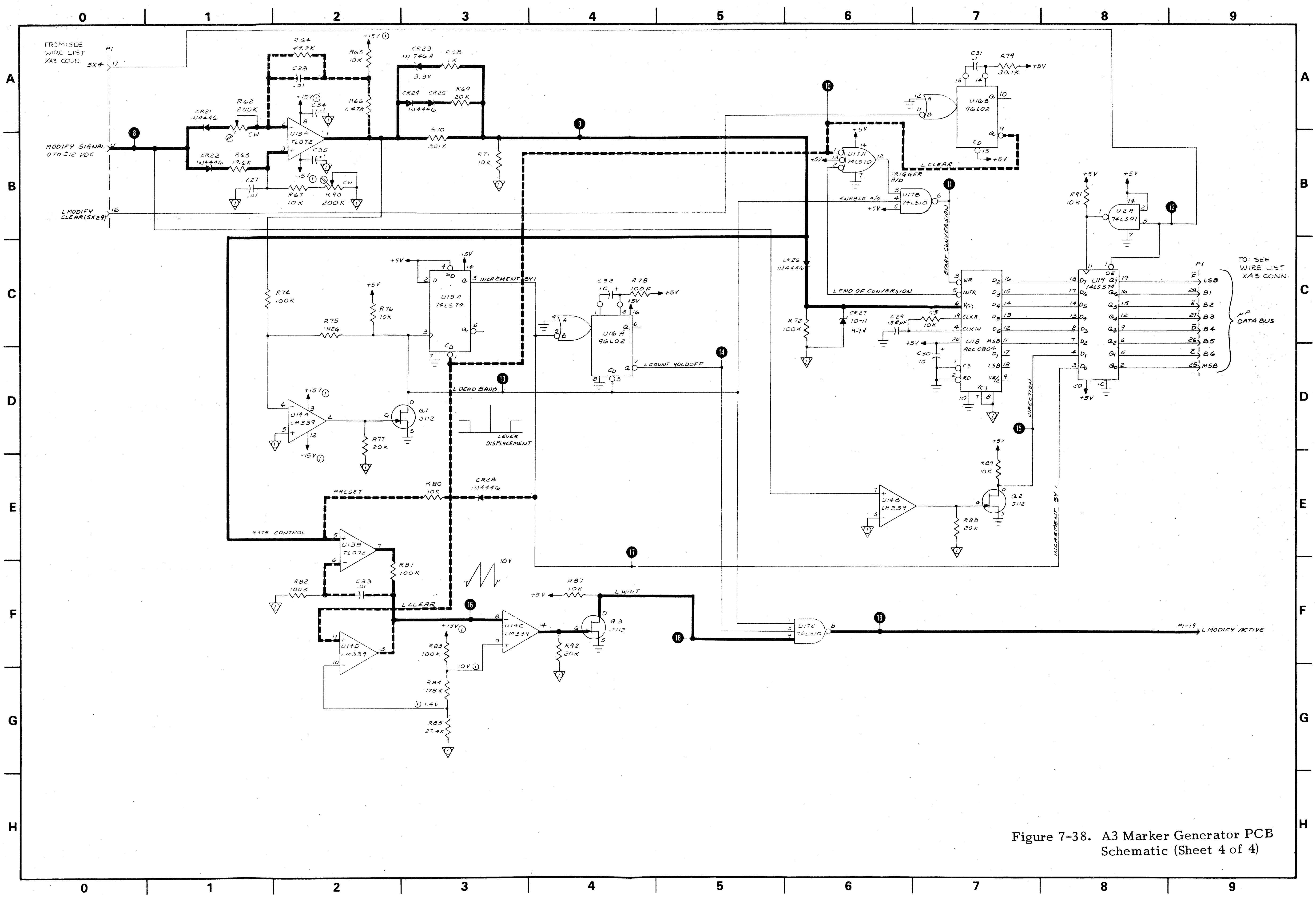


Figure 7-38. A3 Marker Generator PCB Schematic (Sheet 4 of 4)

7-10.2 A3 Marker Generator PCB, Troubleshooting Information and Data

Error Code 22 reports on the status of the A3 Marker Generator PCB. The microprocessor routine associated with this error code performs the A3 PCB test in the following manner:

a. It positions the A3 marker frequencies as follows:

   1. M1 to a frequency point equal to 25% of the sweep width.

   2. F0 to a frequency point equal to 50% of the sweep width.

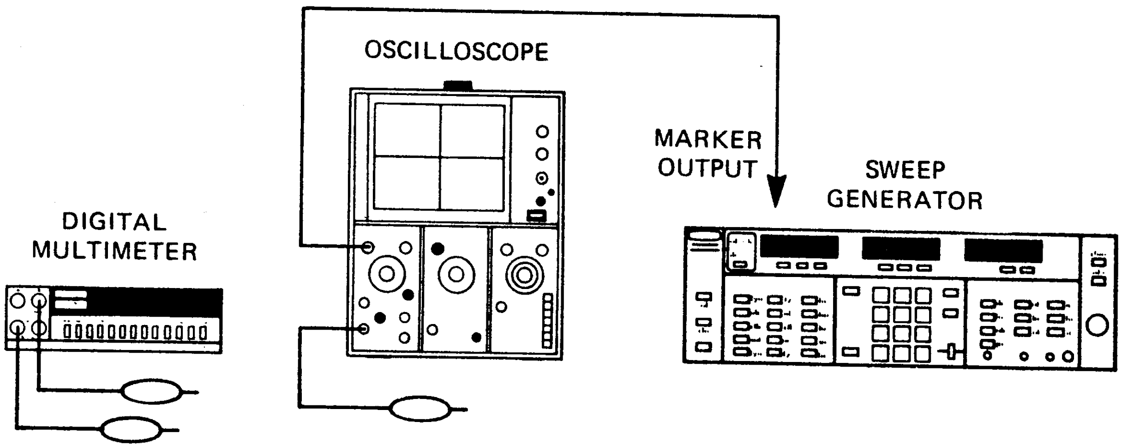
   3. M2 to a frequency point equal to 75% of the sweep width.

b. It selects the Intensity Markers on A3, the A2 Sweep Ramp on A5, and CW Filter Out on A5.

c. It sets the A2 sweep ramp for an 8 ms sweep and selects AUTO triggering.

d. It counts the markers during the forward-sweep period; if three markers are not counted, the routine causes "Error 22" to be displayed.

The test setup for troubleshooting Error Code 22 is provided in Figure 7-39, the troubleshooting flowchart is in Figure 7-40, and the troubleshooting block diagram is in Figure 7-41.



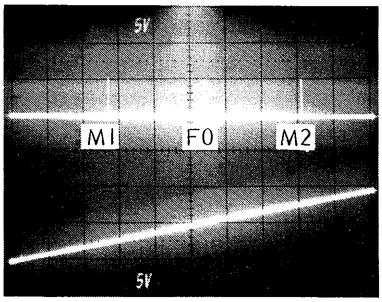
Sweep Generator Control Settings

FREQUENCY RANGE: FULL
TRIGGER: AUTO
MARKERS: VIDEO
LEVELING: INTERNAL
MARKER AMPLITUDE: Fully CW
LEVEL: 0 dBm
SWEEP TIME: 10 ms

RETRACE RF: ON
RF ON: ON
RF SLOPE: OFF
M1: 5 GHz
F0: 10 GHz
M2: 15 GHz

Figure 7-39. Test Equipment for Troubleshooting Error Code 22

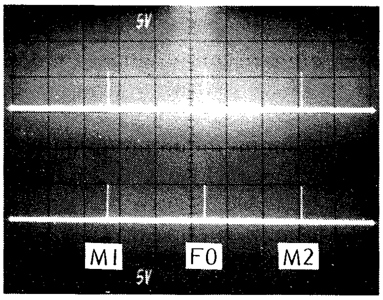
A



MARKER
OUTPUT

TP6

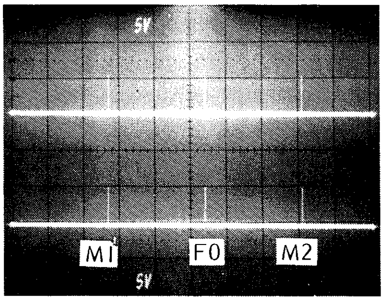
B



MARKER
OUTPUT

TP7

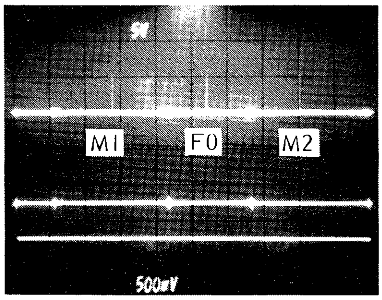
C



MARKER
OUTPUT

XA3,
Pin 8

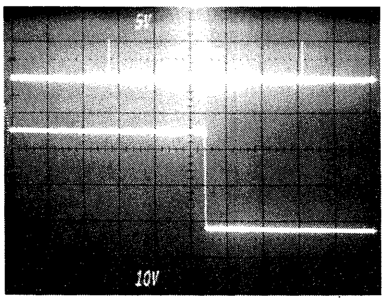
D



MARKER
OUTPUT

XA3,
Pin 18

E



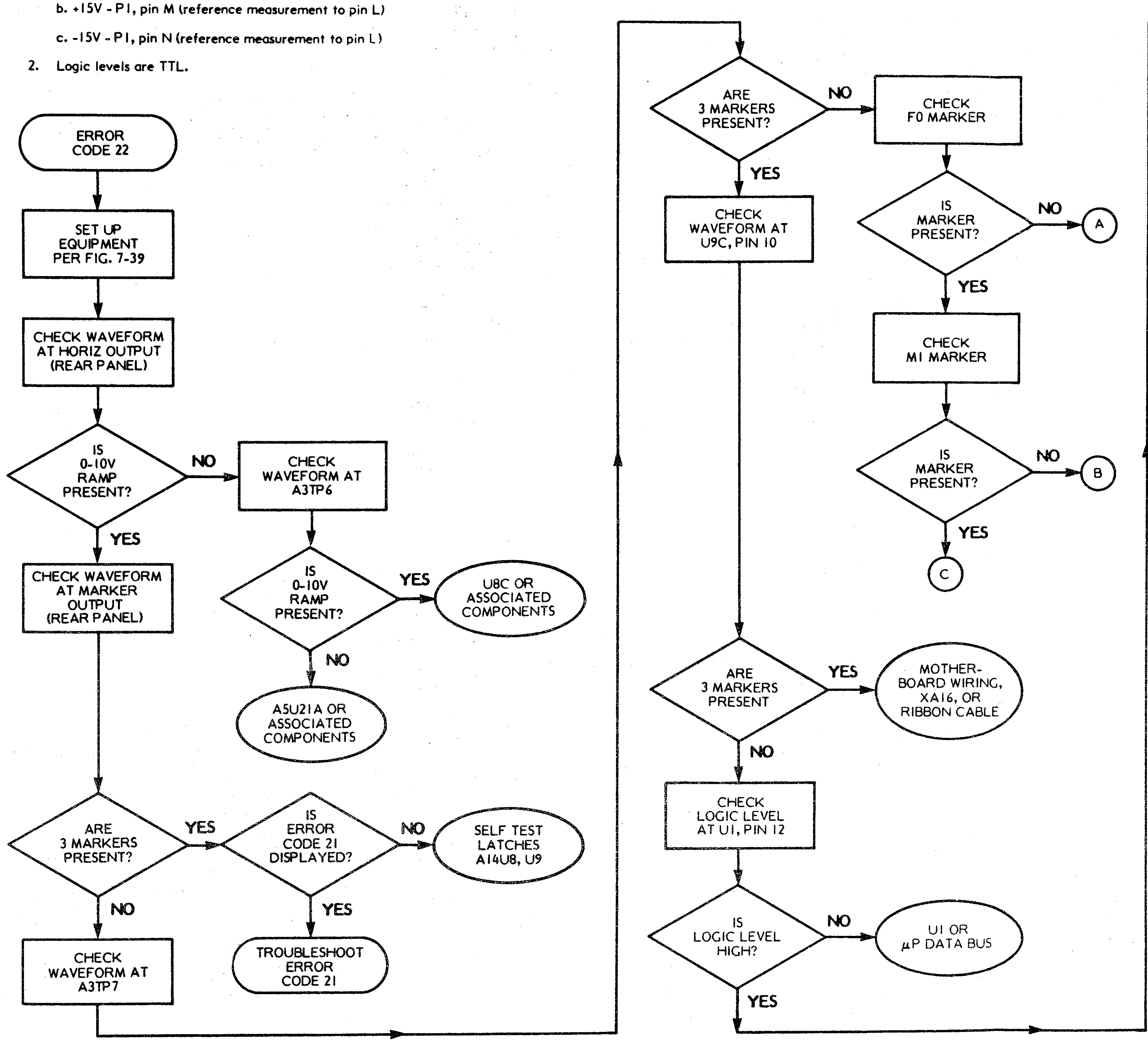
MARKER
OUTPUT

U8D,
Pin 12

A3 Marker Generator PCB Waveforms (part of Figure 7-40)

GENERAL INSTRUCTIONS

1. Check the following dc voltages before starting the flowchart:
   a. +5V - P1, pins R(+) and P(-)
   b. +15V - P1, pin M (reference measurement to pin L)
   c. -15V - P1, pin N (reference measurement to pin L)
2. Logic levels are TTL.



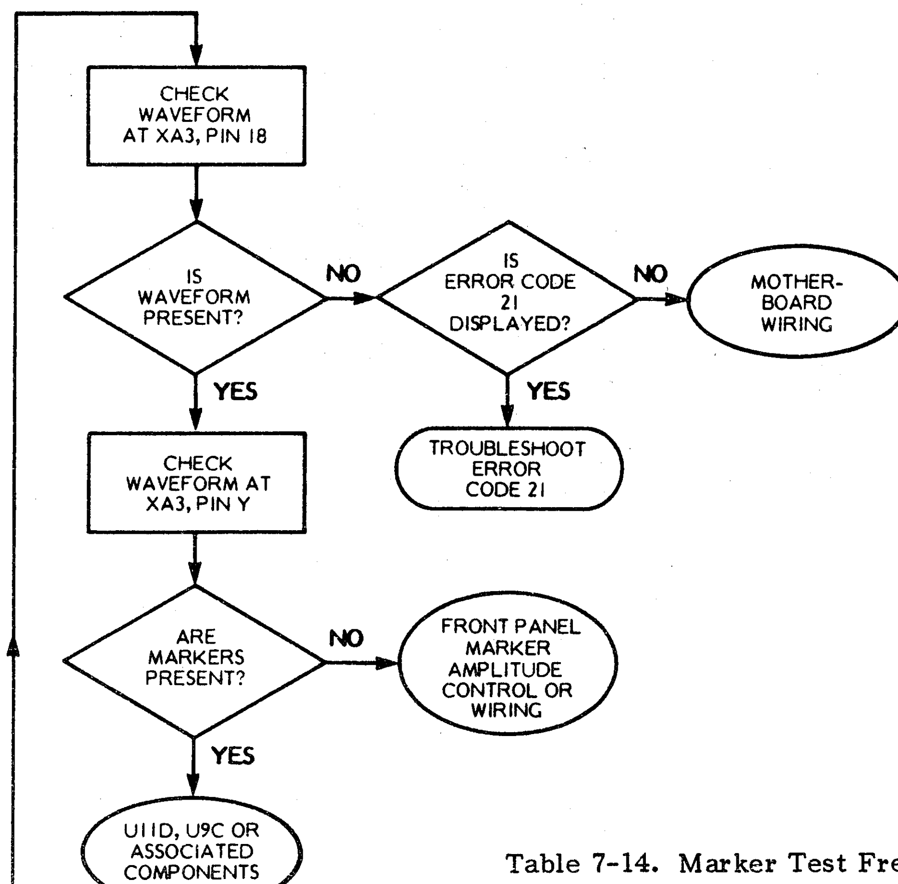
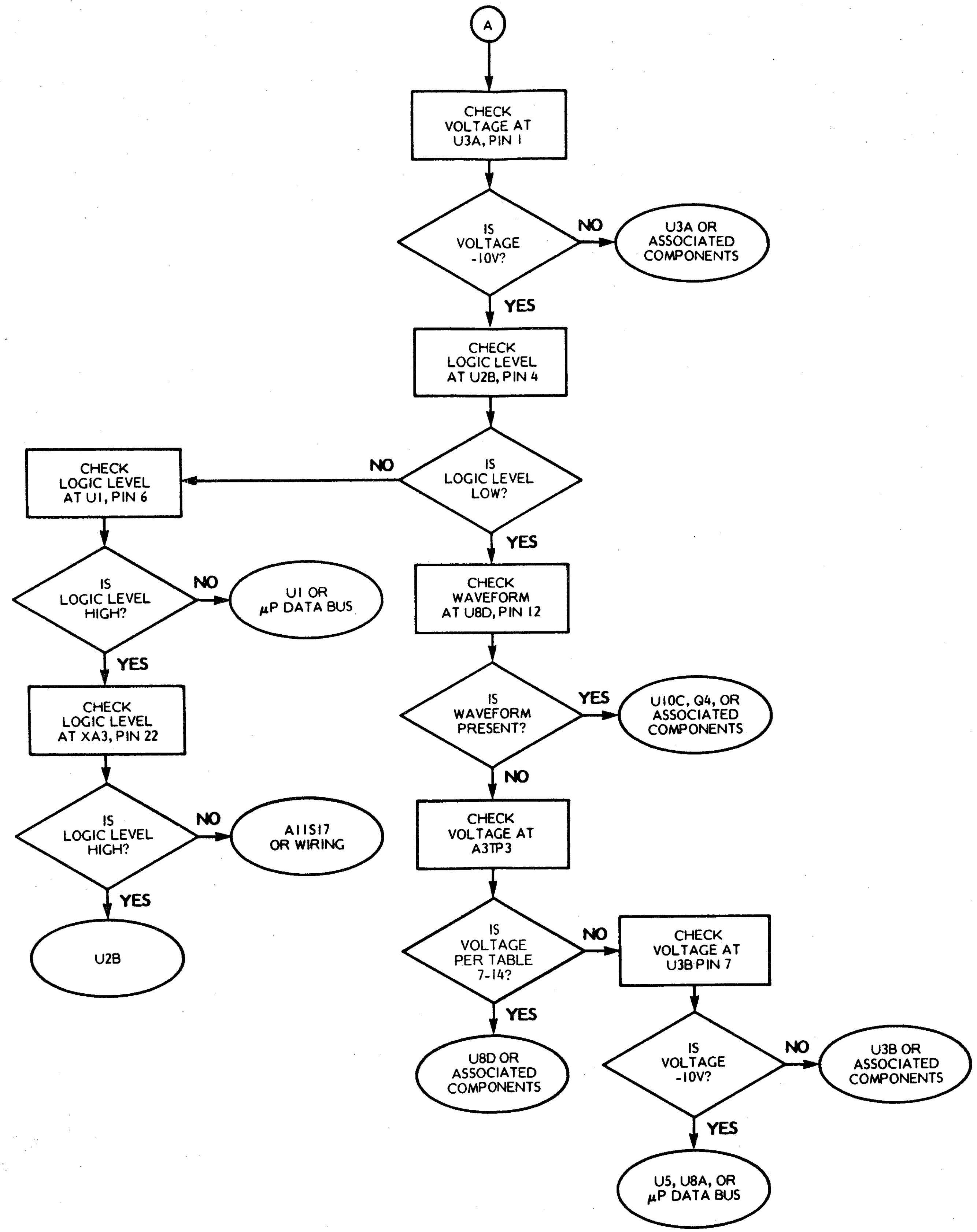


Figure 7-40. Error Code 22 Troubleshooting Flowchart (Sheet 1 of 3)

Table 7-14. Marker Test Frequencies (GHz)

MODEL	M1 DAC 2.5V	F0 DAC 5.0V	M2 DAC 7.5V
6609A	0.508	1.005	1.503
6617A	2.008	4.005	6.003
6621A/6621A-40	4.600	7.200	9.800
6629A/6629A-40	10.650	13.300	15.950
6637A/6637A-40	6.150	10.300	14.450
6638A	6.500	11.000	15.500
6642A	23.500	29.000	34.500
6647A	4.658	9.305	13.953
6648A	5.008	10.005	15.003
6653A	6.633	13.255	19.878
6659A	8.125	14.250	20.375

Formula: $V_{DAC} = 10\left(\frac{F_{Mkr} - F_{Start}}{F_{Stop} - F_{Start}}\right)$



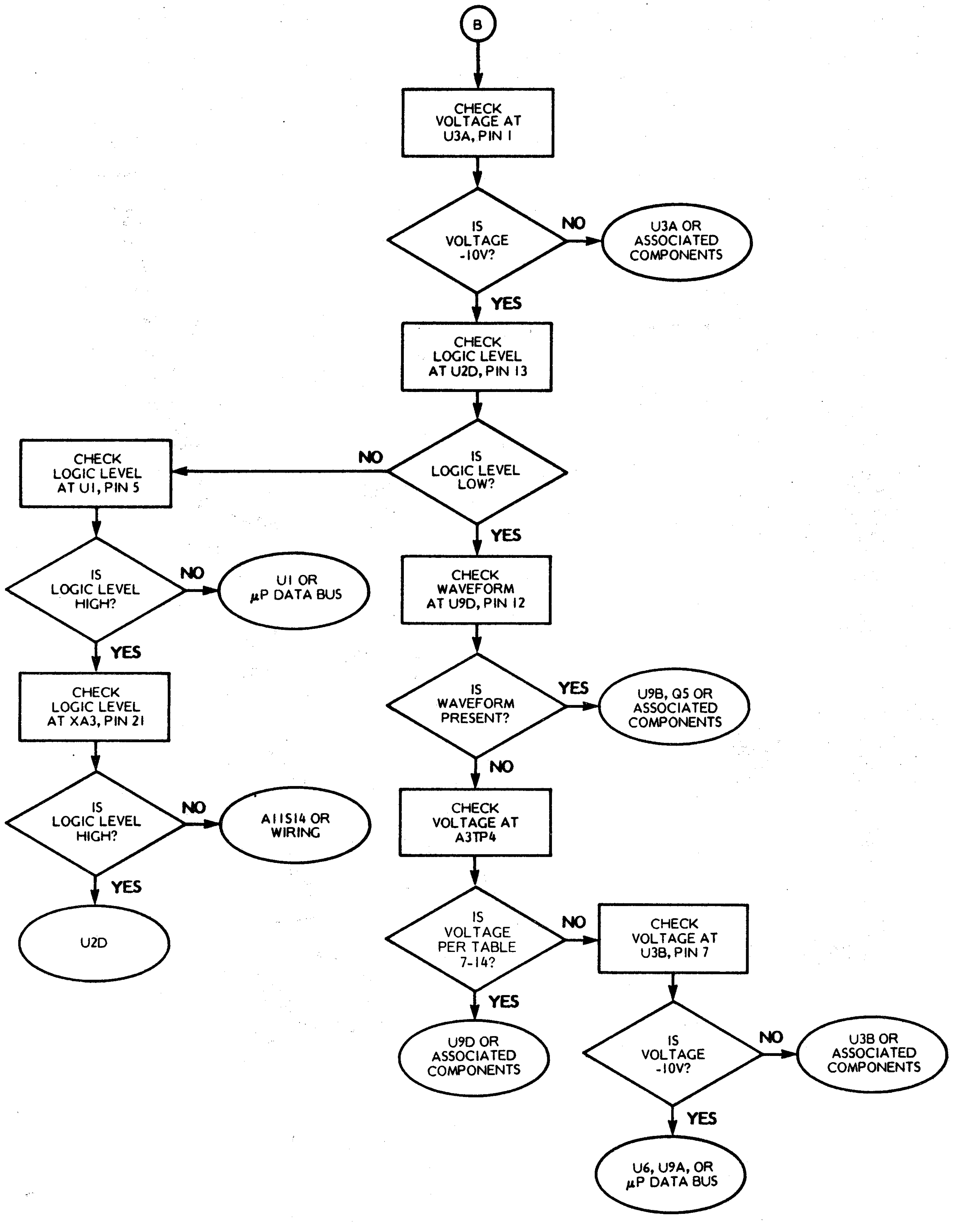


Figure 7-40. Error Code 22 Troubleshooting Flowchart (Sheet 2 of 3)

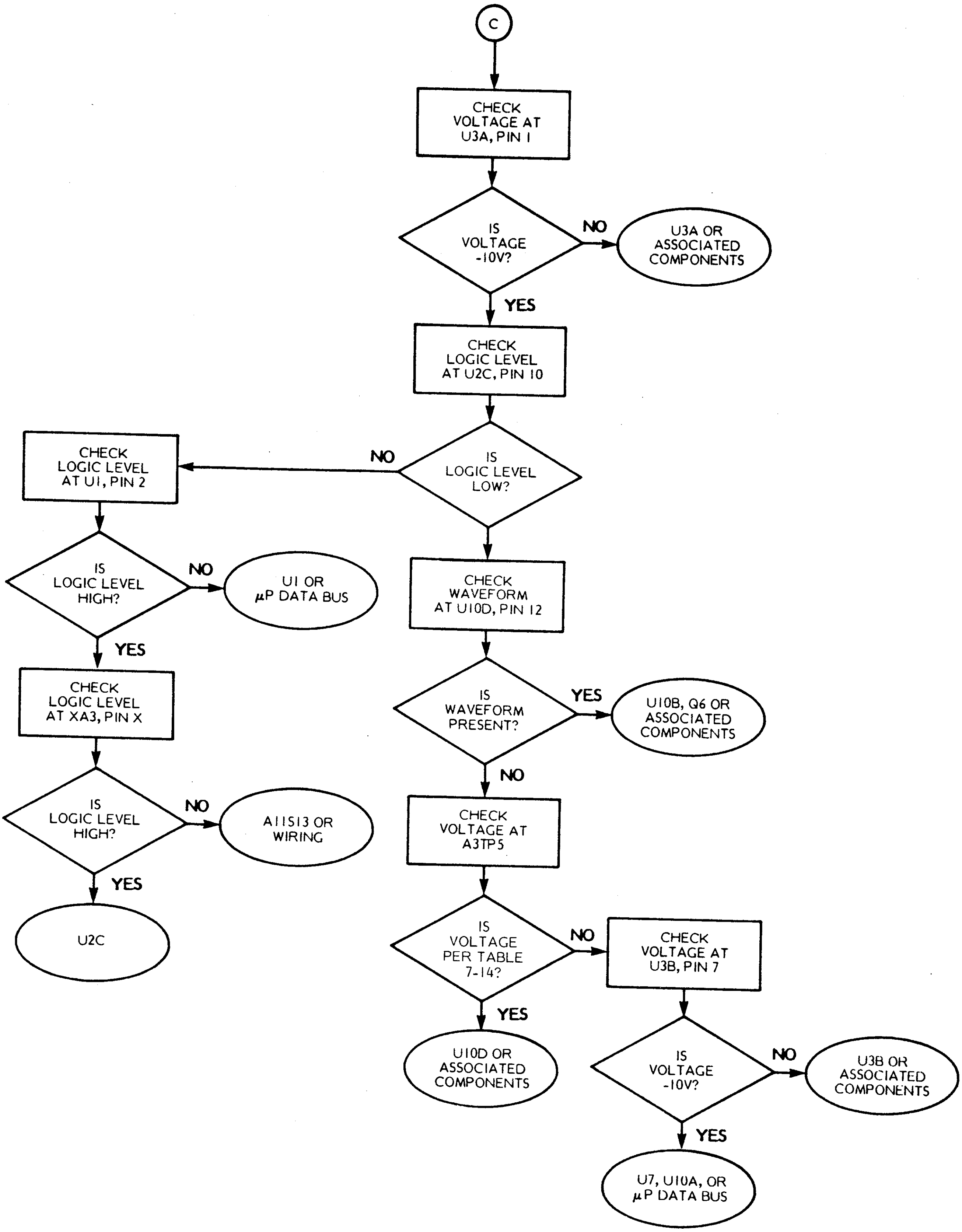


Figure 7-40. Error Code 22 Troubleshooting Flowchart (Sheet 3 of 3)

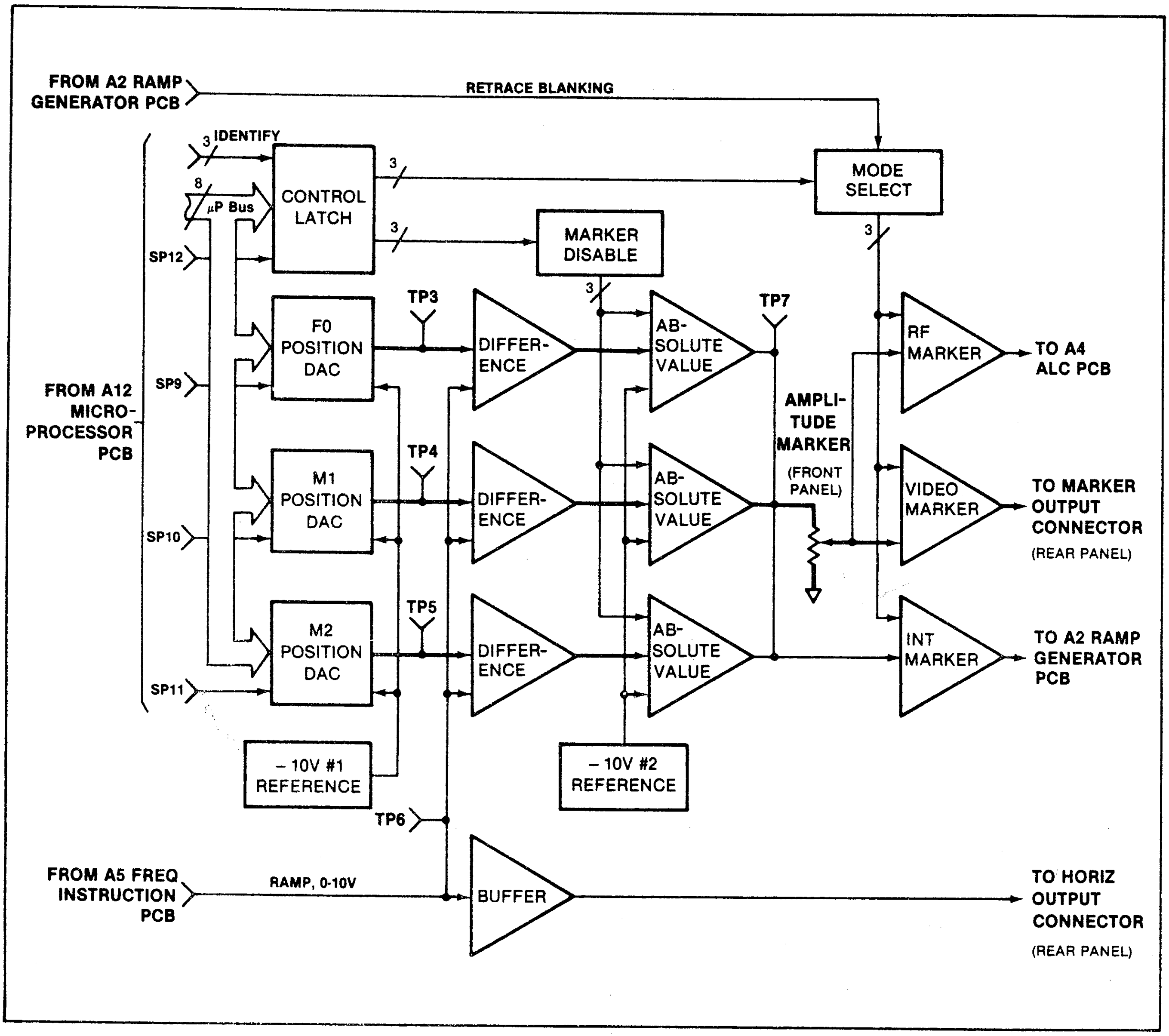


Figure 7-41. Error Code 22 Troubleshooting Diagram

7-11 A4 AUTOMATIC LEVEL CONTROL (ALC) PCB

7-11.1 A4 Automatic Level Control (ALC) PCB, Circuit Description

The A4 Automatic Level Control (ALC) PCB, along with circuitry on the RF Deck and the YIG Driver PCB (A6, A7, A8, or A9), provides for the automatic leveling of the RF output power. The A4 PCB also receives the ATTN 1 thru ATTN 4 control bits from the microprocessor and routes these bits to the Option 2 Step Attenuator current-driver circuits on the A10 PCB. The schematic diagram for the A4 PCB (3 sheets) is contained in Figure 7-44.

The sweep generator ALC loop (Figure 7-42) consists of the following circuits and components:

a. PIN Switch and RF Coupler/Detector. These components are on the RF Deck.

b. PIN Driver/Linearizer circuits. These circuits are on the individual A6, A7, A8, and A9 YIG Driver PCBs.

c. Preamp (3), Absolute Value, Ext Gain Compare, Log Amp/Shaper, Latch/DAC, Level Amp, Compensation, and Unlevel Compare circuits. These circuits are on the A4 PCB.

As shown in Figure 7-42, the output from the RF Oscillator is applied to the RF Coupler/Detector via the PIN Switch. A sample of the RF power signal, attenuated by approximately 16 dB, is coupled to the RF detector. If internal leveling has been selected, the detector output signal is applied

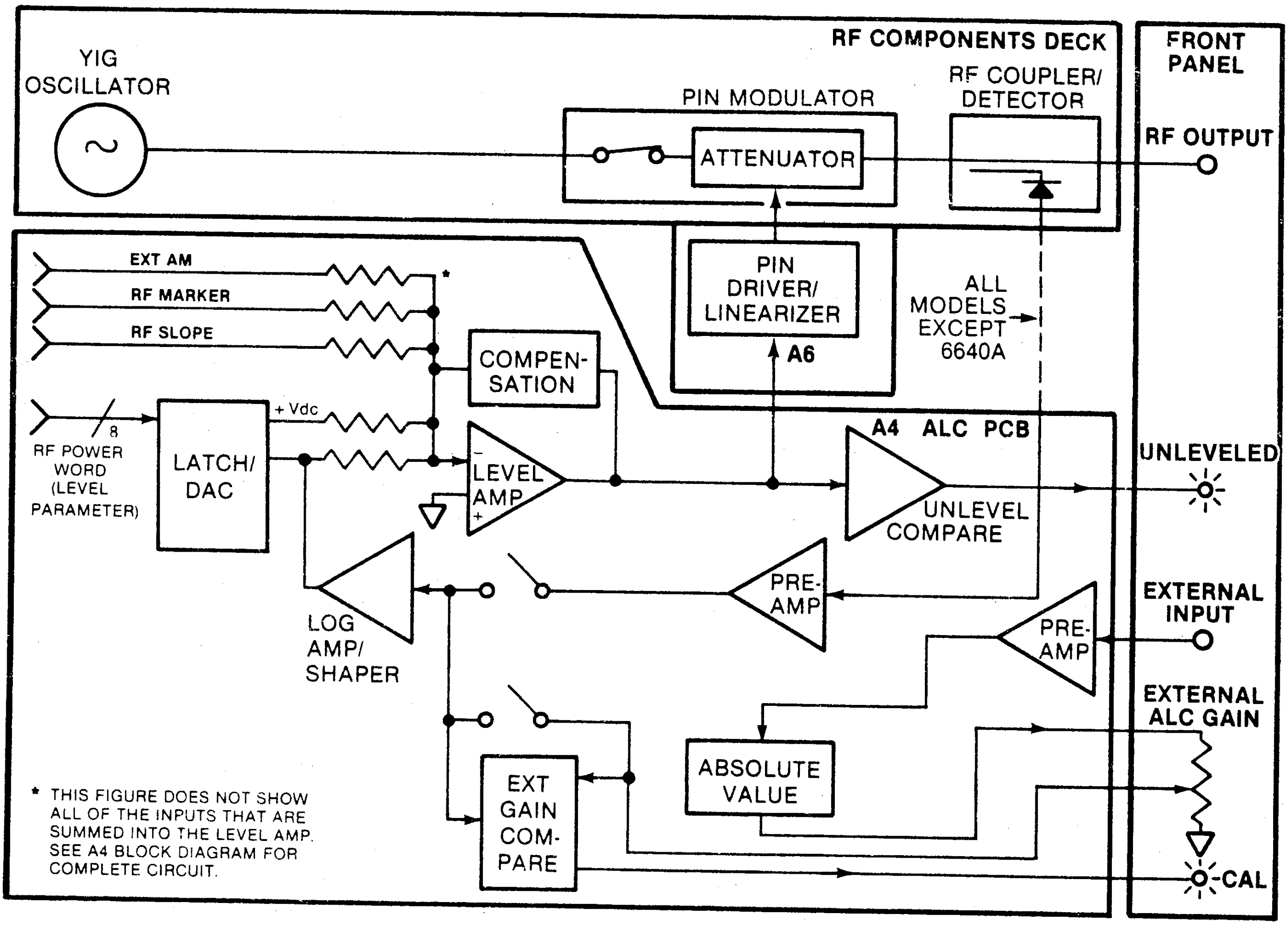


Figure 7-42. Sweep Generator Overall Leveling Loop

to the Log Amp/Shaper via the appropriate Preamp circuit. If external leveling has been selected, the external detector output signal is applied to the Log Amp/Shaper via the Absolute Value circuit.

At the Log Amp/Shaper, the detector output signal is amplified and shaped and its relationship to the main power signal is changed from logarithmic to linear. The linear-change-with-power-level-change output from the Log Amp/Shaper is summed at the Level Amp with the voltage output from the Reference DAC. The output from the DAC is the analog voltage representation of the digital power word that was selected using the front panel LEVEL pushbutton. Another reason for including a log amplifier in the ALC loop is to provide the loop with the means for setting output power in dBm.

The output of the Level Amp is applied to either the A6, A7, A8, or A9 PCB PIN Driver/Linearizer circuit (depending on which YIG oscillator band is supplying the output power). The A6, A7, A8, and A9 PIN Driver/Linearizer circuits provide an adjustment for customizing the loop gain for each YIG oscillator band.

The A4 PCB leveling circuit (Figure 7-43) provides overall control of the RF output power. The A4 PCB has two preamplifiers for internal leveling: a Het Band (U4) and YIG Band(s) circuit (U6).

For external leveling, both a preamplifier (U7) and an Absolute Value circuit (U8A, U8B) are provided. The Absolute Value circuit allows a positive or negative detector to be used for external leveling; the circuit's output is positive for either input sense. If POWER METER leveling has been selected, the L **PWR MTR GAIN** control line is TRUE. When TRUE, this line activates a switch that causes the circuit gain to be reduced to accommodate the larger voltage supplied by the power meter video output.

The Ext Gain Comparator circuit (U11A, U11B), in conjunction with the front panel EXTERNAL ALC GAIN control, provides for calibrating the gain of the external leveling loop. When the EXTERNAL ALC GAIN control is pushed in, the microprocessor causes either the L **<2 GHz** or the L **>2 GHz** line to go TRUE (depending upon the frequency range that has been selected). Either of these lines going TRUE places its associated detector signal on the Ext Gain Comparator's comparison input. With this signal in place, the EXTERNAL ALC GAIN control is adjusted until the voltage of the external detector is equal to the voltage of the internal detector. When these two voltages are equal, the L **EGD** (External Gain Detected) line will go TRUE and light the CAL indicator LED. The CAL indicator will remain lit until the EXTERNAL ALC GAIN control is released and control is restored to the external signal path.

The output signal from the external or internal preamplifier circuit is applied to the Log Amp/Shaper circuit (Figure 7-44, Sheet 2). The Log Amp/Shaper, with its associated temperature compensation and voltage offset circuits, provides gain and shaping for its signal.

The Level Amp (U21) and its associated input circuitry gives the A4 PCB overall control over the level of the sweep generator output-power signal. In addition to the Log Amp, the Level Amp input circuitry consists of the following:

a. <u>DAC Circuit</u>. This circuit (U22, U19B) converts the 8-bit digital-power-level control group from the microprocessor into an analog reference voltage. This voltage is used to set the sweep generator output power level. The microprocessor digital word represents the dBm value that was set using the front panel LEVEL pushbutton.

b. <u>Level-Dip Logic Circuit</u>. This circuit (Q2) causes the PIN Switch Attenuator (Figure 7-42) to go to maximum attenuation ("dip" RF power) when any of the following occurs:

   1. The L **LEVEL DIP** line from the A2 PCB goes TRUE (paragraph 7-9.1b).

   2. The L **RETRACE BLANKING** line from the A2 PCB goes TRUE (provided the front panel RETRACE RF switch is OFF).

Para 7-11.1 (cont'd.)

3. The front panel RF OFF switch is switched off.

When any of the above three conditions occurs, the Level-Dip Logic circuit output goes HIGH and causes the PIN Switch Attentuator to go to maximum attenuation. The L CW MODE line that also connects to this circuit prevents a dip in power when the sweeper is in a CW mode and the rear panel HORIZ OUTPUT DURING CW switch is ON.

c. RF MARKER Signal Line. This input is the 0 to +5V triangular waveform from the A3 Marker Generator PCB (paragraph 7-10.1a). This waveform causes the output power to "dip" up to 5 dB at the marker frequency, depending on the setting of the MARKER AMPLITUDE control.

d. RF SLOPE Control. This input is from the front panel RF SLOPE control. It provides a linear boost in output power as the RF oscillator sweeps across its frequency band. The RF SLOPE input is a negative-going voltage ramp that is proportional to frequency; it provides an increase in output power at the higher frequencies.

e. Slope Calibrate Circuit. This circuit (U19D) calibrates the sweep-frequency output to be optimally horizontal when the RF SLOPE control is OFF. The input to this circuit is a 0 to 10V ramp from the A5 PCB. The output of the circuit can be either a positive or a negative analog voltage, the value of which is proportional to frequency.

f. EXT AM INPUT Connector. This input is from the EXT AM INPUT rear panel connector. This modulation signal is inverted and summed into the Level Amp. Its bandwidth is rated from dc to 50 kHz; signal sensitivity is 1 dB/V.

g. Sq Wave Sample/Hold Logic Circuit. This circuit (Q3, U2C, U1D, U23A, U23B, U2F, U23C, U23D, U20B) provides for square wave modulation of the RF output signal, at rates up to 30 kHz. The inputs to this circuit are the **EXT SQ WAVE IN** signal from the rear panel connector and the **L RF OFF DURING RETRACE** control line from NAND gate U1A. When the **EXT SQ WAVE IN** signal goes negative or when the **L RF OFF DURING RETRACE** line goes TRUE, the **L PIN SW OFF** line goes TRUE and opens the PIN Switch (Figure 7-42). When open, the PIN Switch attenuates the RF output signal by ≈ 40 dB. When the EXT SQ WAVE IN signal again goes positive (or **L RF OFF DURING RETRACE** goes FALSE), the **L PIN SW OFF** line goes FALSE and closes the PIN switch. The ALC loop cannot respond fast enough to track the changes in RF output during square-wave modulation. Therefore, a sample-and-hold network is used to open the ALC loop and hold the previous PIN switch drive current when modulation is applied.

The two remaining blocks on this diagram are the Compensation and the Unlevel Comparator circuits. The Compensation circuit (C23, CR13) is used to stabilize the loop. The circuit also slows the response of the ALC loop when power meter leveling has been selected. Slowing the loop's response is necessary because a power meter's response to variations in output power is much slower than a detector's response.

The Unlevel Comparator circuit (U11D) provides drive for the front panel UNLEVEL indicator LED. If the output of the Level Amp goes positive, indicating more power has been called for than the YIG oscillator can deliver, the H **UNLC** line goes TRUE and lights the UNLEVEL indicator LED.

:ircuit. This
U23B, U2F,
s for square
utput signal,
nputs to this
/E IN signal
or and the L
control line
the **EXT SQ**
or when the
CE line goes
e goes TRUE
'igure 7-42).
tenuates the
. When the
n goes posi-
RETRACE
FF line goes
switch. The
t enough to
utput during
'herefore, a
used to open
previous PIN
modulation is

diagram are
el Compara-
circuit (C23,
loop. The
of the ALC
ng has been
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much slower

(U11D) pro-
l UNLEVEL
of the Level
re power has
scillator can
TRUE and
D.

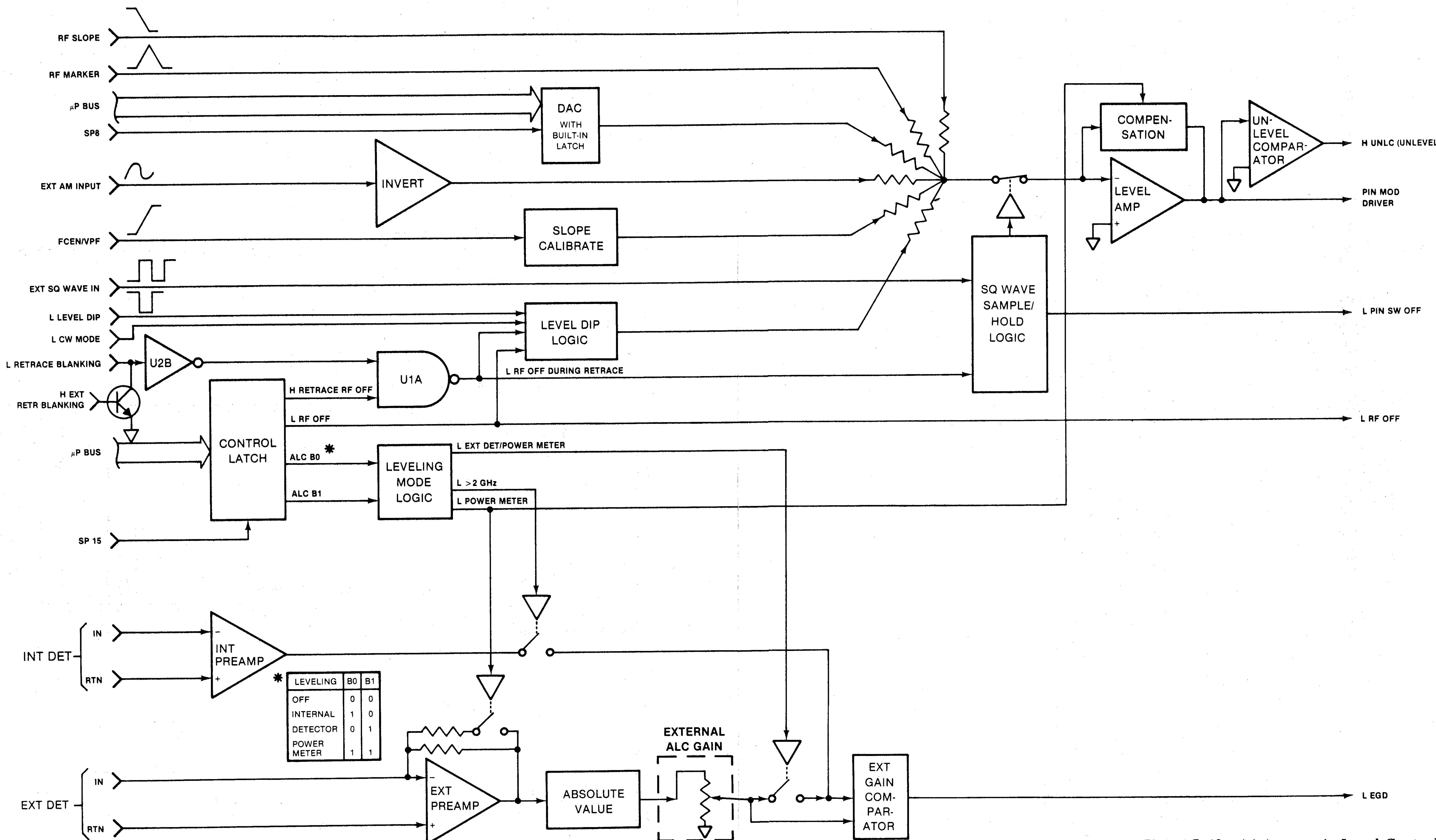
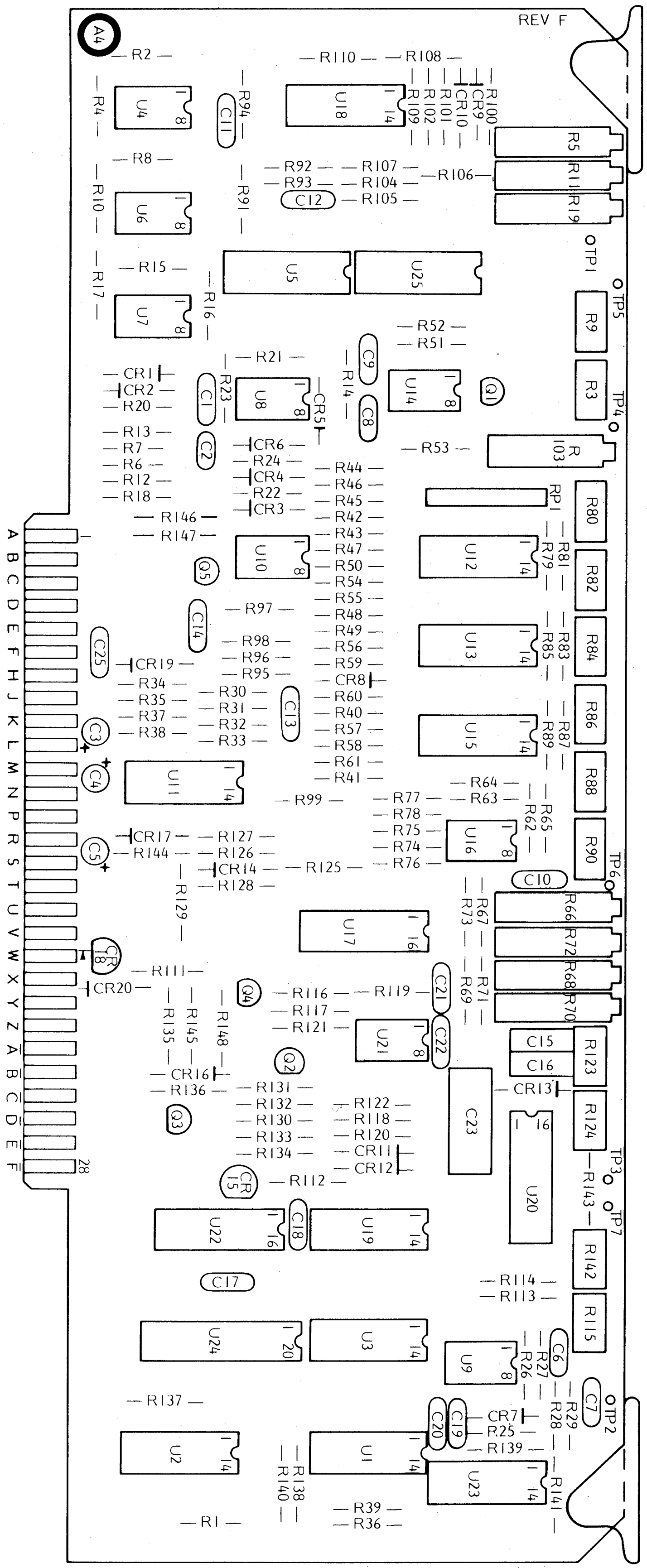


Figure 7-43. A4 Automatic Level Control (ALC) PCB Functional Block Diagram



A4 PCB Parts Locator Diagram

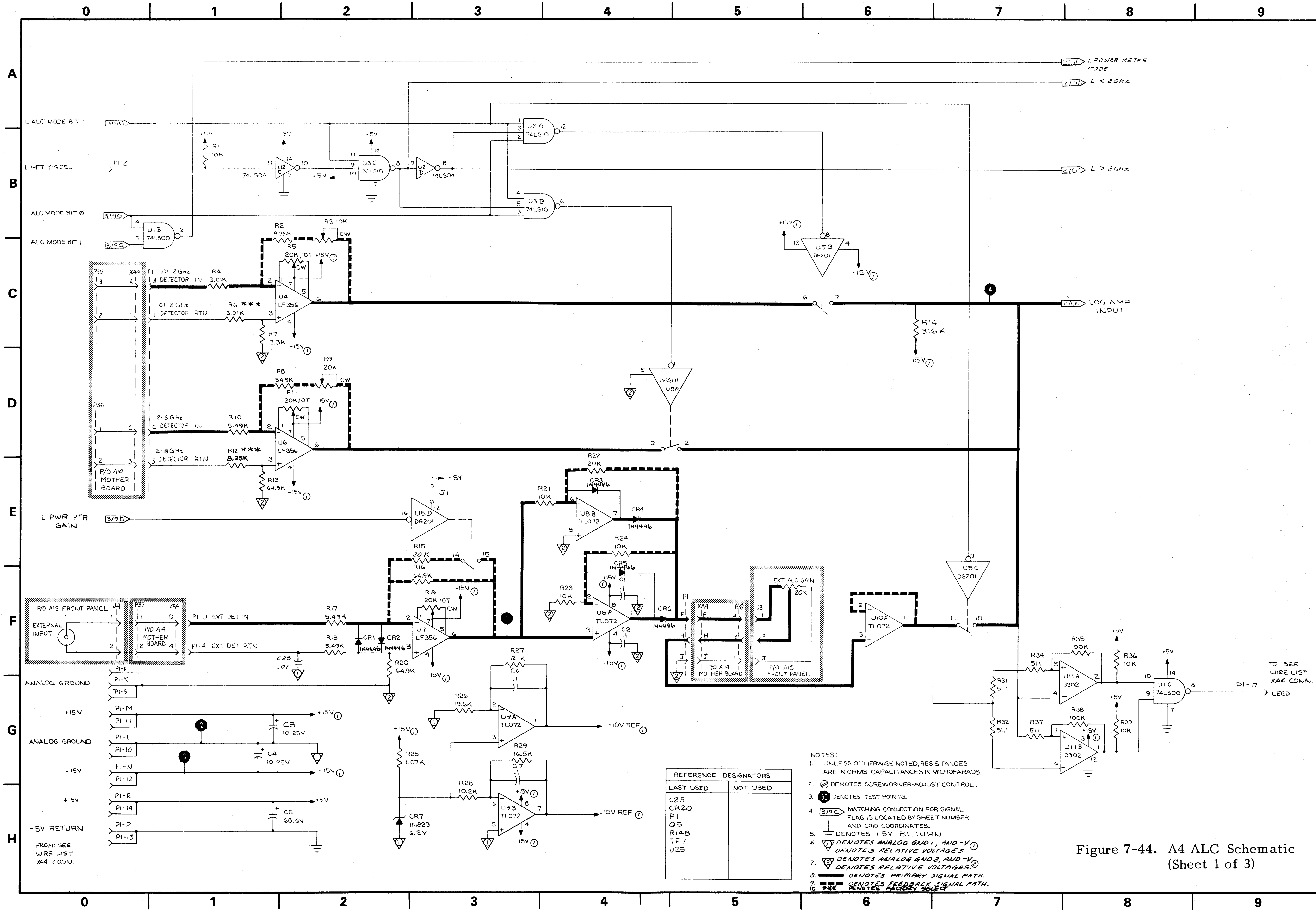


Figure 7-44. A4 ALC Schematic (Sheet 1 of 3)

parts locator

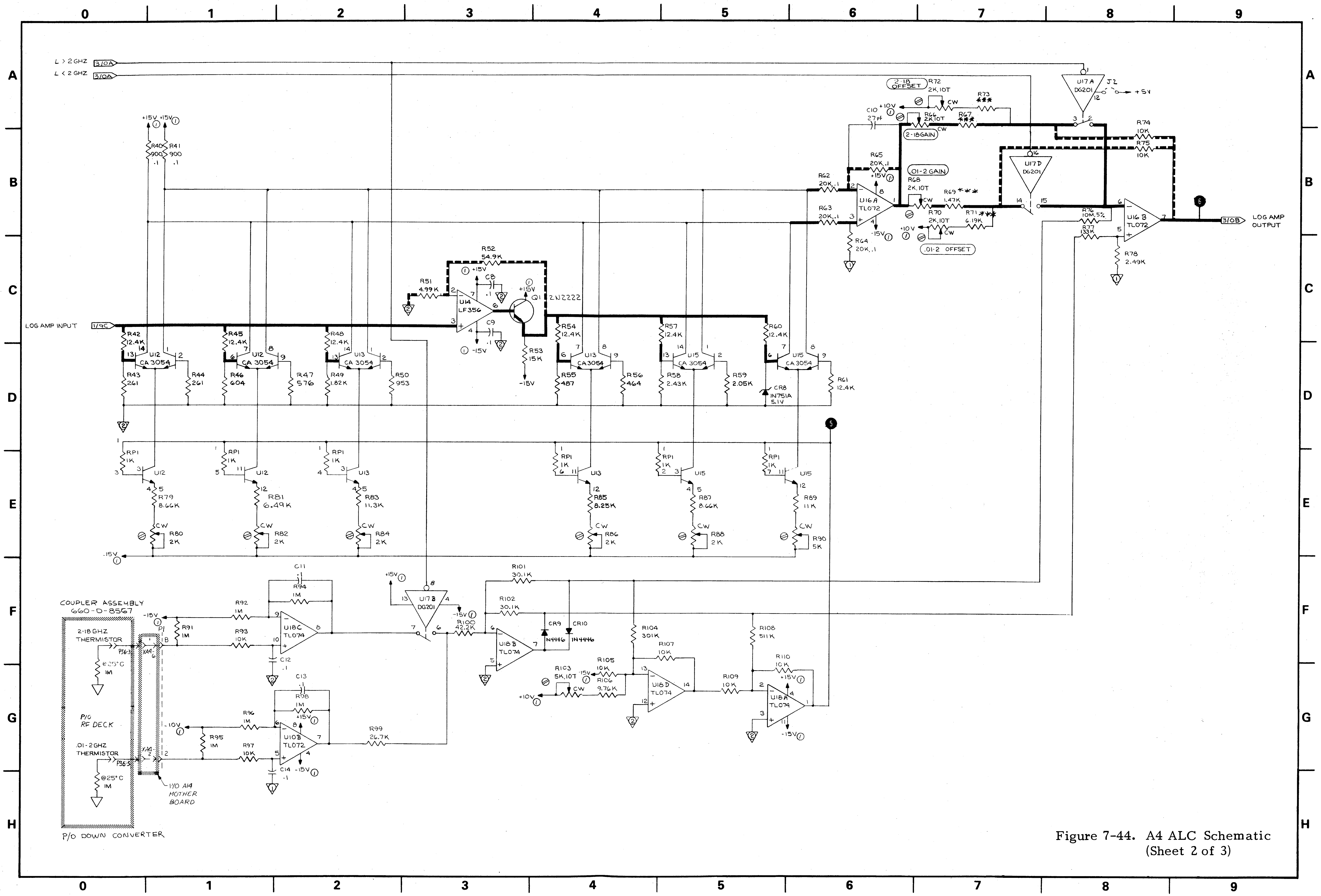


Figure 7-44. A4 ALC Schematic (Sheet 2 of 3)

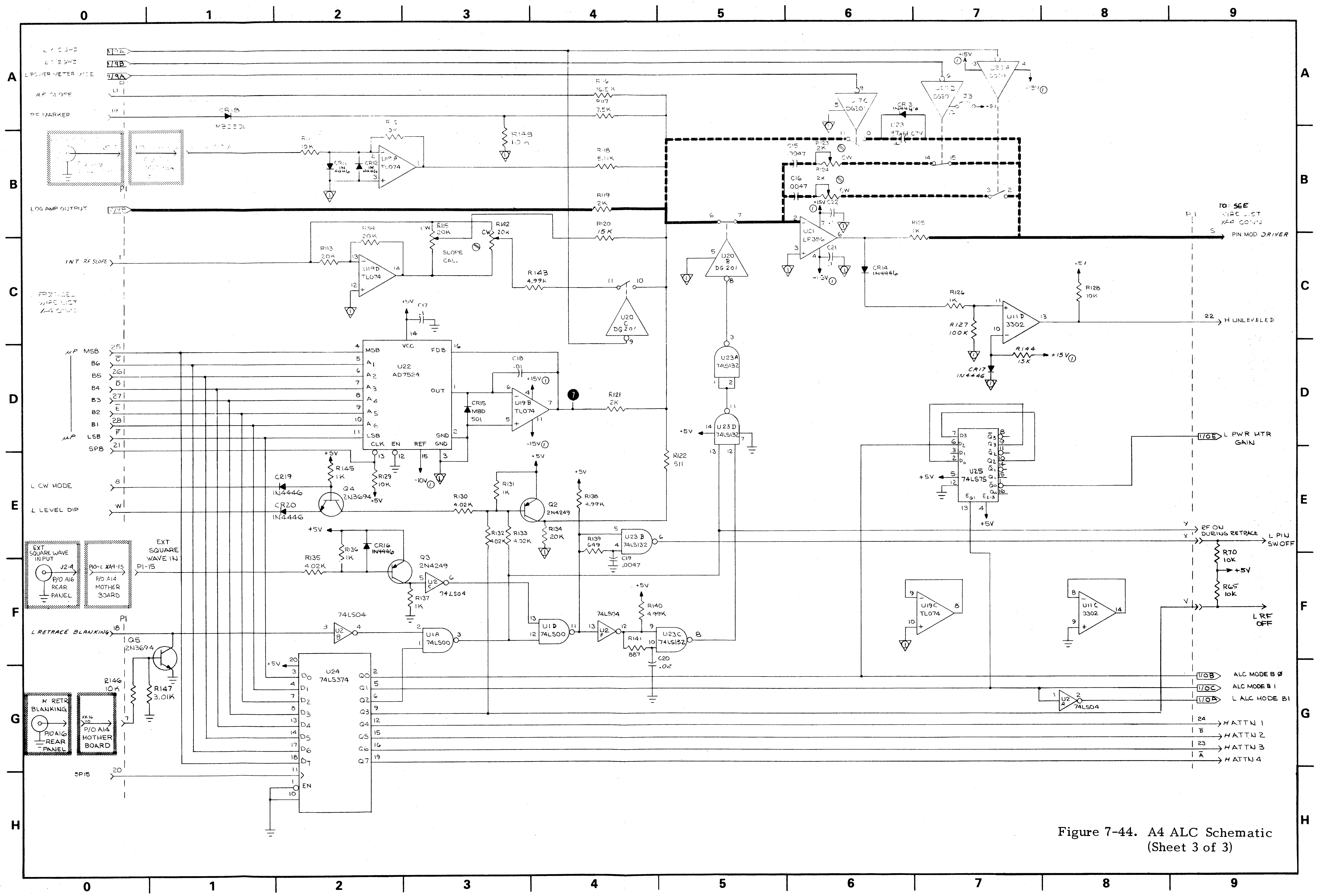


Figure 7-44. A4 ALC Schematic (Sheet 3 of 3)

7-11.2 Sweep Generator Automatic-Leveling-Control (ALC) Loop, Troubleshooting Information and Data

Error codes 15-20 report on the automatic leveling control (ALC) loop. The microprocessor routines associated with these codes monitor the front panel UNLEVEL indicator (H UNL status line). If UNLEVEL is lit

- in the heterodyne (Het) band, error code 15 appears;
- in the YIG 1 band, error code 16 appears;
- in the YIG 2 band, error code 17 appears;
- in the YIG 3 band, error code 18 appears;
- in the YIG 4 band, error code 19 appears;
- anywhere across the range, error code 20 appears.

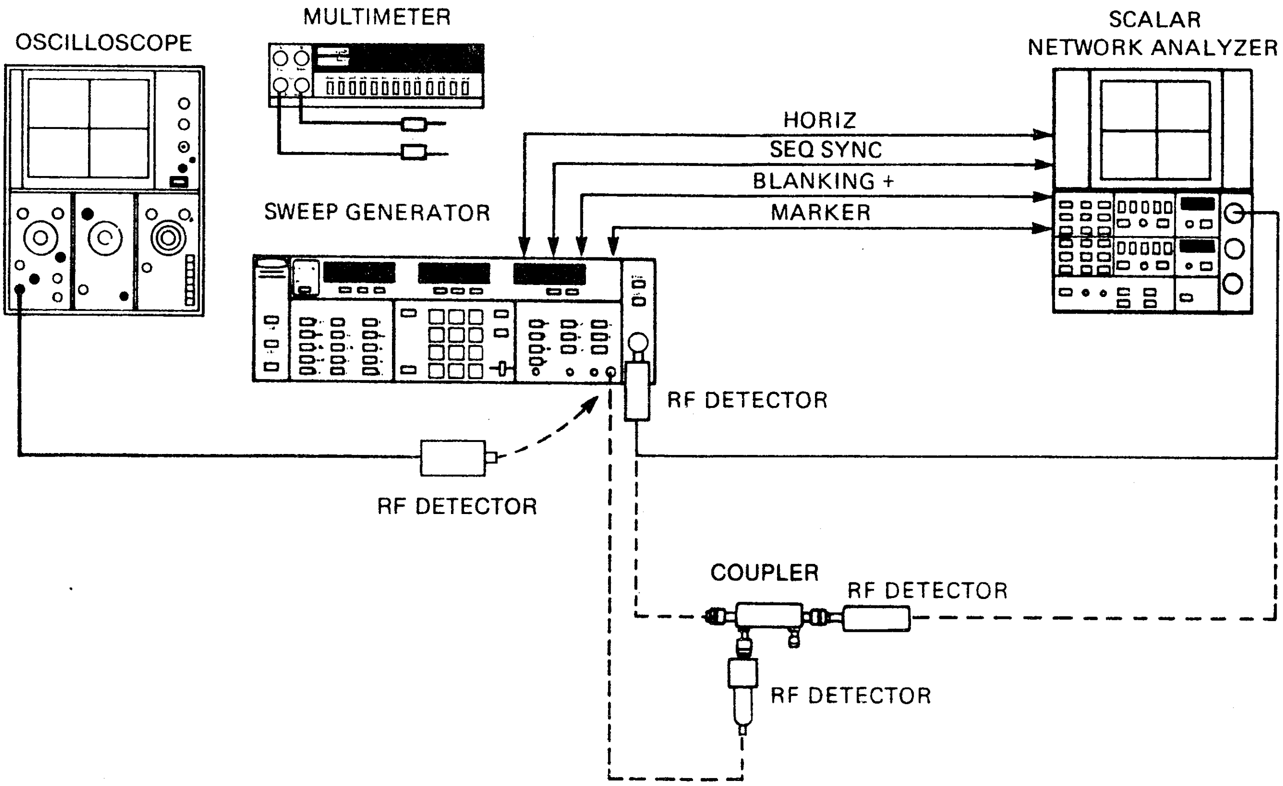
To test the ALC loop, the error code routines function as follows: The routines for error codes 15 thru 19 call up CW operation and set their band to midfrequency. The routine for error code 20 calls up the analog (A2 PCB) sweep ramp and causes it to sweep the frequency across 95% of its entire range. Because of this test method, a band error code (15-19) should always result in a range error code (20) also. However, because power may not always be unlevel in the middle of a band, the range error code can occur independently of a band error code.

To accomplish the ALC error-code tests, the microprocessor configures the ALC loop circuits as follows:

ERROR CODE	MODEL	F CENTER DAC FREQ. (APPROX.)
15	6609A, 6617A 6647A, 6648A, 6653A	1 GHz
16	6617A, 6621A, 6621A-40, 6629A, 6629A-40, 6637A, 6637A-40, 6638A, 6647A, 6648A, 6653A, 6659A	5 GHz
16	6642A	22 GHz
17	6621A, 6621A-40, 6629A, 6629A-40, 6637A, 6637A-40, 6638A, 6647A, 6648A, 6653A, 6659A	10 GHz
18	6629A, 6629A-40, 6637A, 6637A-40, 6638A, 6647A, 6648A, 6653A, 6659A	15 GHz
19	6653A, 6659A	23 GHz
20	6609A	1 GHz
	6617A	5 GHz
	6621A, 6621A-40	7 GHz
	6629A, 6629A-40	13 GHz
	6637A, 6637A-40, 6647A	9 GHz
	6638A, 6648A	10 GHz
	6653A, 6659A	13 GHz
	6642A	29 GHz

All of the ALC error-code routines monitor the **H UNLEVELED** line at the microprocessor input buffer. If this line goes LOW, the appropriate error code is displayed.

The test equipment setup for troubleshooting error codes 15-20 is provided in Figure 7-45; a test setup for troubleshooting the 6642A 26.5 to 40 GHz band is provided in Figure 7-46; a troubleshooting flowchart is provided in Figure 7-47, and individual troubleshooting block diagrams are provided in Figure 7-48 through 7-55. ALC loop waveforms are shown in Figure 7-56, and a tabulation giving minimum output power (YIGs) and insertion loss values for the RF components is provided in Table 7-16.



Initial Control Settings

Sweep Generator

FREQUENCY RANGE: F1-F2
TRIGGER: AUTO
MARKERS: INTENSITY
LEVELING: INTERNAL (DETECTOR*)
RETRACE RF: Off
RF ON: On
CW RAMP: On
RF SLOPE: OFF
LEVEL: 0 dBm
SWEEP TIME: 50 ms
F1: 10 MHz (Error Code 15, not 6642A)
18 GHz (Error Code 15, 6642A)
2 GHz (Error Code 16)
8 GHz (Error Code 17)
12.4 GHz (Error Code 18)
18 GHz (Error Code 19)
Low End (Error Code 20)

F2: 2 GHz (Error Code 15 not 6642A)
26.5 GHz (Error Code 15, 6642A)
8 GHz (Error Code 16)
12.4 GHz (Error Code 17)
18.6 (or 20) GHz (Error Code 18)
(All models except 6653A/6659A)
18.0 GHz (Error Code 18) Models 6653A/6659A
26.5 GHz (Error Code 19)
Wish End (Error Code 20)

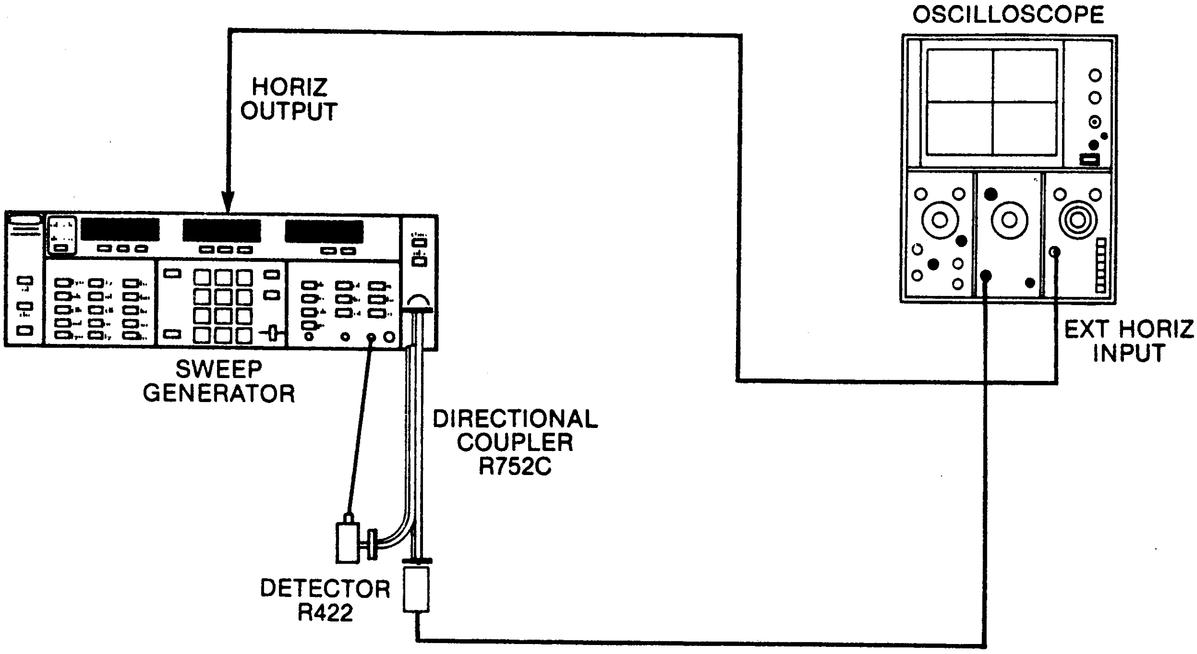
Scalar Network Analyzer

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 5
REFERENCE dB/dBm: dBm
SET (screwdriver pot): Midrange
OFFSET: -00.00
CHANNEL B: Not Used
MARKER THRESHOLD: Midrange
REAL TIME: On
SMOOTHING: Off

POWER: ON

*External leveling shown by dashed-line connections.

Figure 7-45. Test Equipment Setup for Troubleshooting Error Codes 15 thru 20



Initial Control Settings

Sweep Generator

FREQUENCY RANGE: F1-F2
TRIGGER: AUTO
MARKERS: INTENSITY
LEVELING: INTERNAL (DETECTOR*)
RETRACE RF: Off
RF ON: On
CW RAMP: Off
RF SLOPE: OFF
LEVEL: 0 dBm
SWEEP TIME: 50 ms
F1: 26.5 GHz
F2: 40 GHz

Figure 7-46. Test Equipment Setup for Troubleshooting the Model 6642A ALC Loop

GENERAL INFORMATION FOR ALC LOOP TROUBLESHOOTING CHART

1. DC voltages for the A4, A6, A7, A8, and A9 PCBs may be measured at the following pins:

   A4P1 (edge connector)
   - +5V – pins R(+) and P(-)
   - +15V – pins M (+) and L (-)
   - -15V – pins N (-) and L (+)

   A6P1 (edge connector)
   - +5V – pins 12 (+) and 11 (-)
   - +15V – pins 9 (+) and 21 (-)
   - -15V – pins 10 (-) and 21 (+)

   A7, A8, or A9 P1
   - +5V – pins 11 (+) and 10 (-)
   - +15V – pins 8 (+) and 20 (-)
   - -15V – pins 9 (-) and 20 (+)

2. In the case of multiple error codes, troubleshoot lowest-numbered codes first.

3. All logic levels are TTL.

Table 7-15. Available ALC Error Codes

MODEL NUMBER	AVAILABLE ERROR CODES
6609A	15 & 20
6617A	15, 16, & 20
6621A	16, 17, & 20
6621A-40	16, 17, & 20
6629A	17, 18, & 20
6629A-40	17, 18, & 20
6637A	16, 17, 18, & 20
6637A-40	16, 17, 18, & 20
6638A	16, 17, 18, & 20
6642A	16 & 20
6647A	15, 16, 17, 18, & 20
6648A	15, 16, 17, 18, & 20
6653A	16, 17, 18, 19, & 20
6659A	15, 16, 17, 18, 19, & 20

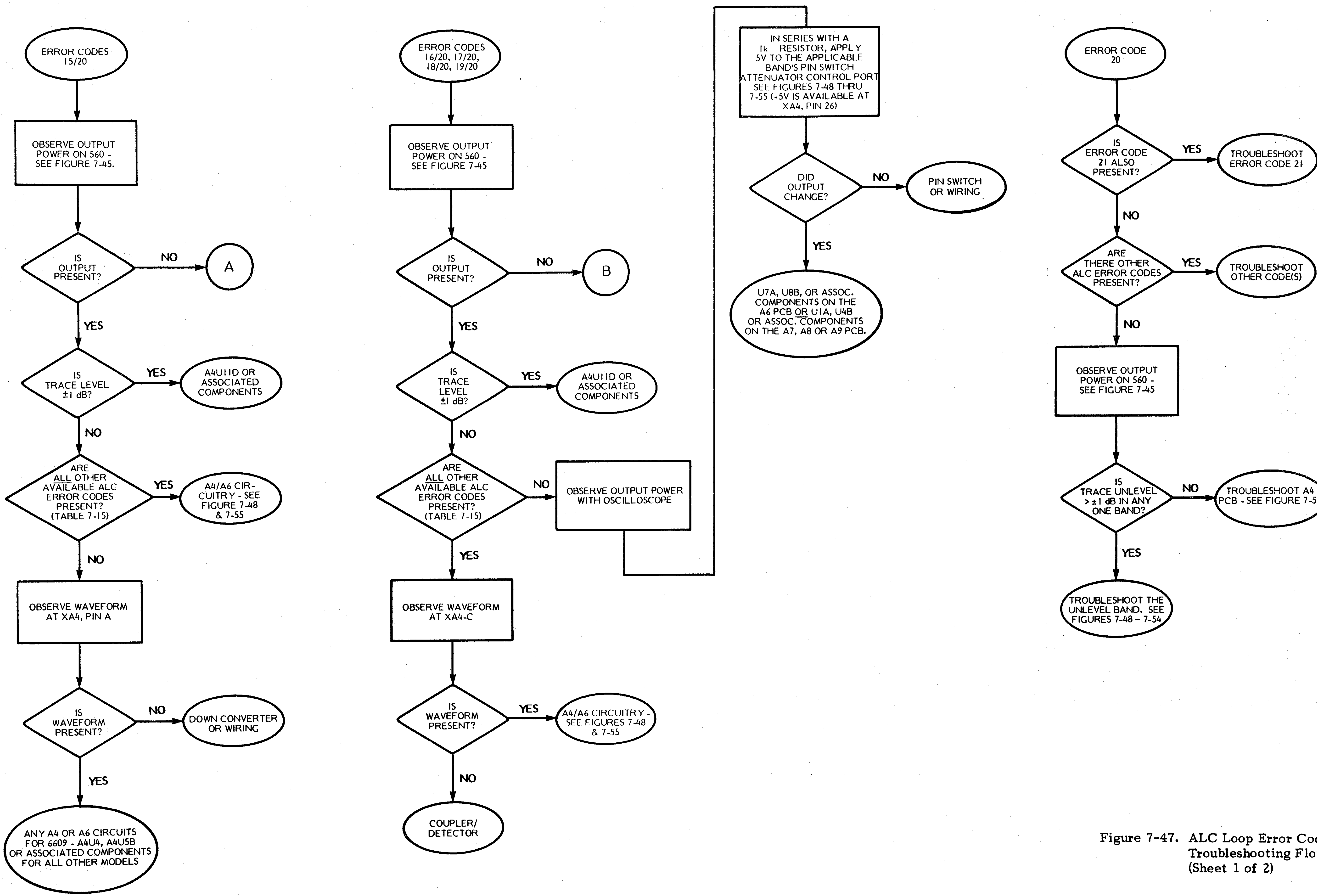
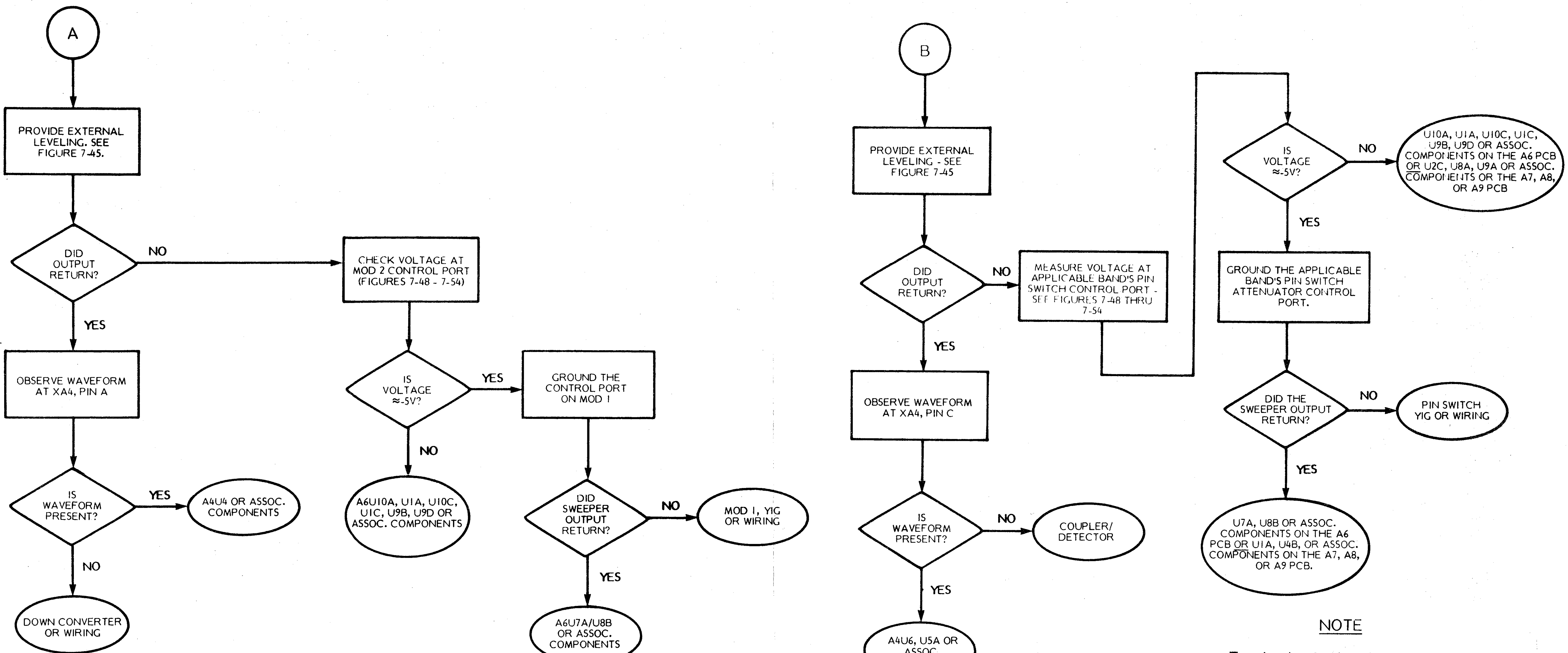


Figure 7-47. ALC Loop Error Code Troubleshooting Flowchart (Sheet 1 of 2)



NOTE

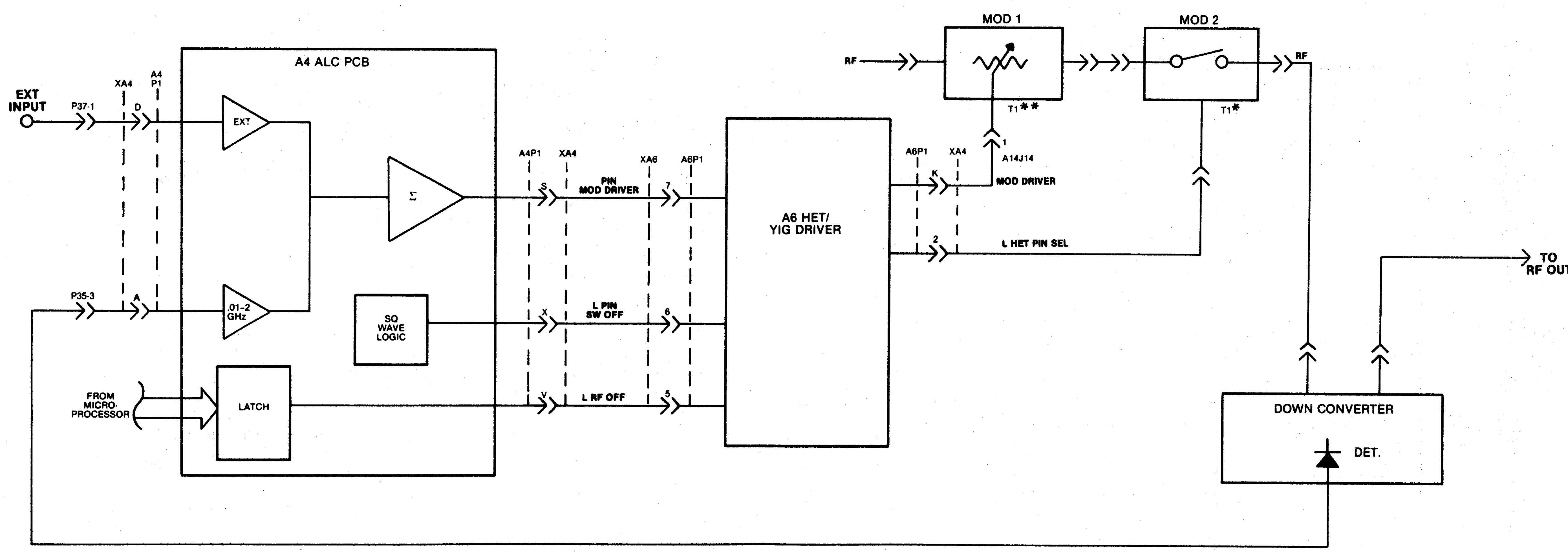
To check if the YIG has bias voltage, refer to paragraph 5-8.2.

NOTE

To check if the YIG has bias voltage, refer to paragraph 5-8.2.

Figure 7-47. ALC Loop Error Code Troubleshooting Flowchart (Sheet 2 of 2)

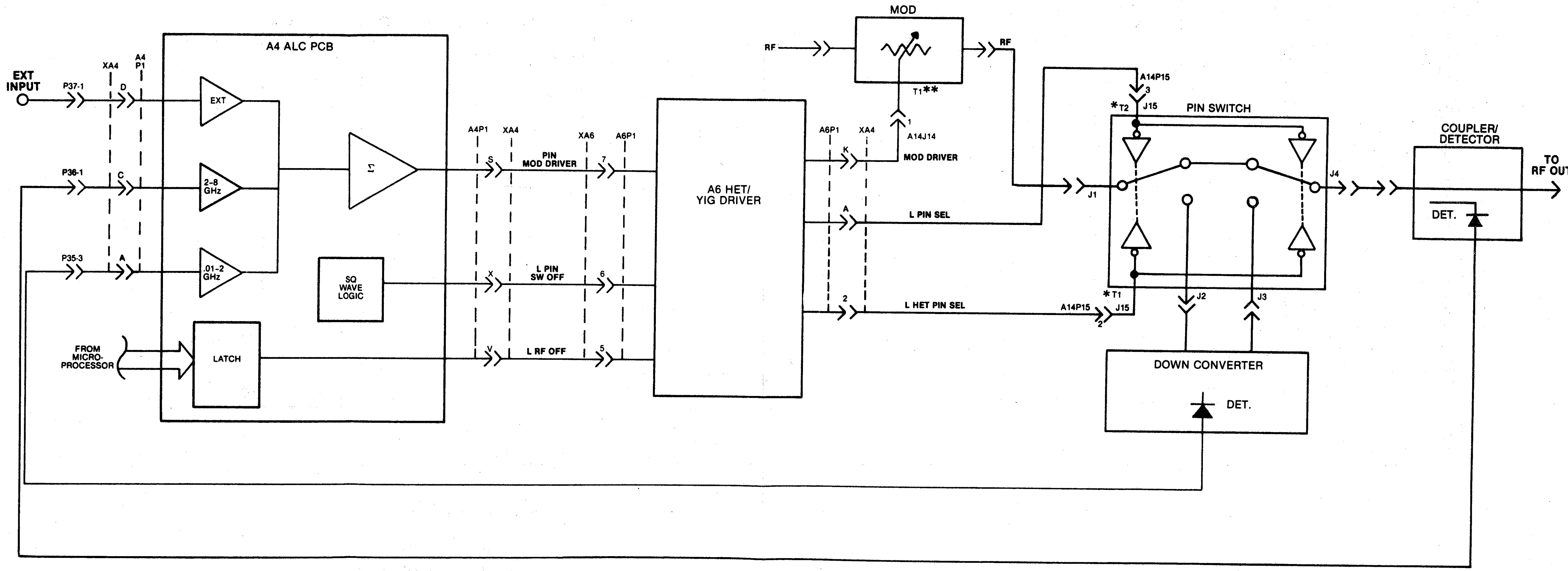
Figure 7-47(A).



*Switch Control Port
* *Attenuator Control Port

NOTE
To measure voltage at the switch and attenuator control ports, press RETRACE RF to ON.

Figure 7-48. Model 6609A ALC Loop Troubleshooting Simplified Schematic



*Switch Control Port
**Attenuator Control Port

NOTE
To measure voltage at the switch and attenuator control ports, press RETRACE RF to ON.

Figure 7-49. Model 6617A ALC Loop Troubleshooting Simplified Schematic

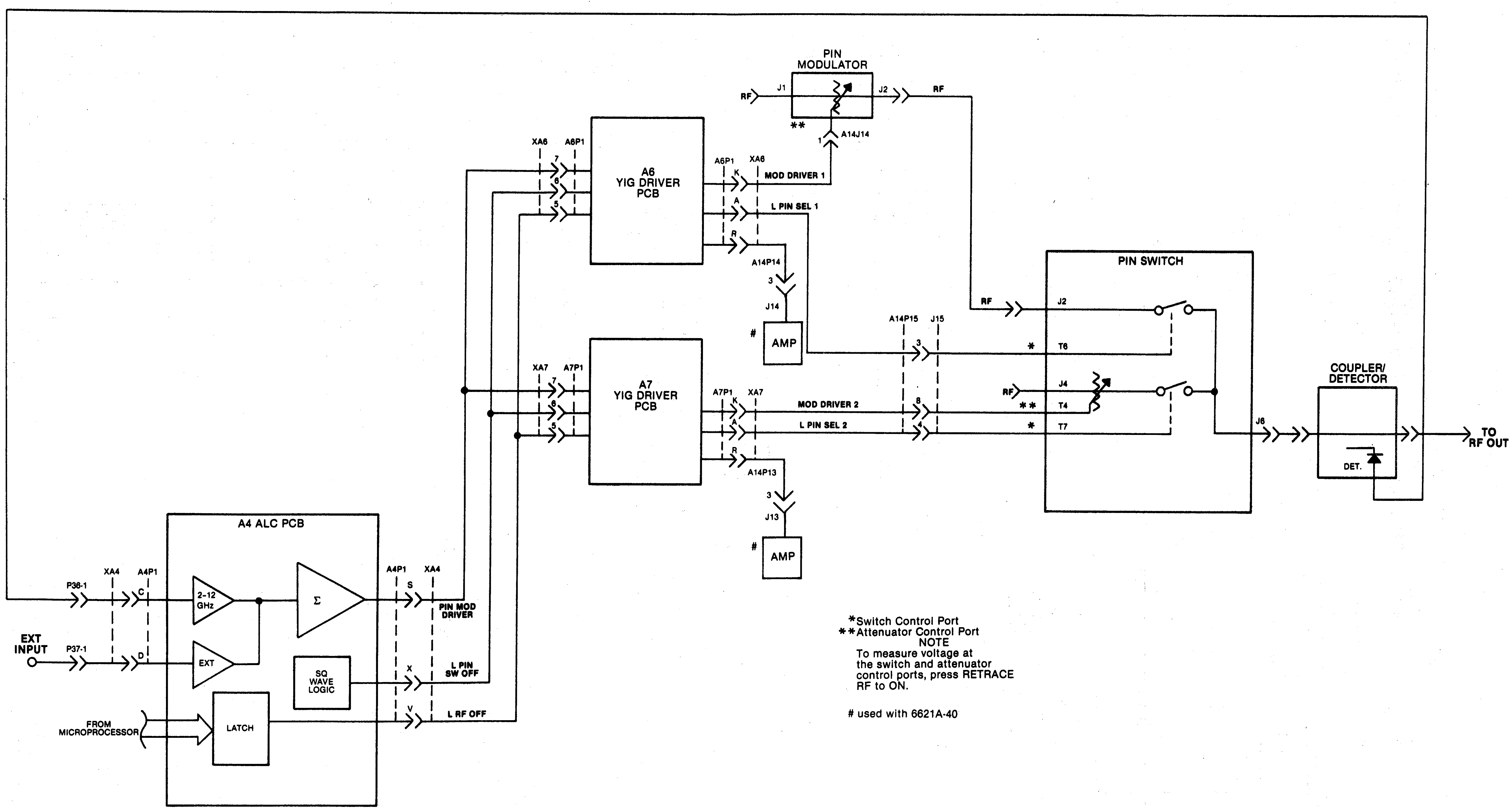
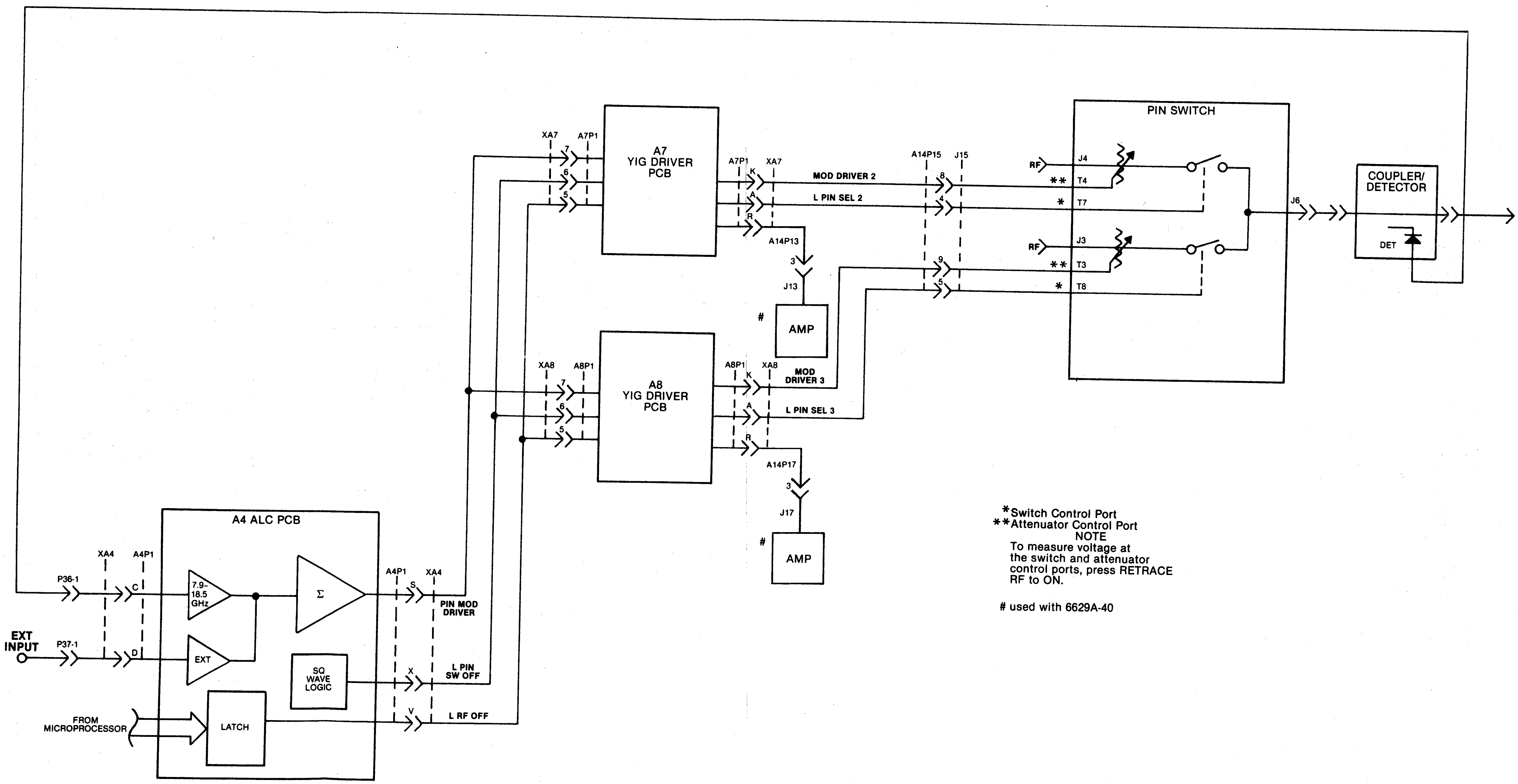


Figure 7-50. 6621A/6621A-40 ALC Loop Troubleshooting Simplified Schematic

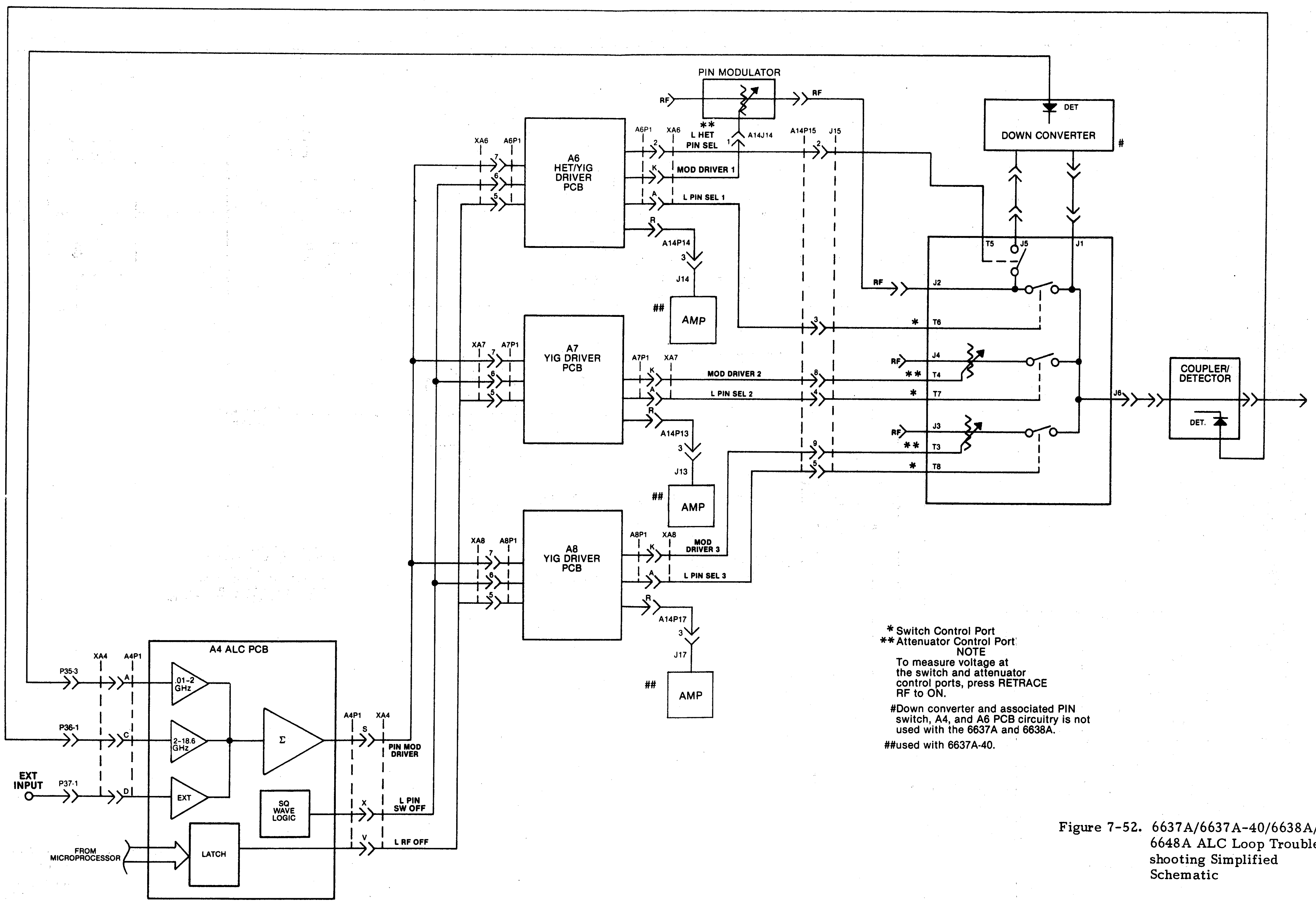


*Switch Control Port
**Attenuator Control Port

NOTE
To measure voltage at the switch and attenuator control ports, press RETRACE RF to ON.

used with 6629A-40

Figure 7-51. 6629A/6629A-40 ALC Loop Troubleshooting Simplified Schematic



* Switch Control Port
** Attenuator Control Port
NOTE
To measure voltage at the switch and attenuator control ports, press RETRACE RF to ON.

#Down converter and associated PIN switch, A4, and A6 PCB circuitry is not used with the 6637A and 6638A.

##used with 6637A-40.

Figure 7-52. 6637A/6637A-40/6638A/6647A/6648A ALC Loop Troubleshooting Simplified Schematic

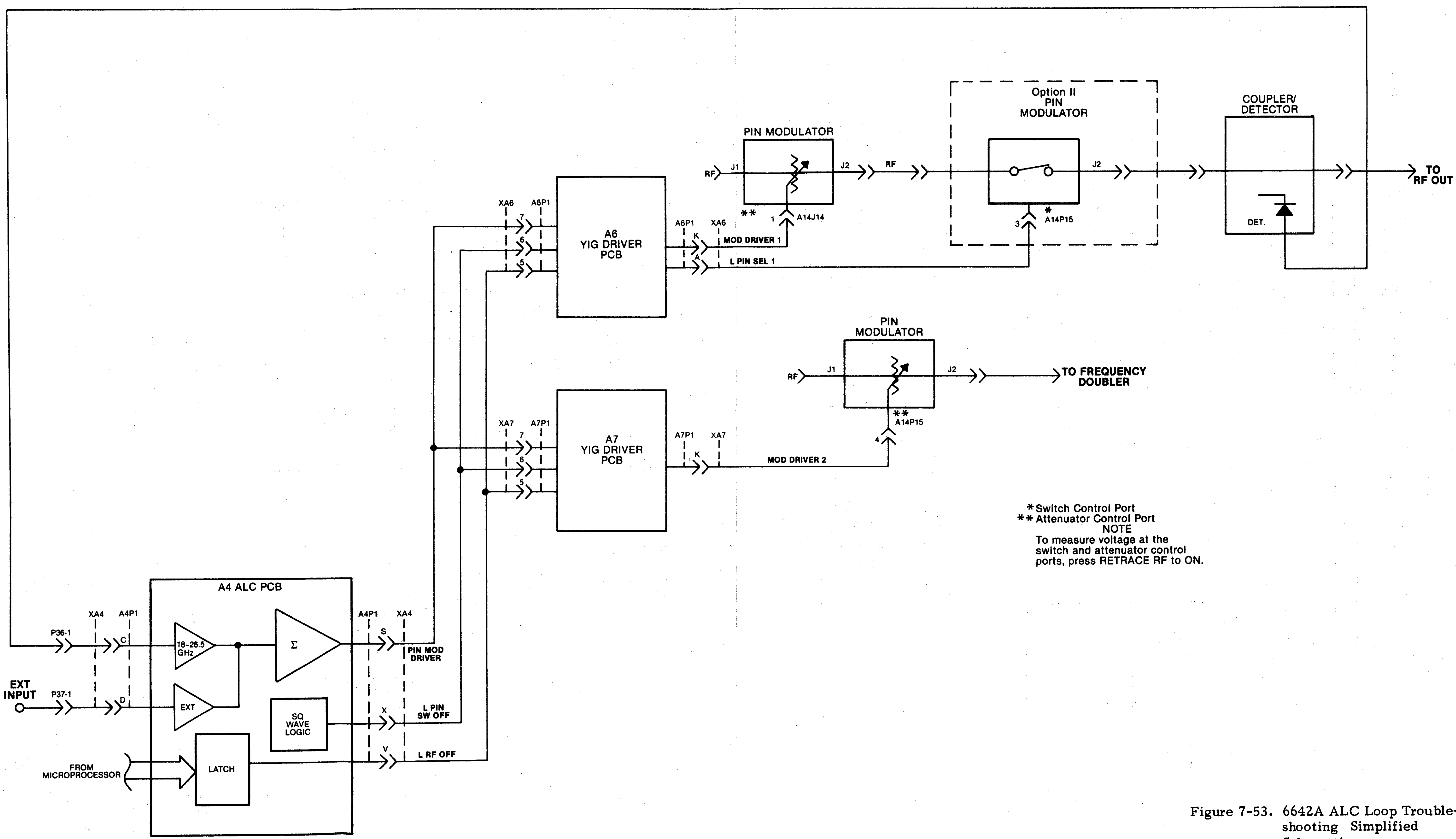


Figure 7-53. 6642A ALC Loop Trouble-shooting Simplified Schematic

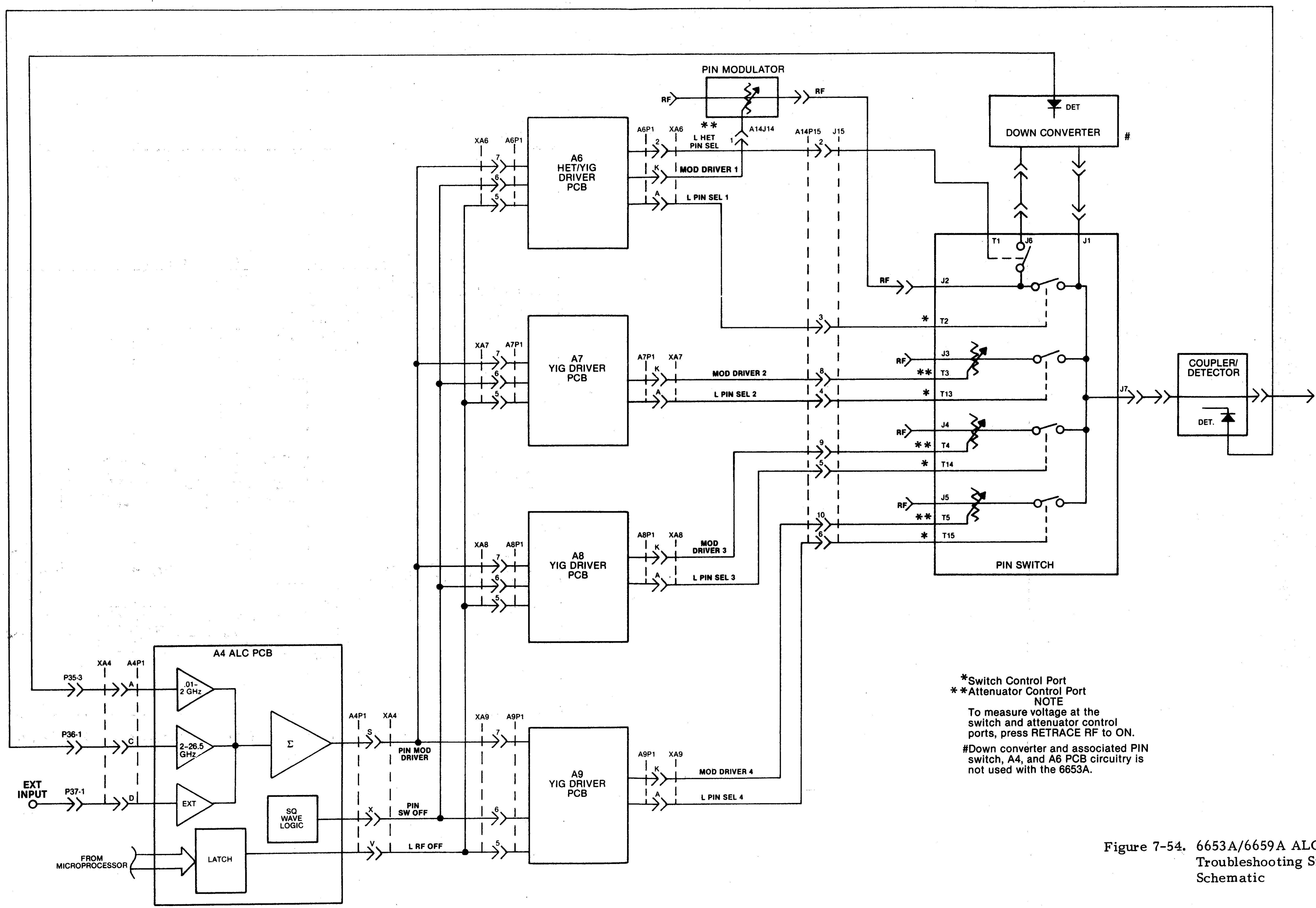


Figure 7-54. 6653A/6659A ALC Loop Troubleshooting Simplified Schematic

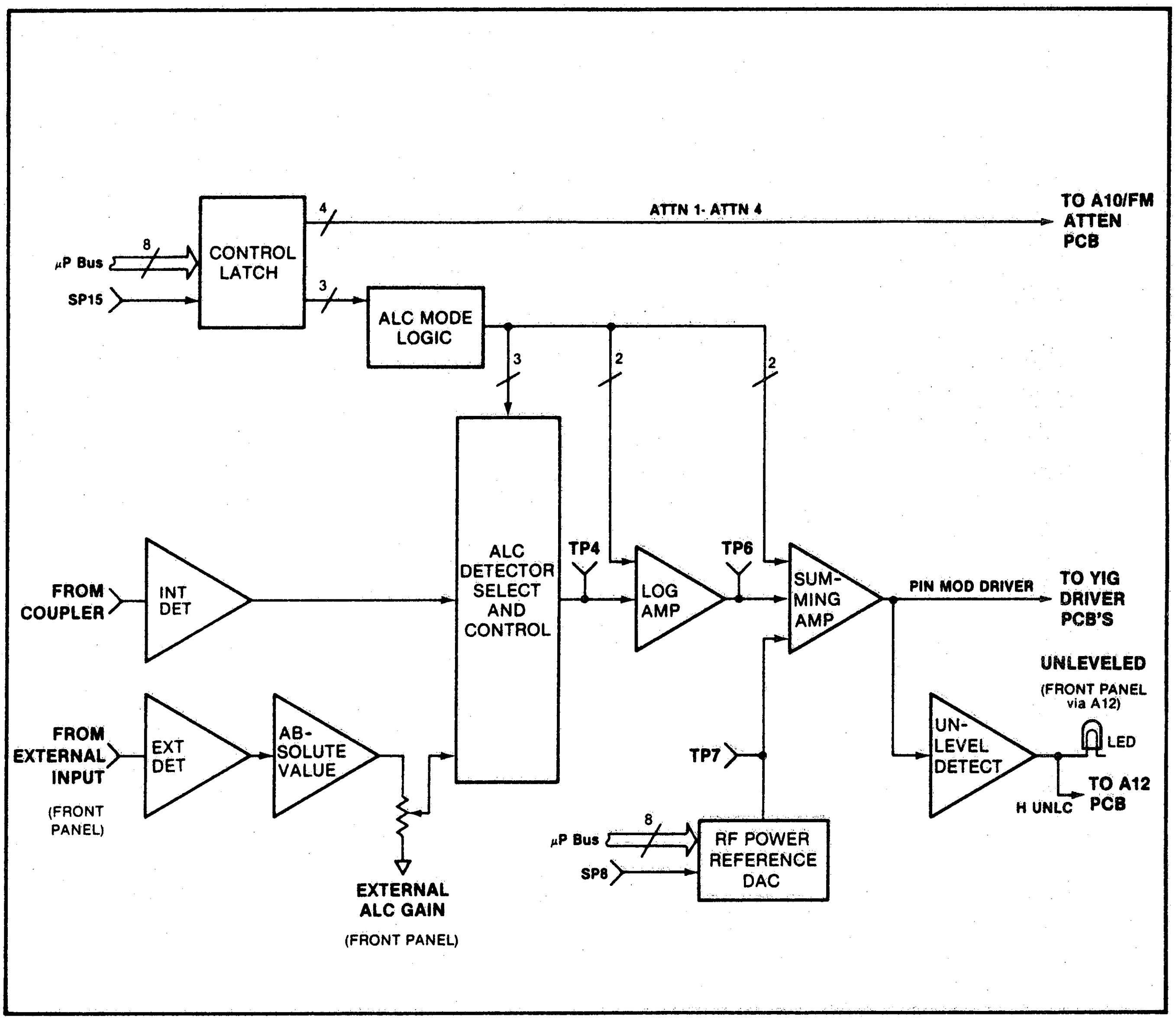
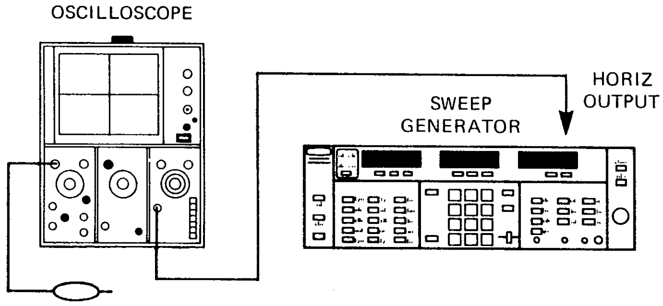


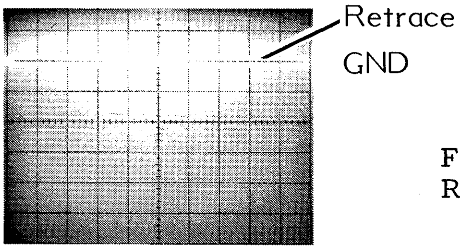
Figure 7-55. Error Code 20 Troubleshooting Block Diagram

TEST EQUIPMENT SETUP

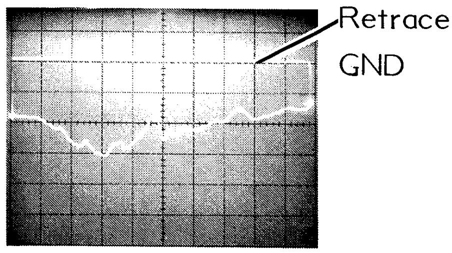


MODEL 720 DETECTOR OUTPUT

LEVELED



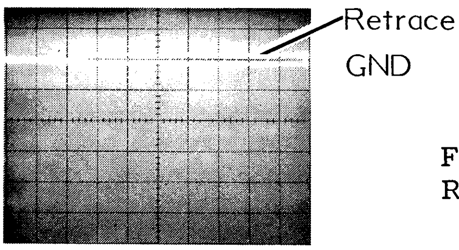
UNLEVELED*



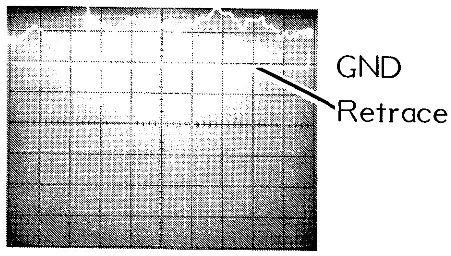
Frequency: .01 - 2 GHz
RF Power: 5 dBm

A4TP4

LEVELED



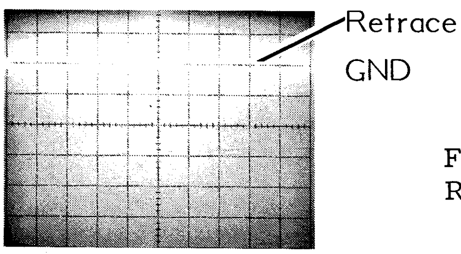
UNLEVELED*



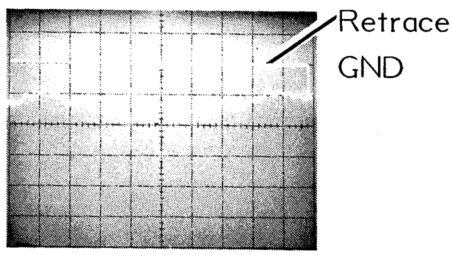
Frequency: .01 - 8 GHz
RF Power: 5 dBm

COUPLER OUTPUT

LEVELED



UNLEVELED*



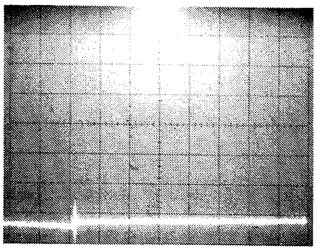
Frequency: 2 - 8 GHz
RF Power: 5 dBm

* Unleveled output simulated by disabling A4P1, pin S.

Figure 7-56. ALC Loop Waveforms

A4TP6

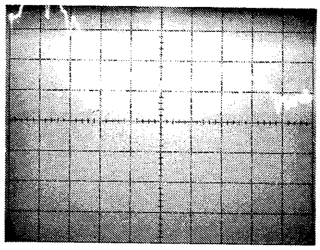
LEVELED



GND

Frequency: .01 - 8 GHz
RF Power: 5 dBm

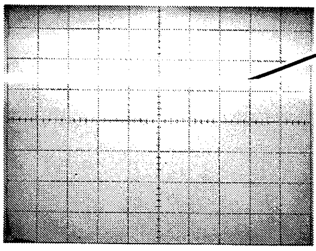
UNLEVELED*



GND

A6P1, Pin K

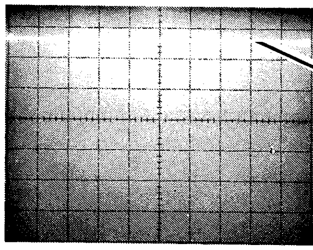
LEVELED



Retrace
GND

Frequency: .01 - 8 GHz
RF Power: 5 dBm

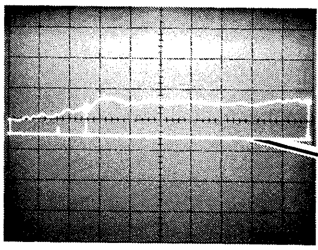
UNLEVELED**



Retrace
GND

A4P1, Pin S

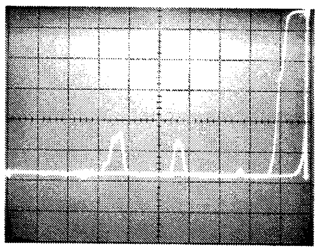
LEVELED



GND
Retrace

Frequency: .01 - 8 GHz
RF Power: 5 dBm

UNLEVELED*



+15V
GND
-15V

NOTE

The unleveled waveform shown is an example of one that could appear at pin S. The Level Amplifier (U24) could also be latched at either rail, in which case the waveform could be a straight line (dc voltage), appearing at either +15V or -15V.

* Unleveled output simulated by disabling A4P1, pin S.
** Unleveled output simulated by disabling A6P1, pin K.

Figure 7-56. ALC Loop Waveforms (Continued)

Table 7-16. RF Components, Specification Data

YIG-TUNED OSCILLATORS

FREQUENCY (GHz)	WILTRON PART NO.	MINIMUM POWER mW	dBm
18 - 36.5	1005-35	10.0	10.0[1]
13.25 - 20	1005-40	20.0	13.0[2]
4.6 - 6.6	1005-45	3.2	5.0
12.4 - 18.6	1005-51	30.2	14.8
12.4 - 20	1005-52	50.0	17.0[3]
8 - 12.4	1005-53 or -54	45.0	16.5
12.4 - 18.0	1005-55 or -59	45.0	16.5
18 - 26.5	1005-61	20.0	13.0

[1] +8 dBm (6.4 mW) from 17.8 to 26.7 GHz.
[2] +17 dBm (15.0 mW) from 12.3 to 18.5 GHz.
[3] 16 dBm (40.0 mW) from 18.5 to 20 GHz.

RF COMPONENTS

COMPONENT	WILTRON PART NO.	FREQUENCY (GHz)	SPECIFICATION (Max.)
Isolators	All	All	Insertion Loss: 0.5 dB
Low Pass Filters	1030-26 1030-21	2 - 8 2 - 18.7	Insertion Loss: 0.5 dB 0 to 10 GHz; 0.6 dB 10.1 to 22 GHz
Low Pass Filters	All Others	--	Insertion Loss: 0.5 to 10 GHz; 0.55 dB to 18.7 GHz
PIN Switch, DPDT	660-B-8149	.01 - 8	Insertion Loss: 2 dB
PIN Switch, 4-Port	660-C-8821	.01 - 20	Insertion Loss @ Ic = 0 .01 -2 GHz Port - 1.5 2 - 8 GHz Port - 2.5 dB 8 - 12.4 GHz Port - 2. 12.4 - 20 GHz Port - 3.
PIN Switch, 5-Port	660-D-11745	.01 - 26.5	Insertion Loss @ Ic = 0 .01 -2 GHz Port - 2.0 2 - 8 GHz Port - 3.0 8 - 12.4 GHz Port - 2 12 - 18.5 GHz Port - 3 18 - 26.6 GHz Port - 4
Directional Coupler	660-C-8657	2 - 18.6	Insertion Loss: 1 ±0 Sensitivity: ±0.4 dB
Directional Coupler	660-B-8125-2	2 - 26.5	Insertion Loss: <1 dB
Modulator	660-C-9342	2 - 8	Insertion Loss @ Ic = 0 1.5 dB
Down Converter	660-D-9157	.01 - 2	Output Power: +13 dB for -8 dBm input

7-12 A5 FREQUENCY INSTRUCTION AND A6-A9 YIG DRIVER PCBs

7-12.1 A5 Frequency Instruction PCB, Circuit Description

The A5 Frequency Instruction PCB provides YIG oscillator tuning voltages to the A6, A7, A8 and A9 YIG Driver PCBs, plus a narrow (≤50 MHz) sweep-tuning-voltage ramp to the A10 FM/Attenuator PCB. The A5 PCB also supplies a regulated +10V bandswitch-reference voltage to the A6-A9 YIG Driver PCBs, and an RF Slope control voltage to the A12 Microprocessor PCB. A functional block diagram of the A5 PCB is shown in Figure 7-57 and the schematic (2 sheets) is shown in Figure 7-58.

The three main YIG tuning voltages supplied by the A5 PCB (Figure 7-57) are the **F CEN**, **ΔF >50 MHz**, and **F CORR** signals. These three signals are summed together at the YIG Driver PCBs and used to generate the YIG oscillator tuning current.

The **F CEN** signal is the output of the Center Frequency digital-to-analog converter (DAC) circuit (U7, U6). The input to this circuit is a 16-bit group from the microprocessor representing one of the following:

- the center frequency in a FULL, F1-F2, or M1-M2 sweep,
- the F0 frequency in a ΔF F0 sweep,
- the F1 frequency in a ΔF F1 sweep, or
- the selected CW F0, CW F1, CW F2, CW M1, or CW M2 frequency.

The two 8-bit words constituting the center-frequency-control group are applied to the FCEN DAC (U7) via FCEN Latches 1, 2, and 3. Word #1 (the MS word) is loaded into latch #2 (U9) when the microprocessor clocks **SP0** HIGH. Word #2 (the LS word) is loaded into latch #1 (U8) when **SP1** is clocked HIGH. Coincident with word #2 being clocked thru latch #1, word #1 is clocked thru latch #3. This latching arrangement allows all 16 bits of the center-frequency-control group to be simultaneously applied to the FCEN DAC. The other A5 PCB input affecting the **F CEN** signal line is **FREQ OFFSET**. This line is only active when the sweep generator is part of a Model 661 Tracking Sweeper Controller System. At that time, the voltage present on this line offsets the **F CEN** signal, as determined by the tracking sweeper controller.

The **ΔF >50 MHz** signal is the output from the Sweep Width (ΔF) DAC (U24). The U24 circuit is a multiplier DAC that scales the analog REF input by a factor of N/4095. The circuit gain is from 0 to 1 and the resolution is $1 \div 2^{12}$ ($1 \div 4096$). The digital input to U24 is a 12-bit group from the microprocessor representing one of the following:

- the sweep width in a FULL, F1-F2, or M1-M2 sweep,
- the ΔF value in a ΔF F0 or ΔF F1 sweep, or
- a zero value in any of the five CW frequency modes.

The input digital group is loaded into the two ΔF Latches (U17, U18) when the microprocessor clocks **SP6** and **SP7** HIGH.

The analog REF input to the Sweep Width (ΔF) DAC (U24) is a 10-volt signal (-5V to +5V) from the Sweep Sel Switch (U22A, U22B, U22C), via the -5V Offset circuit (U23). The inputs to the Sweep Sel Switch are a 0-10V manual tuning voltage from the front panel MANUAL SWEEP control, a 0-10V ramp from the A2 Ramp Generator PCB, or a 0-10V step-frequency tuning voltage from the Step Freq DAC (U19). The input to this DAC is a 12-bit group from the microprocessor that is generated in response to GPIB bus commands (paragraph 3-7.2). This 12-bit group is formed using two 8-bit words (the remaining 4-bits in word #1 are used to (1) control the Sweep Sel Switch and (2) provide an input for the CW Filter Current Driver circuit). Word #1 (the MS word) is loaded into latch #2 (U16) when the microprocessor clocks **SP4** HIGH. Word #2 (the LS word) is loaded into latch #1 (U15) when **SP3** is clocked HIGH. Coincident with word #2 being clocked thru latch #1, word #1 is clocked thru latch #3 (U31). This latching arrangement allows all 12 bits of the step-frequency-control group to be simultaneously applied to the Step Freq DAC.

The output of the Sweep Width DAC is applied to the W/M/N Switch (U28A, U28B, U28C, U28D). This switch is controlled by the microprocessor, via the ΔF Latch 2 circuit. The W/M/N switch is used to select a wide (>1000 MHz), medium (51 to 1000 MHz), or narrow (≤50 MHz) sweep width. If the microprocessor has selected a wide sweep width, the DAC output is applied to the output circuit via the Buffer (U26). If the medium sweep width has been selected, the DAC output is scaled down by the ÷16 resistor (R37) before being applied to the output circuit. And if the narrow sweep width has been selected, the DAC output is applied to the Diff Amp circuit (U10B). This circuit cancels any common-mode signals existing between the analog ground on the A5 PCB and the analog ground on the A10 PCB. The output of the Diff Amp is applied to the A10 PCB via the **ΔF ≤50 MHz** signal line.

The F **CORR** signal is the output from the I/E (current to voltage) Converter circuit (U3). The input to this circuit is the sum of the current outputs from the ROM Lin DAC, the Freq Ver DAC, and the Freq Overlap circuit.

The ROM Lin DAC (U2) provides a linearity-correction frequency for the YIG oscillator. The input to this DAC is from the linearizer ROM on either the A6, A7, A8, or A9 PCB, depending on which YIG oscillator band is presently in use. The purpose of this linearizing ROM is to store data that will correct for nonlinear frequency characteristics in the YIG oscillator. The stored data provides the YIG oscillator with a frequency correction of up to ±64 MHz.

The Freq Ver DAC (U4) provides a vernier-correction frequency for the YIG oscillator. The input to this DAC is an 8-bit group from the microprocessor representing the front panel FREQUENCY VERNIER control-group output. This word is latched into the Freq Ver Latch (U5) when the microprocessor clocks **SP** 2 HIGH. The Freq Ver DAC output provides the YIG oscillator with a frequency correction of up to ±12.7 MHz.

The Freq Overlap circuit (U33A-U33D, U34A-U34D, U35A, U35D) provides a 20 MHz frequency overlap between bands during a >200 MHz frequency sweep. This frequency overlap prevents frequency gaps from occurring due to the ±10 MHz accuracy of the YIG oscillators. There are five control inputs to this switching circuit, in addition to the **FCEN/VPF** signal that provides the frequency-overlap-tuning voltage. Four of the inputs are from the A6-A8 YIG Driver PCBs. These inputs select the resistor values needed to scale the **FCEN/VPF** ramp down to the correct frequency-overlap value. The fifth control input, **L >200 MHz,** determines when the circuit will be activated. For ΔF values greater than 200 MHz, the circuit is switched into the **F CORR** line circuitry; for ΔF values ≤200 MHz, the circuit is not active.

When no frequency correction is needed, the **F CORR** signal is 0 volts. If no linearity correction is required, the Lin ROM DAC input is 01111111 (0 = most significant bit). (There may be cases where a YIG oscillator requires no linearity correction. In such cases, no linearizing ROM is supplied and the U2 input resistors (Figure 7-58) provide the 01111111 input.) If no frequency vernier correction has been programmed for the selected frequency parameter (paragraph 3-2.2c), 01111111 is also clocked into the Freq Ver Latch. When the output currents of the two frequency-correction DACs are summed with the equal-but-opposite current from R4, and if no frequency overlap voltage is applied, the I/E Converter outputs 0 volts.

The other signals generated on the A5 PCB are the **FCEN/VPF**, **V/GHz**, **RAMP OUT**, **CW FILTER**, **L CW** Mode, and **RF** Slope control.

The **FCEN/VPF** signal is from the FCEN/VPF switch. The inputs to this switch are **F CEN** and the sum of F **CEN** and either **ΔF >50 MHz** or **ΔF ≤50 MHz**. If the sweep width is ≤200 MHz, the **F CEN** signal is switched onto the **FCEN/VPF** line. This line is used on the A6 thru A9 YIG Driver PCBs to control oscillator bandswitching. If the sweep width is 200 MHz or less, bandswitch is inhibited. Control for the FCEN/VPF switch is from the microprocessor, via the ΔF Latch 2 circuit.

The **V/GHz** signal is the sum of the **F CEN** and either the **ΔF >50 MHz** or the **ΔF≤50MHz** signals. The two signals are summed at the

FCEN/VPF Sum circuit (U14) and applied to the V/GHz Amp (U12). At U12, the output of the sum circuit is scaled so that the amplitude of the output ramp is 1V/GHz for all models except the 6642A, 6653A, and 6659A; in these models it is 0.5V/GHz. This output is applied to the rear panel 1V/GHz OUTPUT connector.

The RAMP OUT signal is from the +5V Offset circuit (U21A). This circuit restores the frequency tuning voltage to its original 0 to 10V state. The **RAMP OUT** signal is applied to the A3 Marker Generator PCB, where it is buffered and applied to the rear panel HORIZ OUTPUT connector.

The **CW FILTER** signal is from the CW Filter Current Driver circuit (Q1). The input to this circuit is from the microprocessor, via the Step Freq Latch 2 circuit. The CW Filter Current Driver converts the latch-output voltage to a current, which is used to drive the CW filter relay on the A6, A7, A8, and A9 YIG Driver PCBs.

The **L CW MODE** signal is created by ANDing together the three ΔF Latch 2 signals that control the W/M/N Switch. Only in a CW mode are all three of these signals HIGH simultaneously. The **L CW MODE** signal is applied to the A4 PCB.

The **RF SLOPE CONTROL** signal is from the Offset Amplifier circuit (U35B, U35C). This signal applies a model-dependent offset voltage to the front panel RF Slope control circuitry on the A12 Microprocessor PCB.

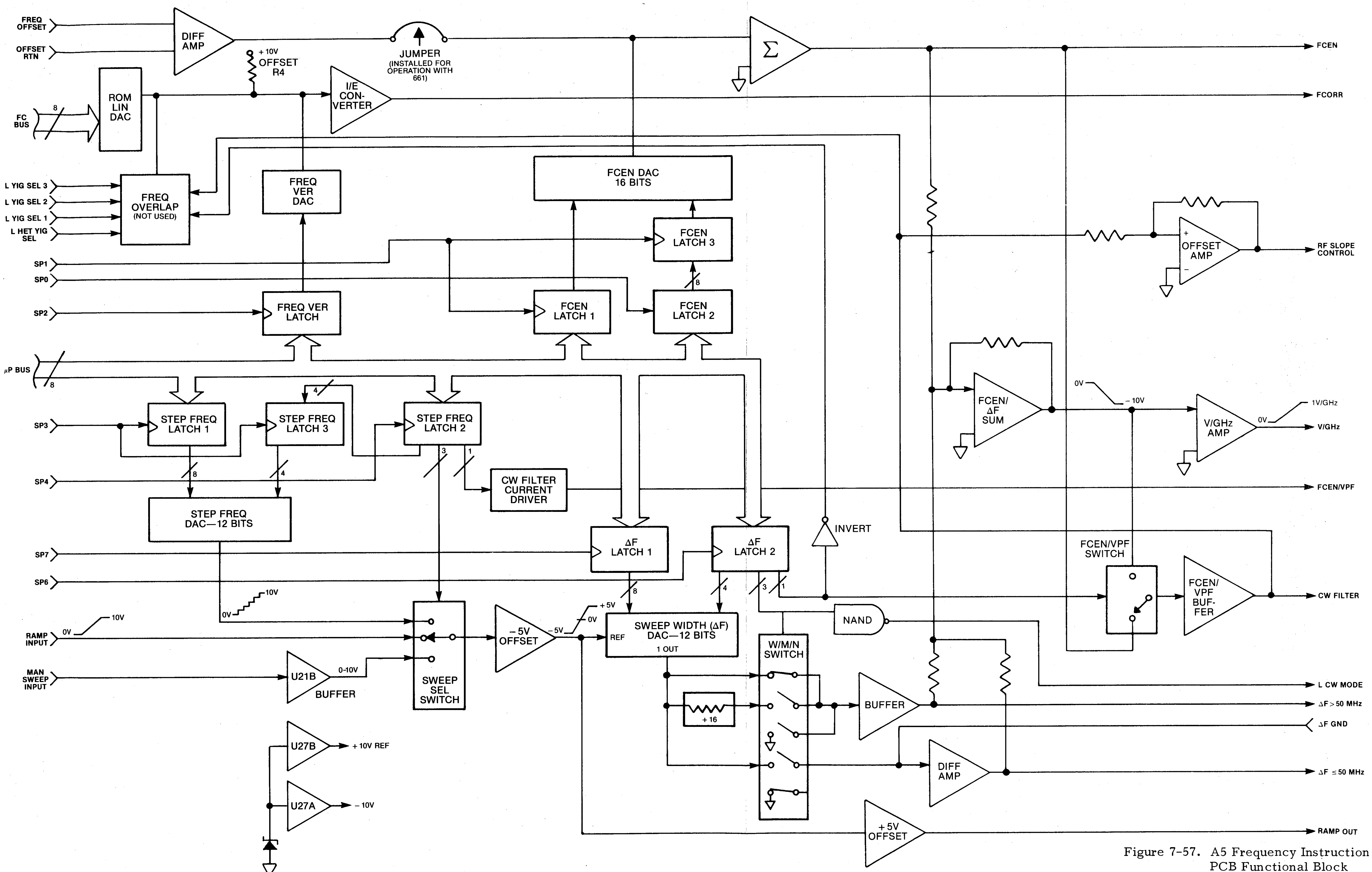


Figure 7-57. A5 Frequency Instruction PCB Functional Block Diagram

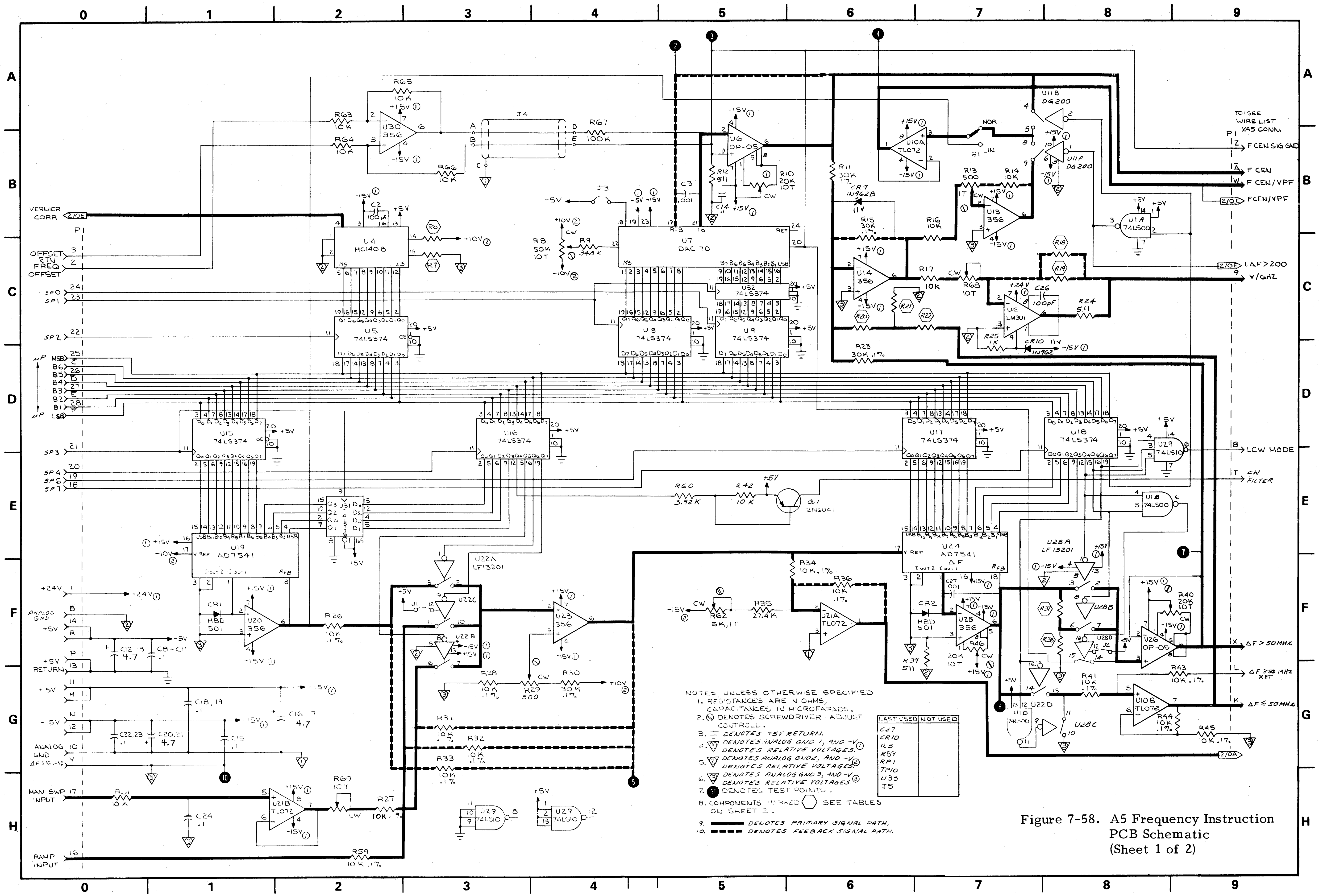
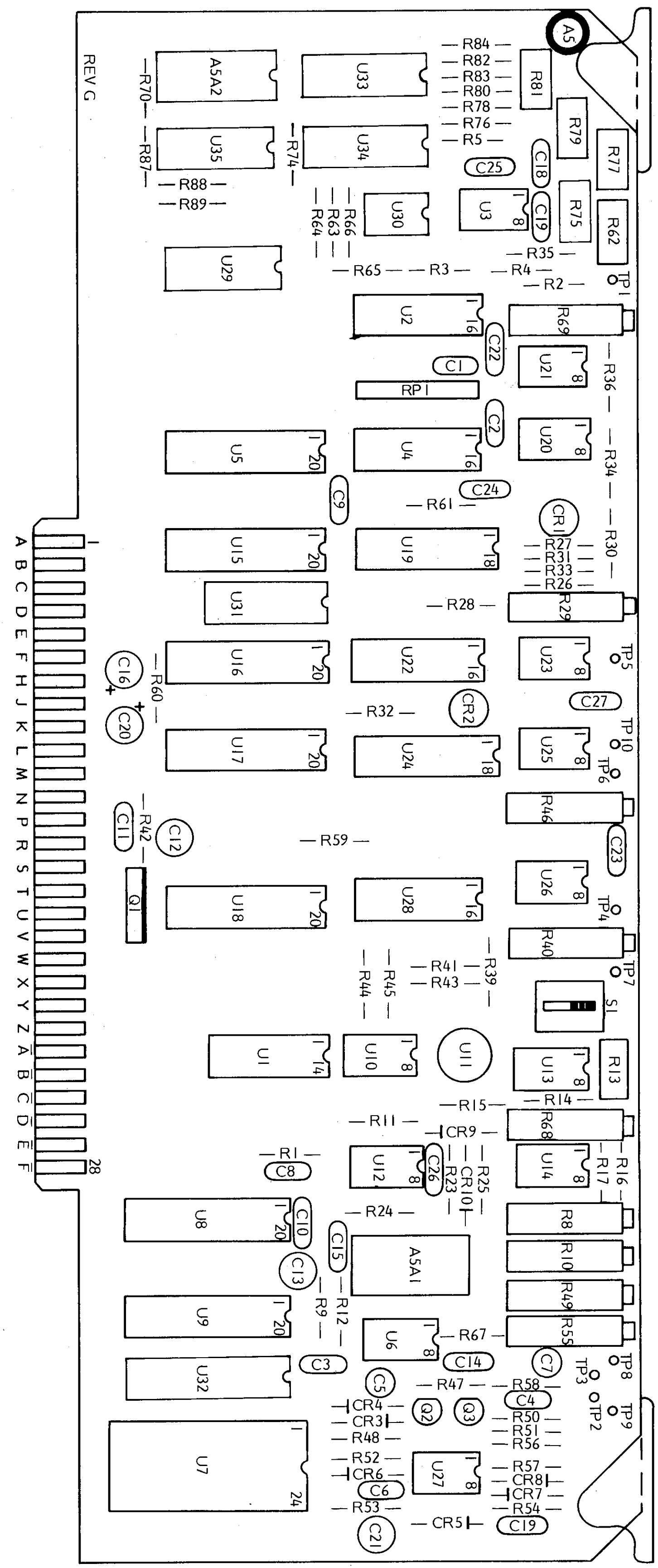
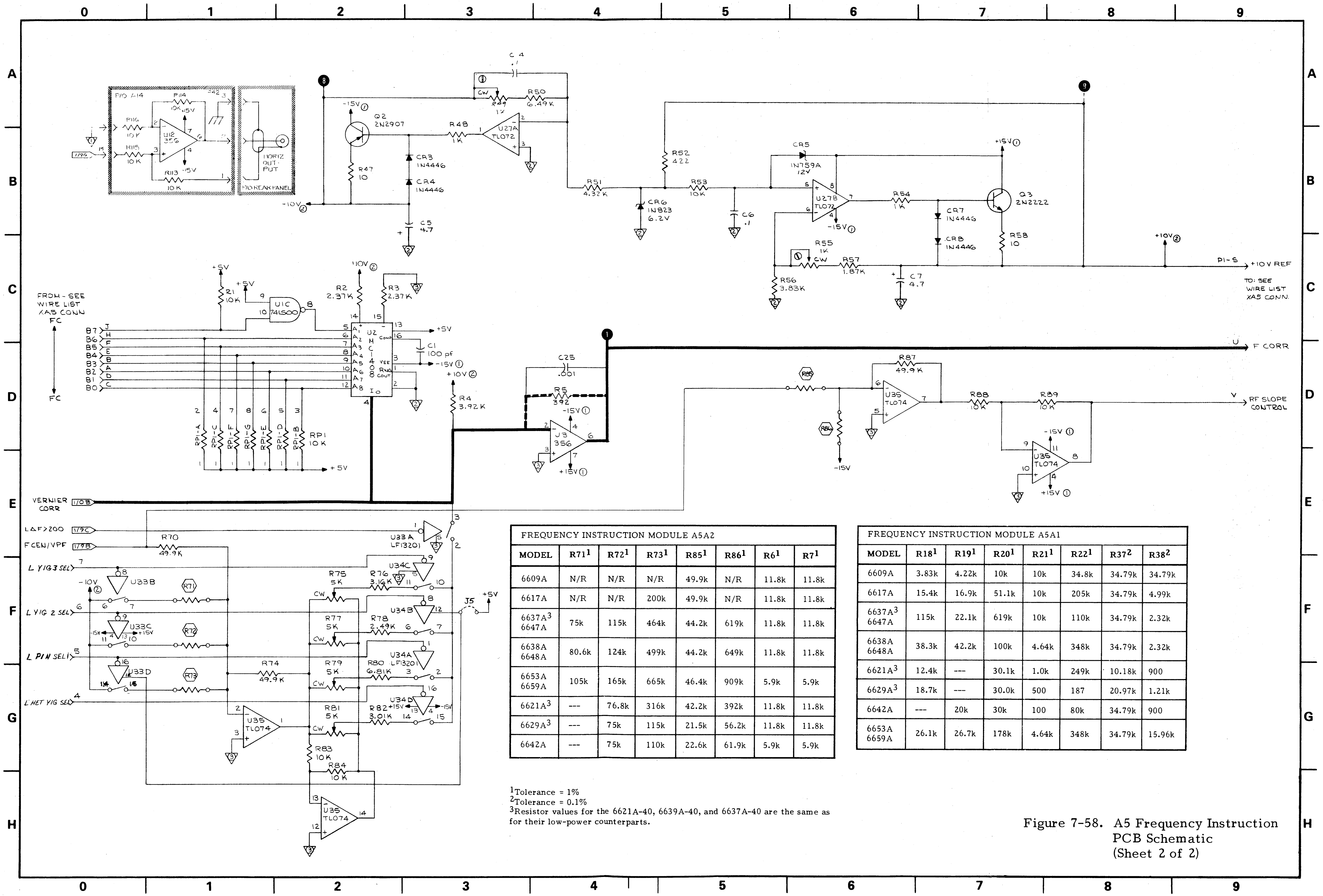


Figure 7-58. A5 Frequency Instruction PCB Schematic (Sheet 1 of 2)



A5 PCB Parts Locator Diagram

Figure 7-58 (Sheet 1 of 2)



FREQUENCY INSTRUCTION MODULE A5A2							
MODEL	R71[1]	R72[1]	R73[1]	R85[1]	R86[1]	R6[1]	R7[1]
6609A	N/R	N/R	N/R	49.9k	N/R	11.8k	11.8k
6617A	N/R	N/R	200k	49.9k	N/R	11.8k	11.8k
6637A[3] 6647A	75k	115k	464k	44.2k	619k	11.8k	11.8k
6638A 6648A	80.6k	124k	499k	44.2k	649k	11.8k	11.8k
6653A 6659A	105k	165k	665k	46.4k	909k	5.9k	5.9k
6621A[3]	---	76.8k	316k	42.2k	392k	11.8k	11.8k
6629A[3]	---	75k	115k	21.5k	56.2k	11.8k	11.8k
6642A	---	75k	110k	22.6k	61.9k	5.9k	5.9k

FREQUENCY INSTRUCTION MODULE A5A1							
MODEL	R18[1]	R19[1]	R20[1]	R21[1]	R22[1]	R37[2]	R38[2]
6609A	3.83k	4.22k	10k	10k	34.8k	34.79k	34.79k
6617A	15.4k	16.9k	51.1k	10k	205k	34.79k	4.99k
6637A[3] 6647A	115k	22.1k	619k	10k	110k	34.79k	2.32k
6638A 6648A	38.3k	42.2k	100k	4.64k	348k	34.79k	2.32k
6621A[3]	12.4k	---	30.1k	1.0k	249k	10.18k	900
6629A[3]	18.7k	---	30.0k	500	187	20.97k	1.21k
6642A	---	20k	30k	100	80k	34.79k	900
6653A 6659A	26.1k	26.7k	178k	4.64k	348k	34.79k	15.96k

[1] Tolerance = 1%
[2] Tolerance = 0.1%
[3] Resistor values for the 6621A-40, 6639A-40, and 6637A-40 are the same as for their low-power counterparts.

Figure 7-58. A5 Frequency Instruction PCB Schematic (Sheet 2 of 2)

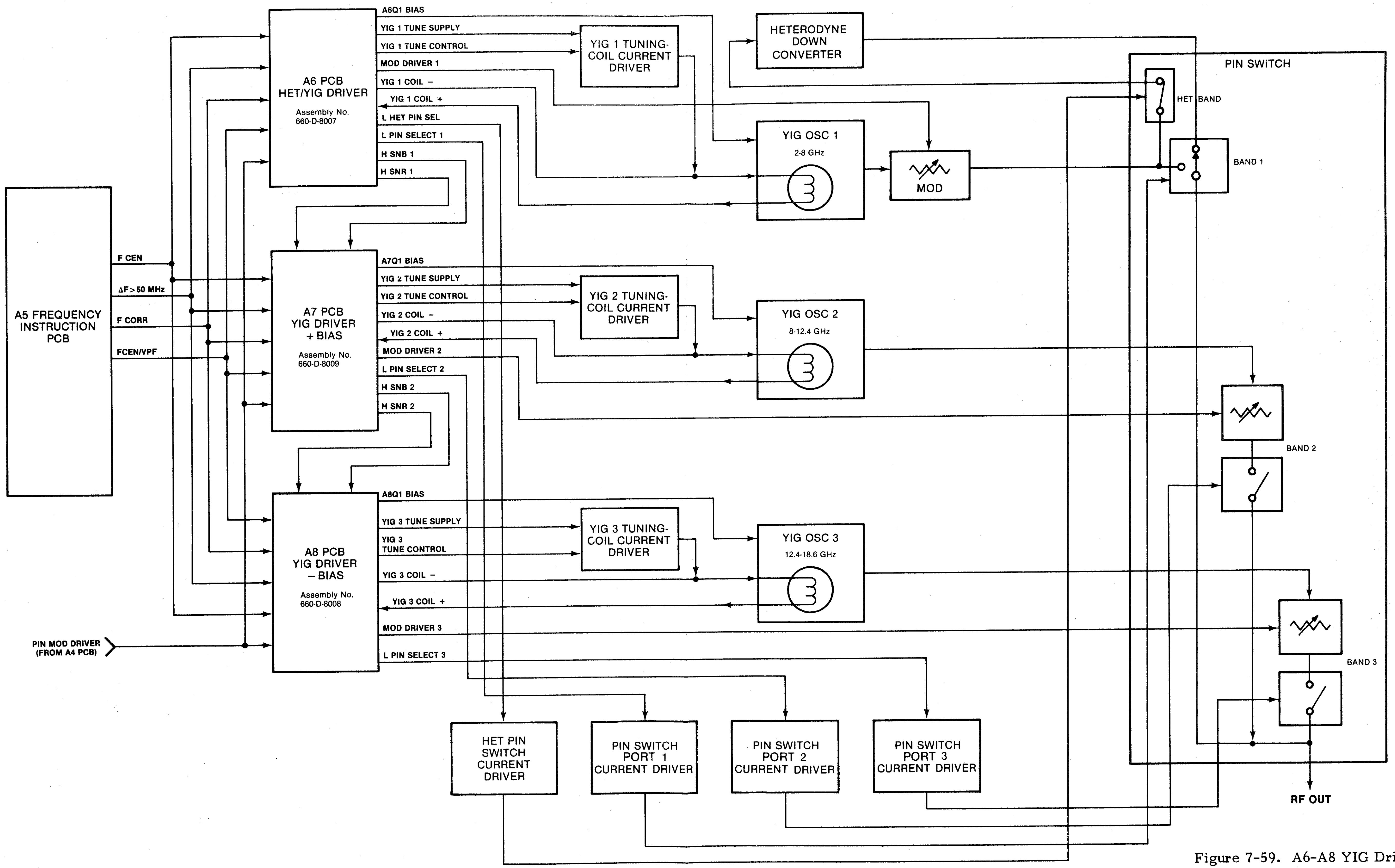


Figure 7-59. A6-A8 YIG Driver PCBs Overall Block Diagram

7-12.2 A6-A9 YIG Driver PCBs, Overall Description

The A6-A9 YIG Driver PCBs provide (1) drive currents for both the PIN switch and the bands 1 thru 4 YIG oscillator tuning coils and (2) modulating currents for the ALC-loop PIN attenuator (paragraph 7-11.1). The PCBs also develop the oscillator-bandswitch logic voltages.

Some 6600A models, such as the 6653A and 6659A, use four YIG oscillators to sweep their frequency range. Each YIG oscillator requires a YIG Driver PCB; consequently, the 6600A sweep generators have four YIG Driver PCB slots: A6-A9. For 6600A models having less than four YIG oscillators, the unused slots contain jumper plugs. To provide for YIG oscillators that have been designed and built by different manufacturers, there are five different YIG Driver PCB designs. Each of these designs is identified by a unique assembly (Assy) number. To further provide for the models different frequency ranges each assembly number contains a dash-number breakout. Table 7-17 tabulates these assembly numbers and relates them to circuit-card slots and model numbers. This table also gives the paragraph number in which the Assy is described.

An example describing how the YIG Driver PCBs interface for multi-YIG models is provided below. This narrative, in conjunction with Figure 7-59 (facing page), describes the A6-A8 YIG Driver PCB operation for the 6647A or 6648A. For this discussion, assume the sweep is starting at 10 MHz.

The three main signals that cause a tuning and bias current to be developed are the **F CEN**, **ΔF>50 MHz**, and **F CORR** signals from the A5 PCB (paragraph 7-12.1). These three signals are applied in parallel to all three YIG driver PCBs. However, because the **H SNB** (select next band) 1 and 2 oscillator-bandswitch lines are both FALSE, the A6 is the only PCB that can use the signals. Here they are summed and used to generate the frequency sweep.

The fourth A5 signal, **FCEN/VPF**, provides for oscillator bandswitching. An A6 bandswitch occurs when 2 GHz is reached and again when 8 GHz is reached. At 2 GHz, **L HET PIN SELECT** goes FALSE and switches the Het Band out and Band 1 to YIG Osc 1. At 8 GHz, several events occur:

- The YIG oscillator tuning coil retunes the oscillator to a rest frequency of 2 GHz.
- The **MOD DRIVER 1** line sets the Mod attenuator to maximum attenuation, and the **L PIN SELECT 1** line causes the PIN Switch's Osc 1 switch to be turned off. This action attenuates by ≥60 dBc the feedthrough of the oscillator 1 signal.
- The **SNB 1** and **SNR 1** oscillator-bandswitch and select-next-ROM lines toggle from LOW to HIGH, causing the Osc 2 YIG and linearizer ROM to be selected.

When Osc 2 is selected, the A7 PCB sums the three signals from A5 (**F CEN, ΔF>50 MHz, F CORR**) and uses them to generate the Osc 2 sweep, starting at 8 GHz. As on A6, the **FCEN/VPF** signal from A5 provides for oscillator bandswitching. The A7 has only one bandswitch point (12.4 GHz) and when it is reached, the following occur:

- The YIG oscillator tuning coil retunes the oscillator to a rest frequency of 8 GHz.
- The **MOD DRIVER** 2 line sets the PIN Switch's Osc 2 attenuator to maximum attenuation, and the **L PIN SELECT 2** line turns the Osc 2 switch off. This action attenuates by ≥60 dBc the feedthrough of the oscillator 2 signal.
- The **SNB** 2 and **SNR** 2 lines toggle from LOW to HIGH and select the Osc 3 YIG and ROM.

The Osc 3 circuit action is similar to that described for Osc 1 and Osc 2. The Osc 3 YIG rest frequency is 12.4 GHz.

Table 7-17. YIG Driver PCB Loading

YIG DRIVER ASSY NO.	PCB SLOT	YIG OSCILLATOR PART NO.	MODEL(S)	CIRCUIT DESCRIPTION PARAGRAPH NO.	SCHEMATIC FIG. NO.
660-D-8007-3	A6	1005-47	6637A, 6647A	7-12.3	7-62
660-D-8007-4	A6	1005-45	6609A	7-12.4	7-67
660-D-8007-5	A6	1005-47	6638A, 6648A	7-12.3	7-62
660-D-8007-6	A6	1005-47	6617A	7-12.5	7-70
660-D-8007-7	A6	1005-47	6653A, 6659A	7-12.3	7-63
660-D-8007-99-91	A6	1005-47	6621A	7-12.3	7-62
660-D-8190-99-96	A6	1005-35	6642A	7-12.6	7-73
660-D-12868-3	A6	1005-47	6637A-40	7-12.3	7-64
660-D-12868-99 -91	A6	1005-47	6621A-40	7-12.3	7-64
660-D-8009-4	A7	1005-53	6637A, 6647A	7-12.7	7-78
660-D-8009-6	A7	1005-53	6638A, 6648A	7-12.7	7-78
660-D-8009-7	A7	1005-54	6637A, 6647A	7-12.7	7-78
660-D-8009-8	A7	1005-54	6638A, 6648A	7-12.7	7-78
660-D-8009-9	A7	1005-53	6653A, 6659A	7-12.7	7-79
660-D-8009-12	A7	1005-54	6653A, 6659A	7-12.7	7-79
660-D-8009-14	A7	1005-53	6637A-40	7-12.7	7-82
660-D-8009-17	A7	1005-53	6637A-40	7-12.7	7-82
660-D-8009-99-92	A7	1005-53	6629A-40	7-12.7	7-82
660-D-8009-99-90	A7	1005-53	6621A-40	7-12.7	7-82
660-D-8191-99-93	A7	1005-40	6642A	7-12.6	7-74
660-D-8009-99-90	A7	1005-53	6621A	7-12.7	7-78
660-D-8009-99-91	A7	1005-53	6629A	7-12.7	7-78
660-D-8008-4	A8	1005-51	6637A, 6647A	7-12.7	7-76
660-D-8008-7	A8	1005-52	6638A, 6648A	7-12.7	7-76
660-D-8008-99-90	A8	1005-55	6629A-40	7-12.7	7-76
660-D-8009-10	A8	1005-51	6653A, 6659A	7-12.7	7-80
660-D-8009-13	A8	1005-59	6653A, 6659A	7-12.7	7-80
660-D-8009-15	A8	1005-55	6637A-40	7-12.7	7-83
660-D-8009-16	A8	1005-59	6637A-40	7-12.7	7-83
660-D-8009-11	A9	1005-61	6653A, 6659A	7-12.7	7-81

7-12.3 Assy 660-D-8007-3, -5, -7, and -99-91; -12868-3 and -99-91 Het/YIG Driver PCBs, Circuit Description

The Het/YIG Driver PCB generates the following voltages and currents:

- A tuning current for the Osc 1 YIG.
- A modulating current for the Osc 1 attenuator (Assy. 660-B-9432), which is located in the Osc 1 YIG output circuit.
- A tracking filter voltage for the Osc 1 YIG. (This filter is mounted inside the Osc 1 YIG package and provides ≥40 dB of harmonic suppression.)
- A fixed bias voltage (-5V) for the Osc 1 YIG.
- Linearizer ROM output data. (A linearizing ROM, if installed, provides correction data for making the frequency characteristics of the YIG oscillator linear.)
- Bandswitch logic voltages.

A block diagram for the Het/YIG PCB is shown in Figure 7-60. A simplified schematic of the E/I (voltage to current) Converter circuit is given in Figure 7-61. The -8007-3, -5, and -99-91 PCB schematic is shown in Figure 7-62. The -8007-7 PCB schematic is shown in Figure 7-63. And the -12868-3, -99-91 schematic is shown in Figure 7-64.

The **F CEN**, **ΔF>50 MHz**, and **F CORR** signals generated on the A5 PCB are summed together at the E/I Converter (Figure 7-61) and used to generate the YIG tuning-coil current. The E/I Converter circuit consists of all the components shown in Figure 7-61. As shown, the three A5 voltage signals are applied to U4, via U3D. If the output frequency is <2 GHz, a heterodyne offset voltage via U3B is also summed in with the A5 voltages. This offset voltage causes the YIG to sweep between 4.61 and 6.6 GHz. When this 4.61 to 6.6 GHz sweep is beat with the output from the 4.6 GHz local oscillator in the Down Converter, a 10 MHz to 2 GHz sweep results.

The output from U4 controls the current through the YIG tuning coil, via transistor A6Q2 (located on the RF Deck). The current through the coil develops a proportional voltage drop across sense resistor (R SENSE) R15.

When the output frequency goes above 2 GHz, a bandswitch occurs. The Bandswitch/ROM Select Logic (Figure 7-60) causes the **L HET YIG SEL** line to go FALSE and open U3B. When U3B opens, the heterodyne offset voltage is removed from the U4 input. The U4 output then causes the YIG to sweep between 2 and 8 GHz.

When the output frequency goes above 8 GHz, the Bandswitch/ROM Select Logic causes the **L YIG SEL** line to go FALSE. When this line goes FALSE, U3D opens and U3A closes. When U3A closes, the R_{fb} (rest) resistor R17 provides the input to U4. This R17 input to U4 causes the YIG coil to tune the oscillator to a rest frequency of 2 GHz. Also, when the **L YIG SEL** line goes FALSE, it causes transistor Q1 to saturate and reverse-bias transistor A6Q3. When A6Q3 is reverse-biased, -15 volts is applied to the emitter of A6Q2. This reduced emitter voltage causes less current to flow through A6Q2 and less heat to be developed across the transistor.

The remaining input to the E/I Converter is the **CW FILTER** line. When the microprocessor commands that the CW filter be inserted, relay K1 is activated. (The CW filter is inserted when the sweep width is ≤50 MHz or when a CW mode has been selected from the front panel.) When K1 is activated, the R27-C16 network creates an alternate path around the YIG oscillator. This path reduces the noise current flowing through the coil, thereby quieting the YIG oscillator frequency output.

As shown in Figure 7-60, the input to the Tracking Filter Voltage Generator (U2A-U2D) is the voltage ramp developed across R Sense (R15). This R15 voltage ramp is modified in slope (gain) and offset (if necessary) and used indirectly to tune the Band 1 YIG tracking filter. If the Band 1 YIG is supplying the output frequency, the **L YIG SEL** line will be TRUE, closing U3C. When U3C closes, it supplies the **TRACK FILTER 1** signal to the A10 PCB, which develops a tuning current for the tracking filter coil.

The inputs to the Bandswitch/ROM Select Logic circuit (U1A, U1B, U1C, U10B, U10C) are the **FCEN/VPF** and **F CEN** voltage signals from the A5 PCB. The **FCEN/VPF** voltage is compared at U9A with a voltage representing 8 GHz and at U9B with a voltage representing 2 GHz. When the **FCEN/VPF** voltage equals or exceeds the 2 GHz voltage at U9B, the L **HET YIG SEL**, **L HET PIN SEL**, and L **HET OFFSET** lines go FALSE. When the **FCEN/VPF** voltage equals or exceeds the 8 GHz voltage at U9A, the L **YIG SEL**, **L YIG 1 SEL**, and L **PIN SELECT** 1 lines go FALSE and the **H SNB 1** line goes TRUE. When the **F CEN** voltage equals or exceeds the 8 GHz voltage at U9C, the H **SNR** 1 line goes TRUE (**L ROM** SEL line goes FALSE).

In addition to the **FCEN/VPF** and F **CEN** analog voltage inputs, there are two logic control inputs to the Bandswitch/ROM Select Logic. These logic control inputs are **L RF OFF** and L **PIN SW OFF.** The L **RF OFF** input is from the microprocessor, via a latch on the A4 PCB. The L **PIN SW OFF** input is from the Sq Wave Sample/Hold Logic circuit on the A4 PCB (paragraph 7-11.1g). When either of these two logic inputs goes TRUE, both the L **HET PIN** SELECT and L **PIN SELECT 1** lines go FALSE.

When the L **HET PIN** SELECT lines is FALSE, it reverse-biases A14CR17 (Figure 7-62, Sheet 3). Reverse-biasing CR17 causes A14Q5 to turn on, A14Q8 to turn on, and A14Q9 to turn off. When on, Q8 sources current into the PIN Switch. This current shunts the RF at J1 to ground and places a high attenuation between J1 and J5 – the RF OUT port.

Conversely, when the L **HET PIN SELECT** line is TRUE (.01-2 GHz Het Band is selected), CR17 is forward-biased. Forward-biasing CR17 causes Q5 to turn off, Q8 to turn off, and Q9 to turn on. When on, Q9 sinks current from the PIN Switch. This current biases the switch so that RF is passed from J1 to J5.

When the L **PIN SELECT 1** line changes states, the circuit composed of A14CR18, A14Q6, Q14Q10, and A14Q11 is used to operate the Osc 1 section of the PIN Switch. The operation of this circuit is identical to that described above for the CR17-Q5-Q8-Q9 circuit.

The inputs to the Linearizing ROM (U5) are the **ROM Bus** lines from the microprocessor, via the A14U6 latch on the motherboard. The Linearizing ROM is enabled by the TRUE state of the L **ROM SEL** line from the Bandswitch Logic circuit. When enabled this ROM outputs eight bits of data to the A5 PCB.

The input to the PIN Driver/Linearizer (ALC) circuit (U7A, U8B, Q6, Q7) is from the A4 PCB. This circuit has two functions: (1) It provides the Band 1 ALC-loop-gain adjustment, and (2) it makes linear the relationship between the A4 PCB Level Amp output in Vdc (paragraph 7-11.1) and the RF power output in dBm. Control for the PIN Driver/Linearizer circuit is provided by the H **YIG SEL** line from the E/I Converter circuit. The **H YIG SEL** line is TRUE when the Band 1 YIG is supplying the output frequency. The output from this circuit is a current, **MOD DRIVER** 1. This current is supplied to the MOD (Modulator) component on the RF Deck, via A14R34 (Figure 7-62, Sheet 3).

The input to the -5V Bias Supply (U7B, U8A, Q3, Q4, Q5) is the control line, **L RF OFF.** When the front panel RF ON switch is disengaged (out), the microprocessor sets this line TRUE. When **L RF OFF** is TRUE, the -5V Bias Supply is turned off; thus turning off the Band 1 YIG oscillator.

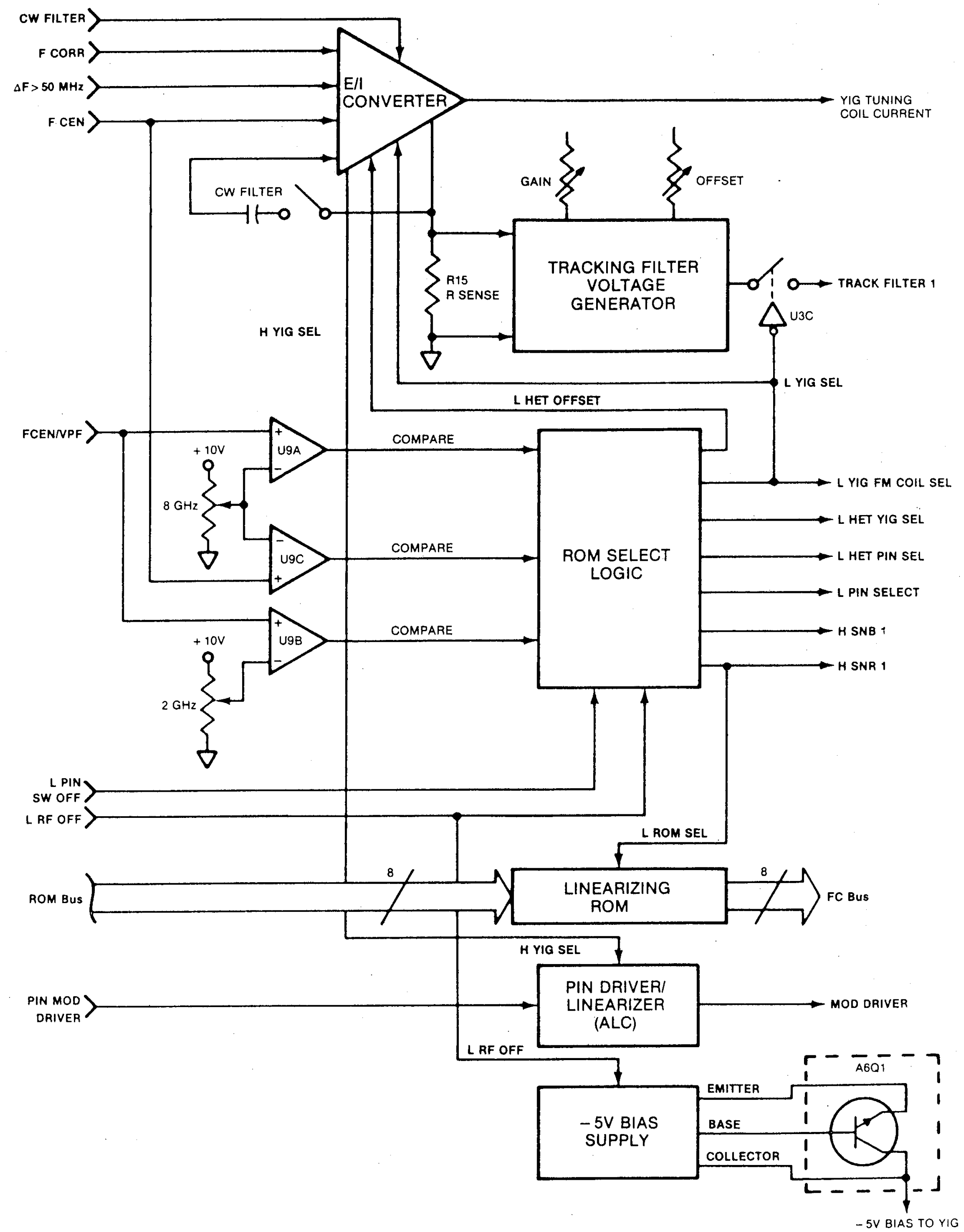


Figure 7-60. A6 Het/YIG Driver PCB (Assy. 660-D-8007 (Block Diagram)

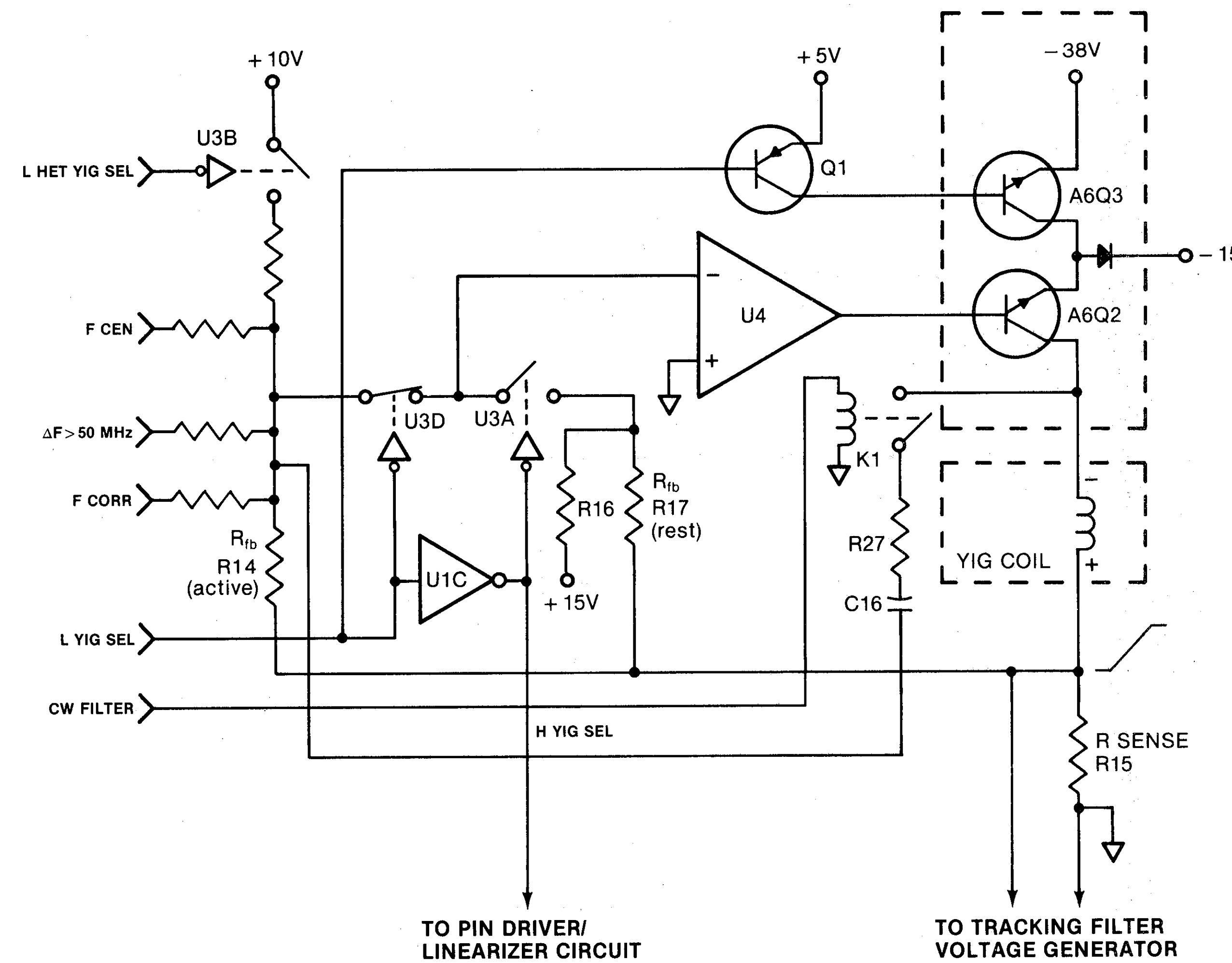


Figure 7-61. A6 Het/YIG Driver PCB E/I Converter Circuit Simplified Schematic

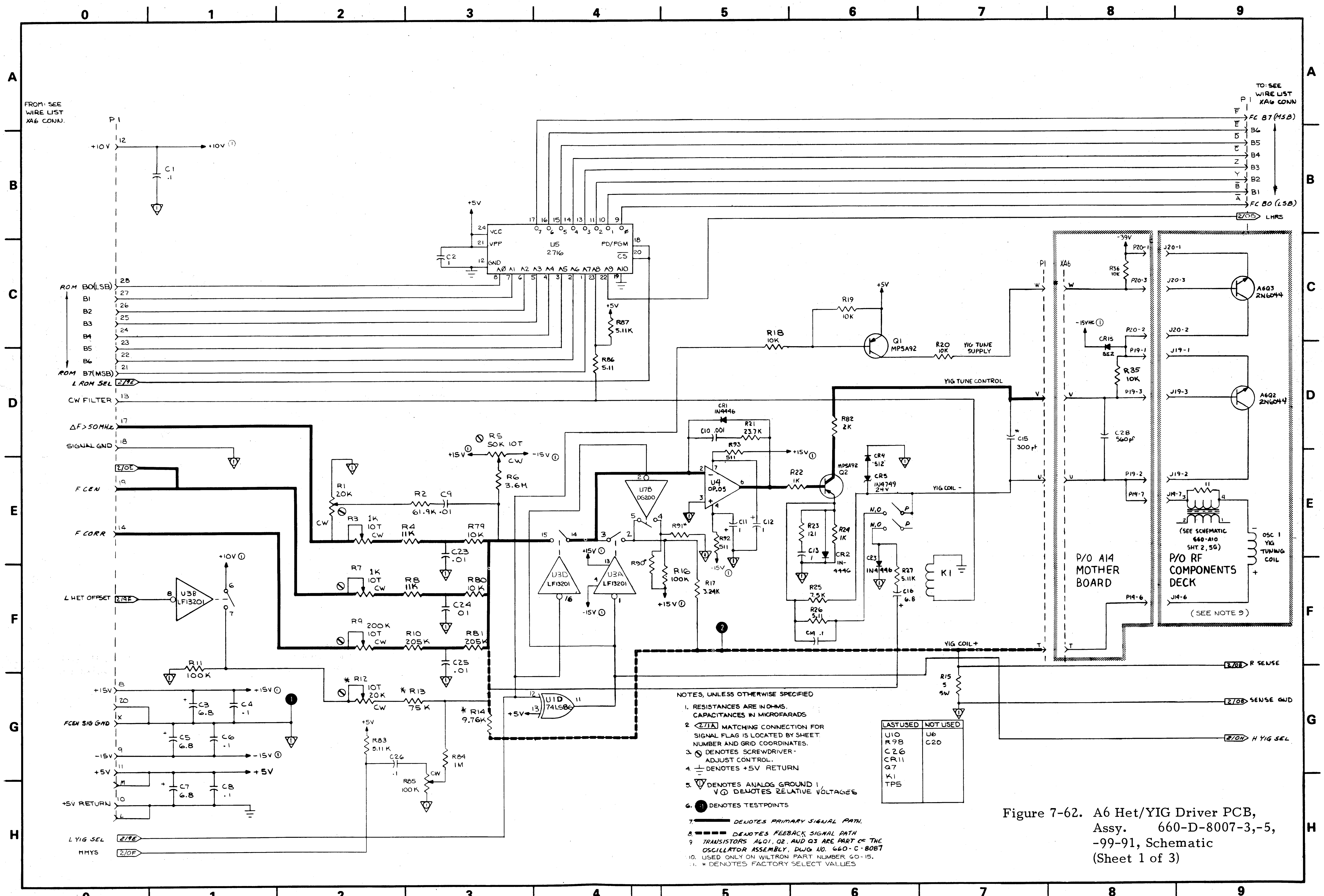
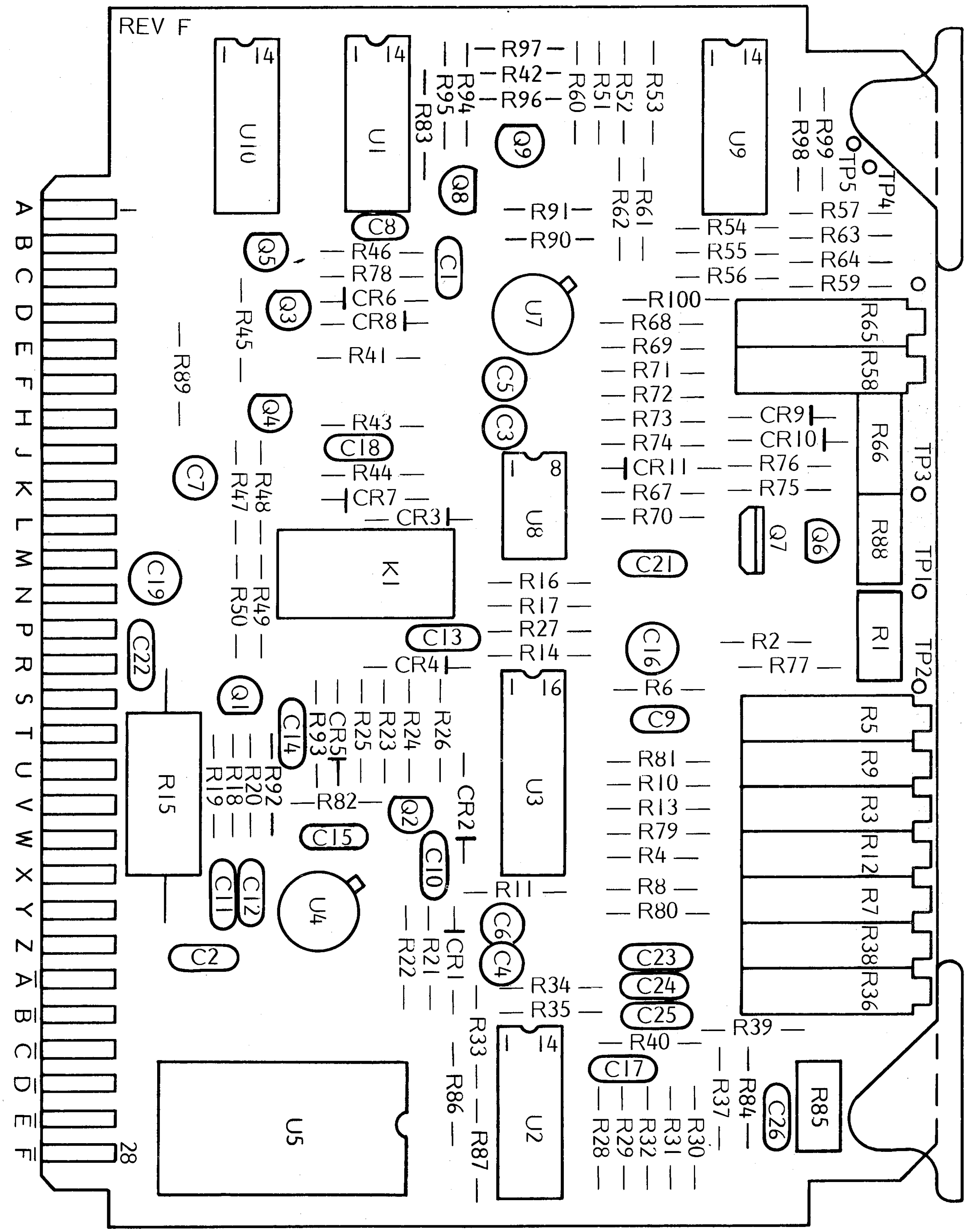


Figure 7-62. A6 Het/YIG Driver PCB, Assy. 660-D-8007-3,-5, -99-91, Schematic (Sheet 1 of 3)

A
B
C
D
E
F
G
H



A6 PCB Parts Locator Diagram

Figure 7-62
(Sheet 1 of 3)

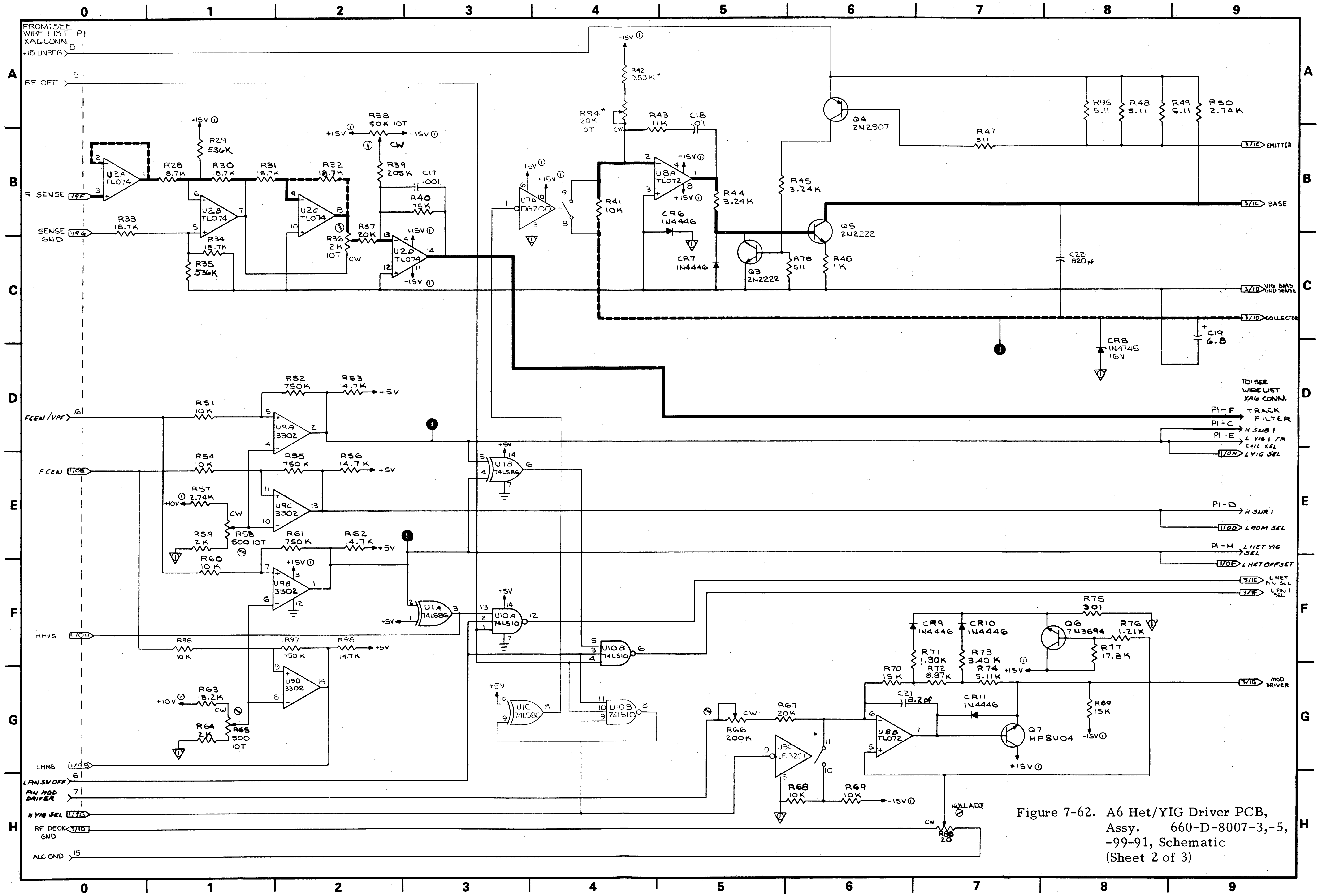


Figure 7-62. A6 Het/YIG Driver PCB, Assy. 660-D-8007-3,-5, -99-91, Schematic (Sheet 2 of 3)

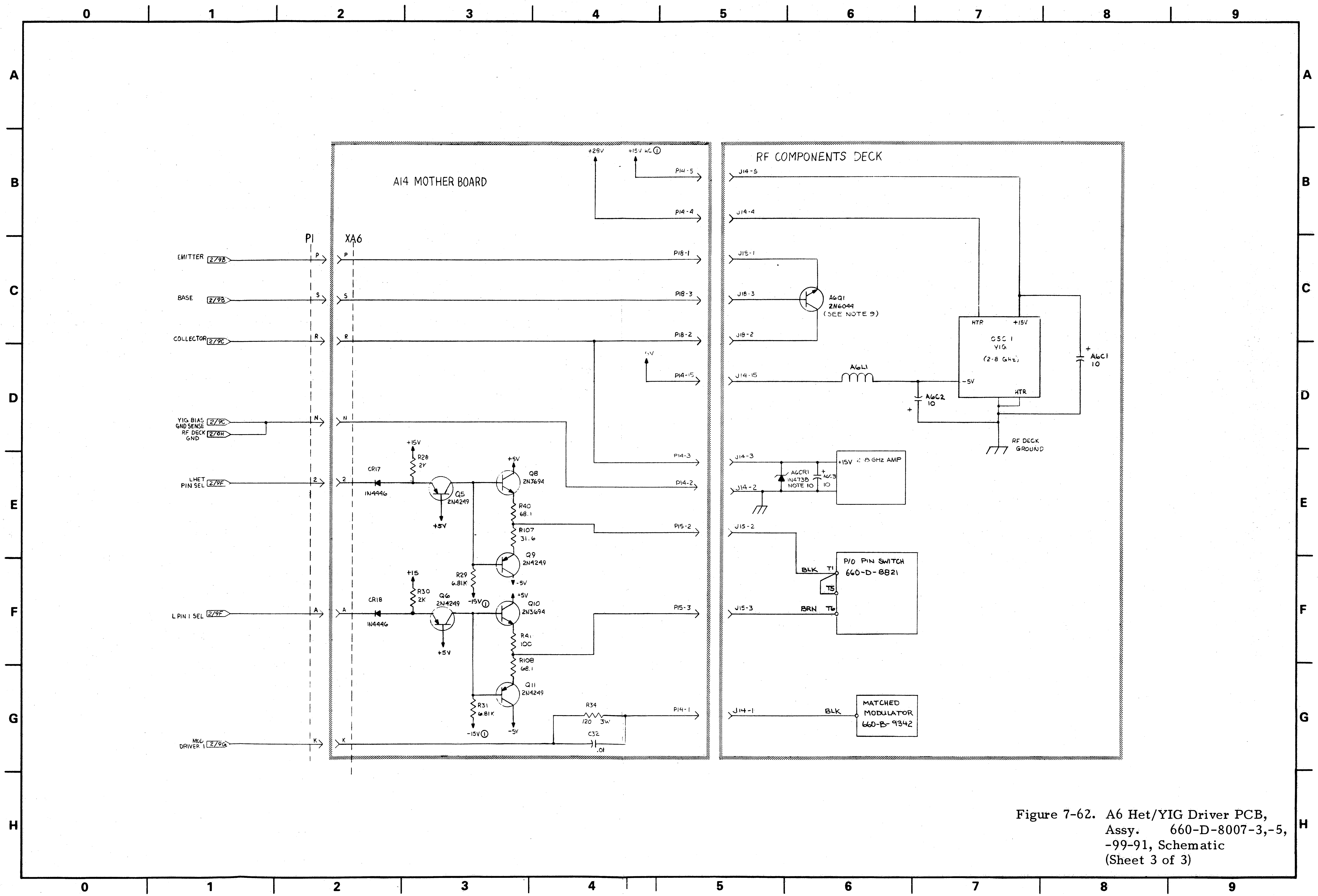
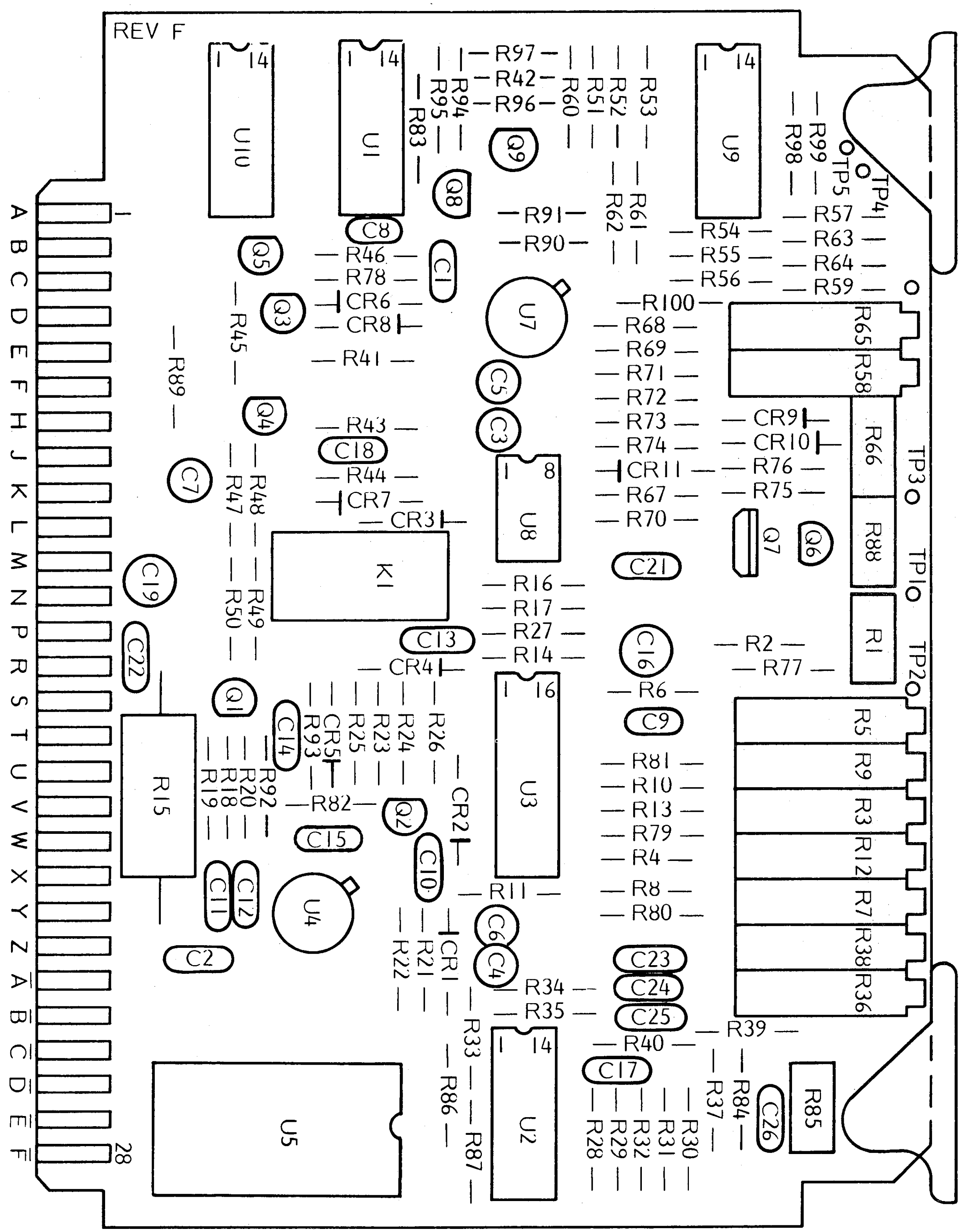
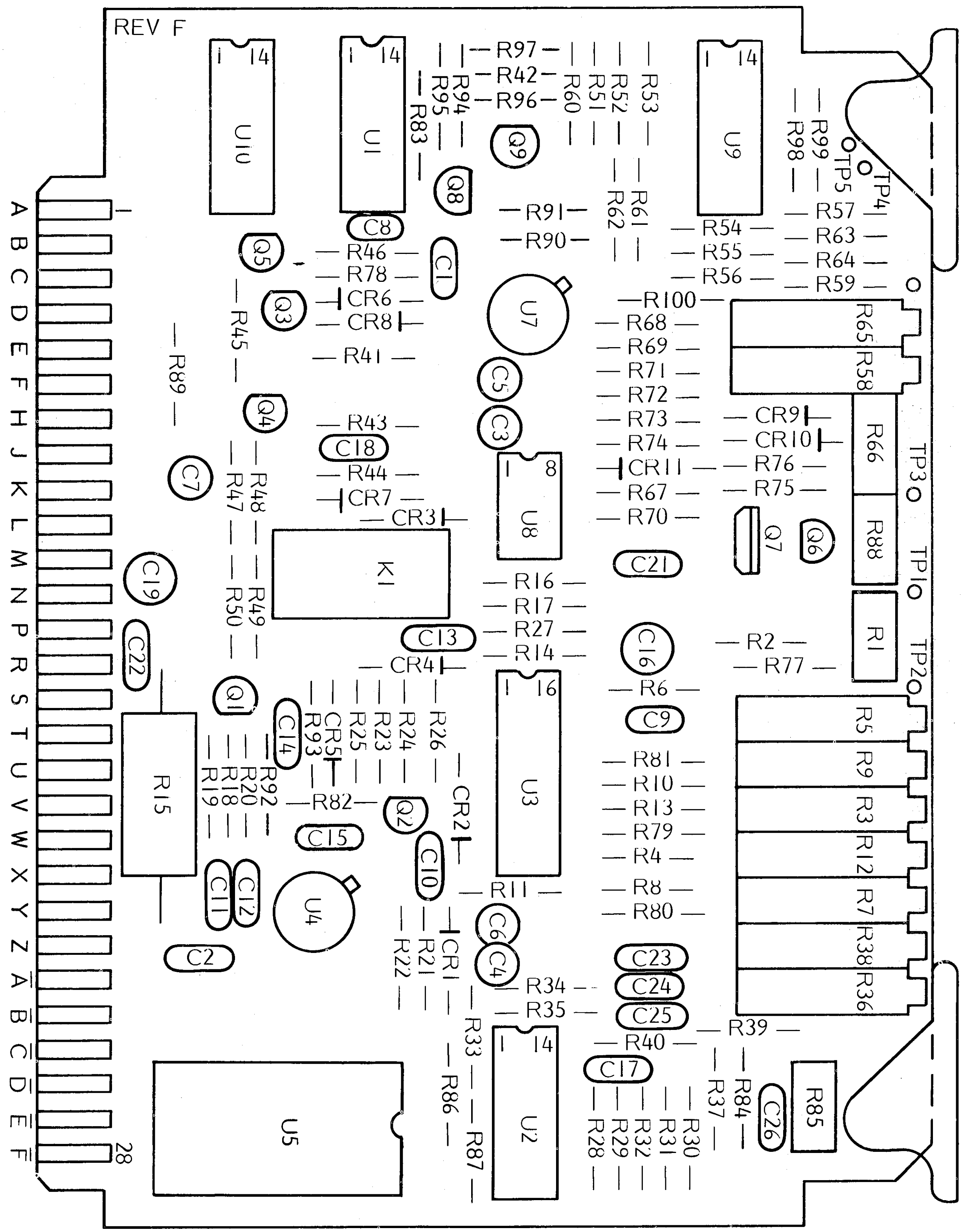


Figure 7-62. A6 Het/YIG Driver PCB, Assy. 660-D-8007-3,-5, -99-91, Schematic (Sheet 3 of 3)

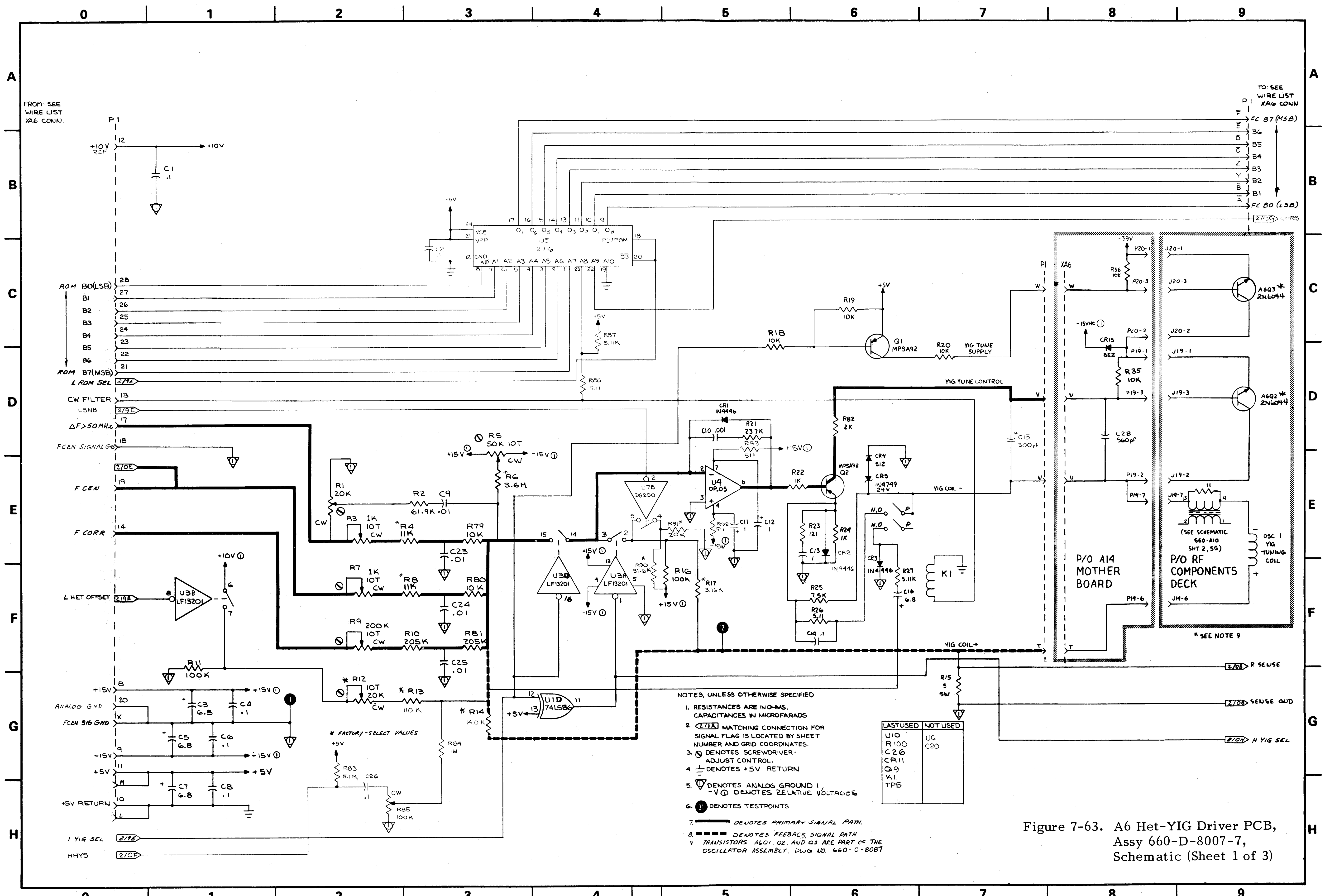


A6 PCB Parts Locator Diagram



A6 PCB Parts Locator Diagram

Figure 7-63
(Sheet 1 of 3)



NOTES, UNLESS OTHERWISE SPECIFIED

1. RESISTANCES ARE IN OHMS, CAPACITANCES IN MICROFARADS
2. [2/1A] MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
3. ⊘ DENOTES SCREWDRIVER-ADJUST CONTROL.
4. ⏚ DENOTES +5V RETURN
5. ▽① DENOTES ANALOG GROUND 1, -V① DENOTES RELATIVE VOLTAGES
6. ● DENOTES TESTPOINTS
7. ━━━ DENOTES PRIMARY SIGNAL PATH.
8. ▬ ▬ ▬ DENOTES FEEBACK SIGNAL PATH
9. TRANSISTORS A601, Q2, AND Q3 ARE PART OF THE OSCILLATOR ASSEMBLY, DWG NO. 660-C-8087

LAST USED	NOT USED
U10	U6
R100	C20
C26	
CR11	
Q9	
K1	
TP5	

Figure 7-63. A6 Het-YIG Driver PCB, Assy 660-D-8007-7, Schematic (Sheet 1 of 3)

parts locator

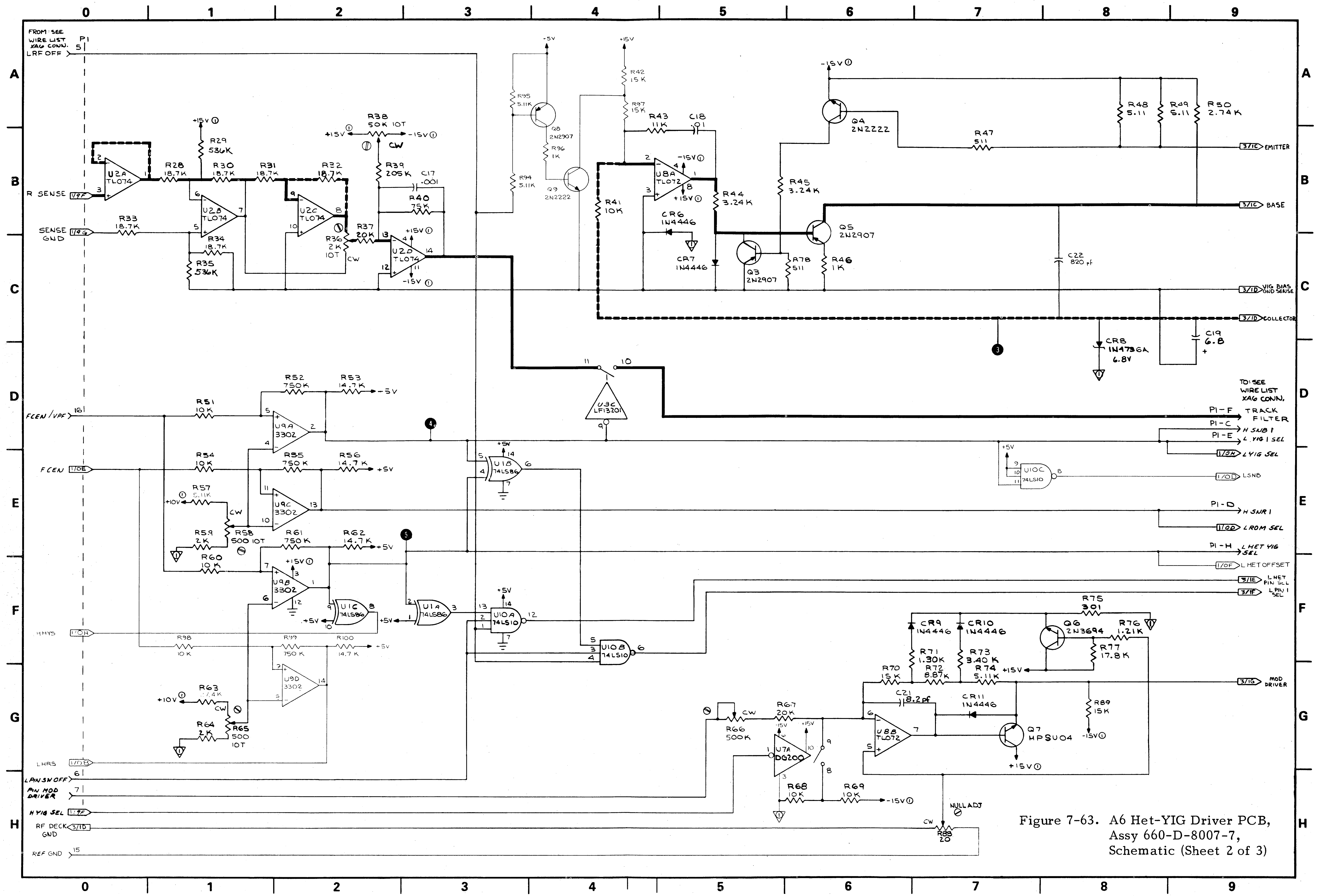
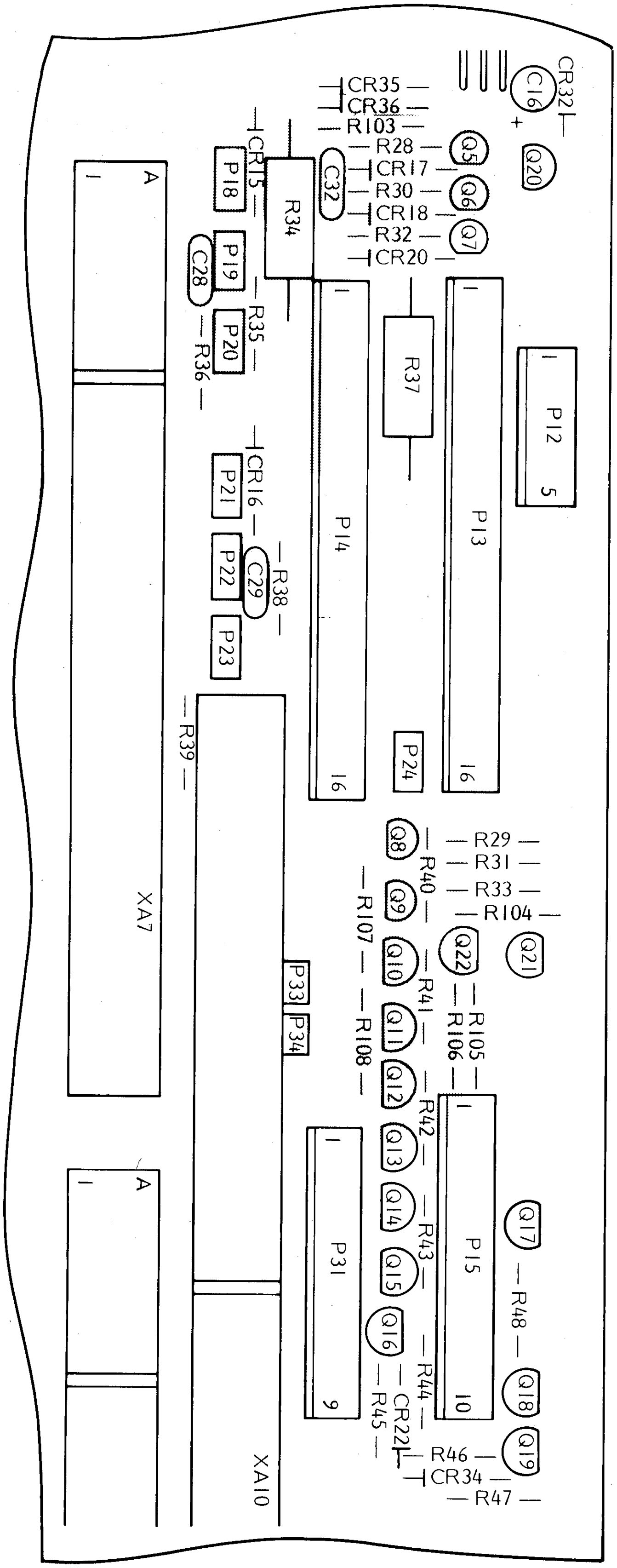
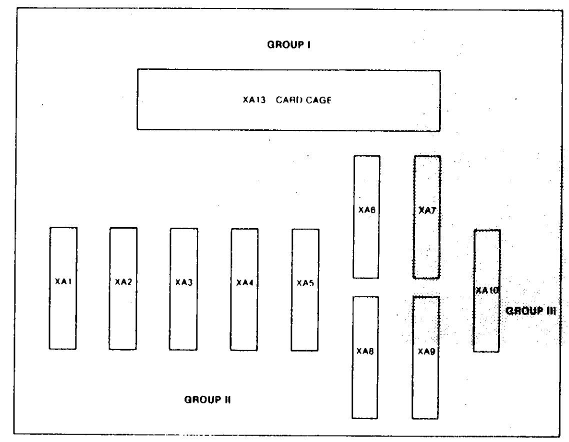


Figure 7-63. A6 Het-YIG Driver PCB, Assy 660-D-8007-7, Schematic (Sheet 2 of 3)





Osc 1 YIG, PIN Driver, and PIN/Modulator Parts Locator Diagram

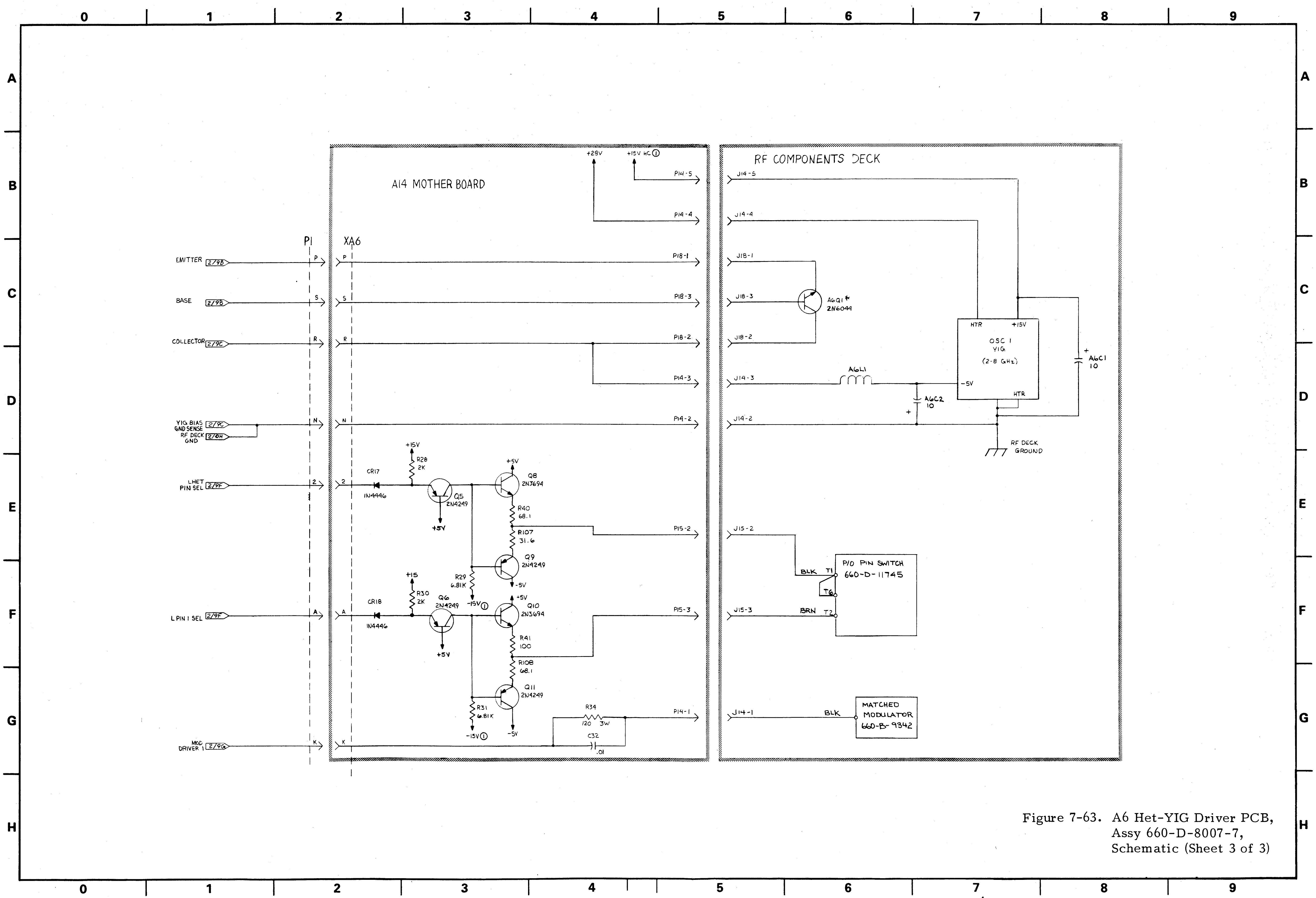
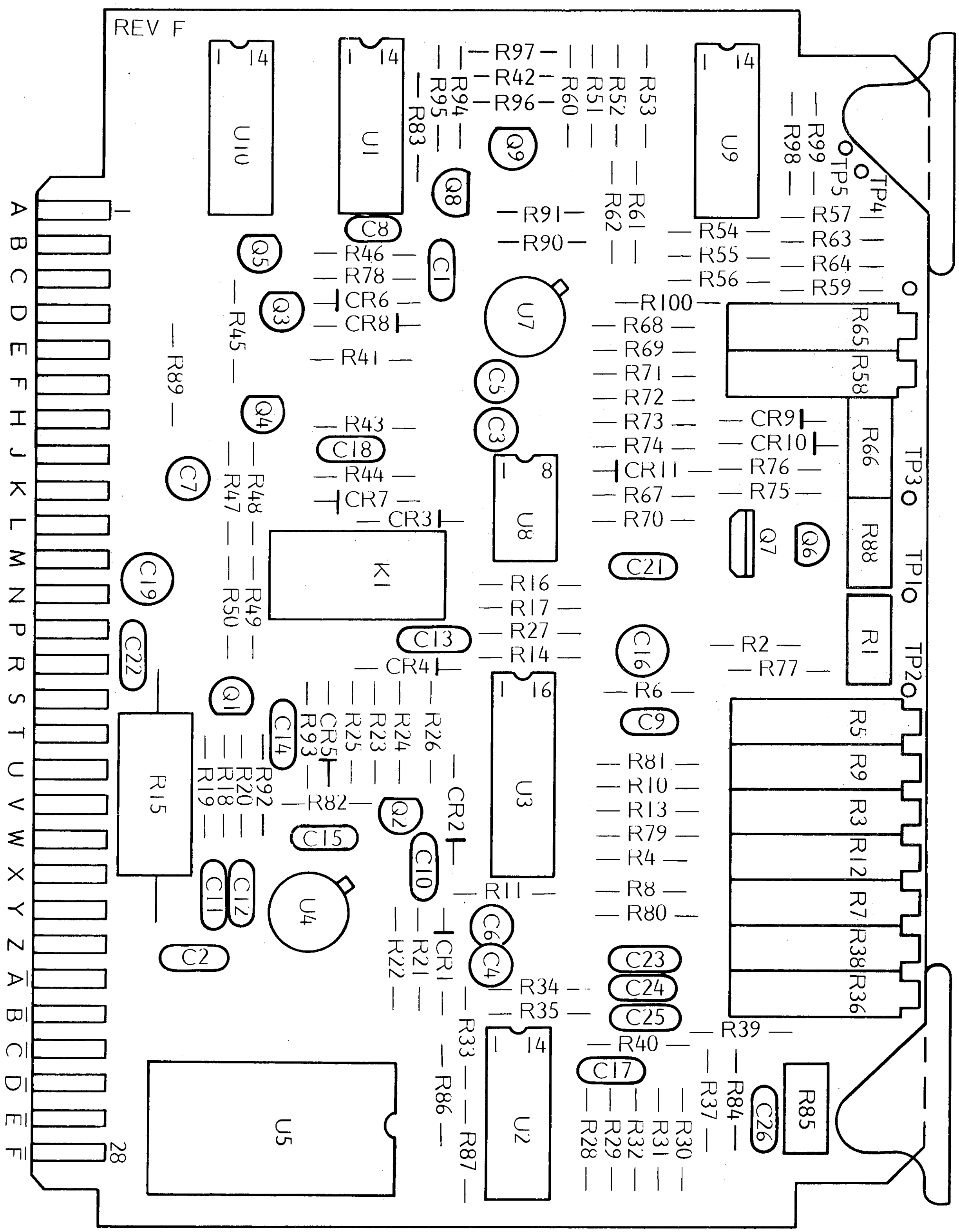
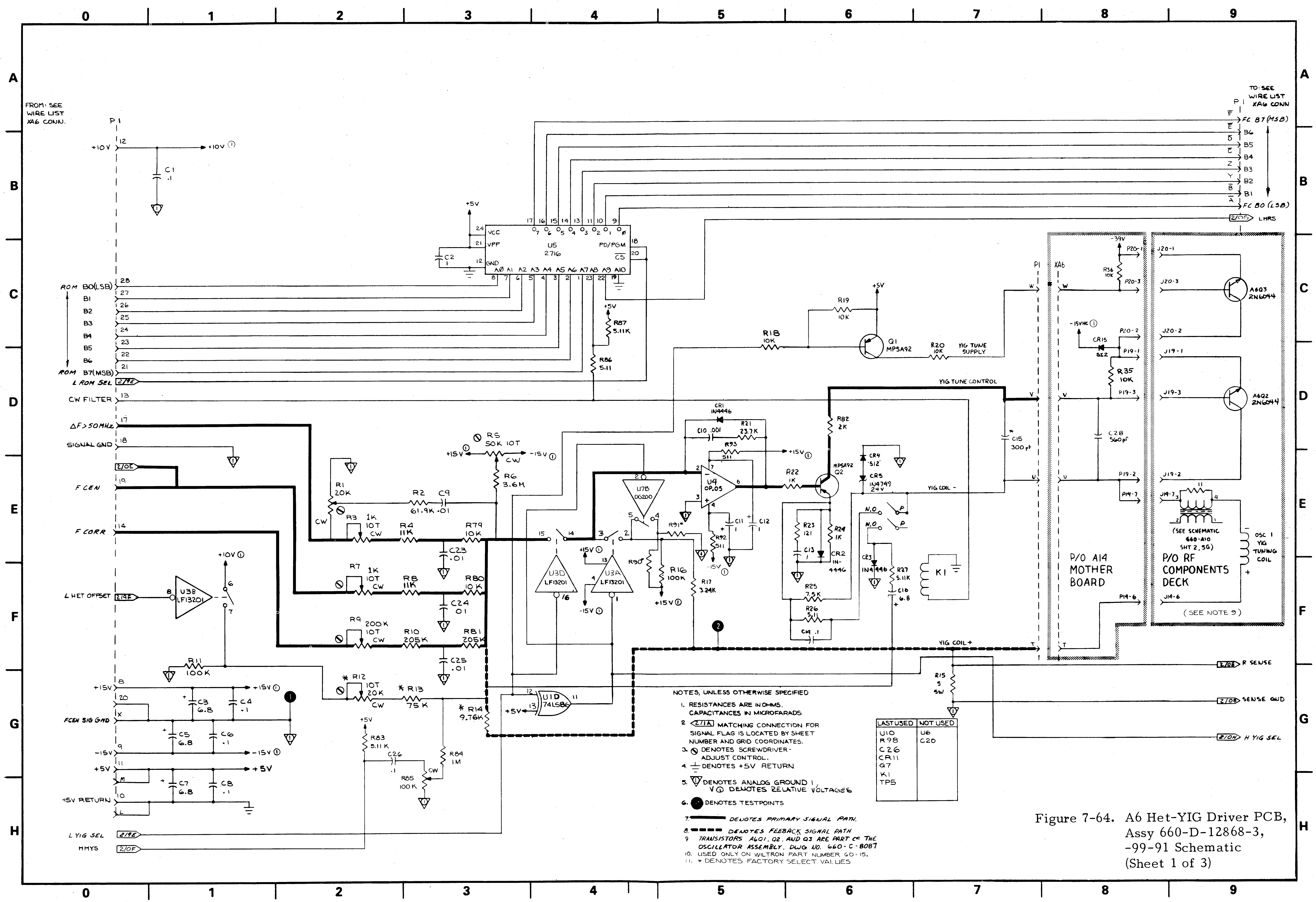


Figure 7-63. A6 Het-YIG Driver PCB, Assy 660-D-8007-7, Schematic (Sheet 3 of 3)

parts locator



A6 PCB Parts Locator Diagram



NOTES, UNLESS OTHERWISE SPECIFIED

1. RESISTANCES ARE IN OHMS, CAPACITANCES IN MICROFARADS
2. <2/1A] MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
3. ⦸ DENOTES SCREWDRIVER-ADJUST CONTROL.
4. ⏚ DENOTES +5V RETURN
5. ▽① DENOTES ANALOG GROUND 1, V① DENOTES RELATIVE VOLTAGES
6. ● DENOTES TESTPOINTS
7. ▬▬ DENOTES PRIMARY SIGNAL PATH.
8. ■■■■ DENOTES FEEBACK SIGNAL PATH
9. TRANSISTORS A6Q1, Q2, AND Q3 ARE PART OF THE OSCILLATOR ASSEMBLY, DWG NO. 660-C-8087
10. USED ONLY ON WILTRON PART NUMBER 60-15.
11. * DENOTES FACTORY SELECT VALUES

LAST USED	NOT USED
U10	U6
R98	C20
C26	
CR11	
Q7	
K1	
TP5	

Figure 7-64. A6 Het-YIG Driver PCB, Assy 660-D-12868-3, -99-91 Schematic (Sheet 1 of 3)

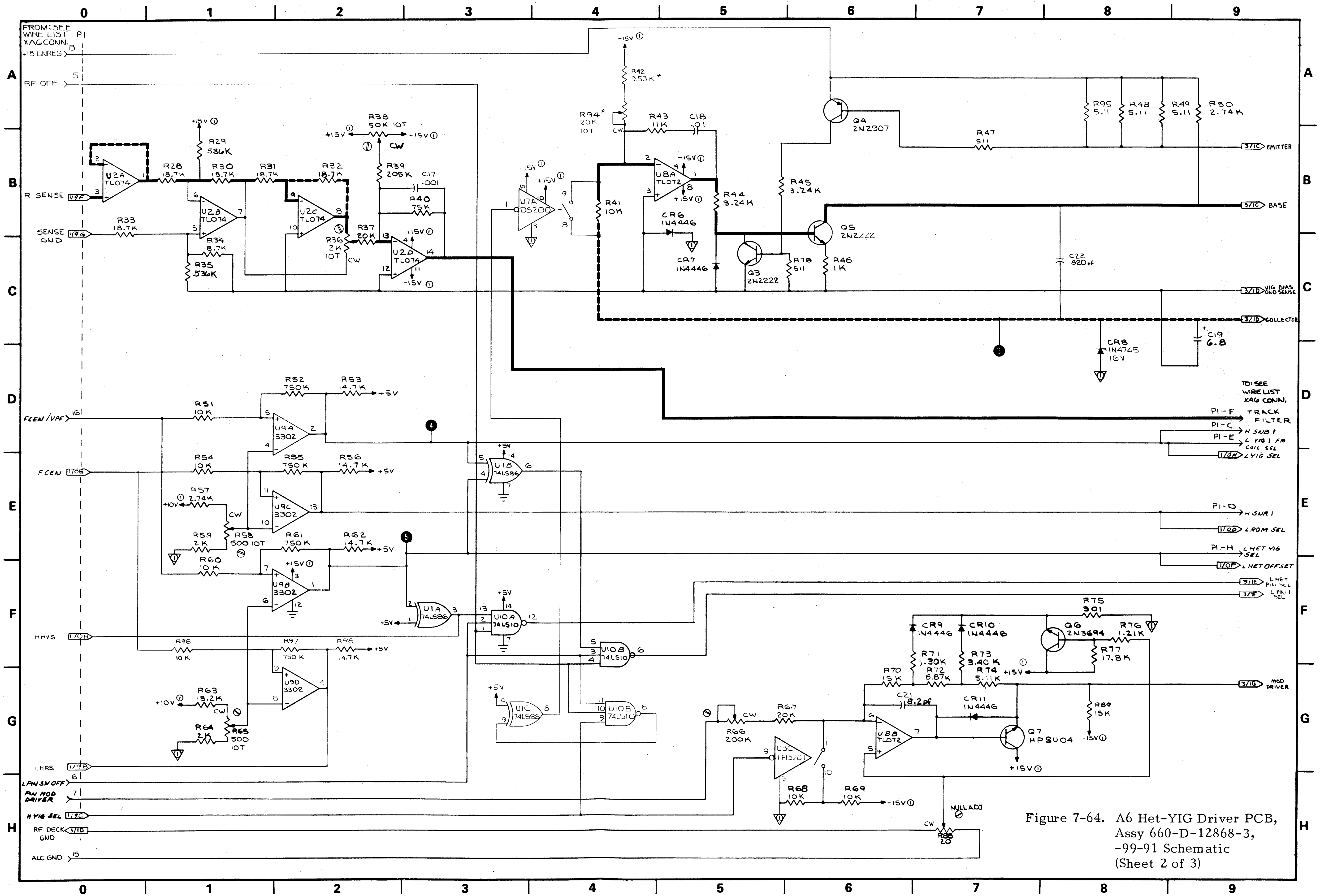


Figure 7-64. A6 Het-YIG Driver PCB, Assy 660-D-12868-3, -99-91 Schematic (Sheet 2 of 3)

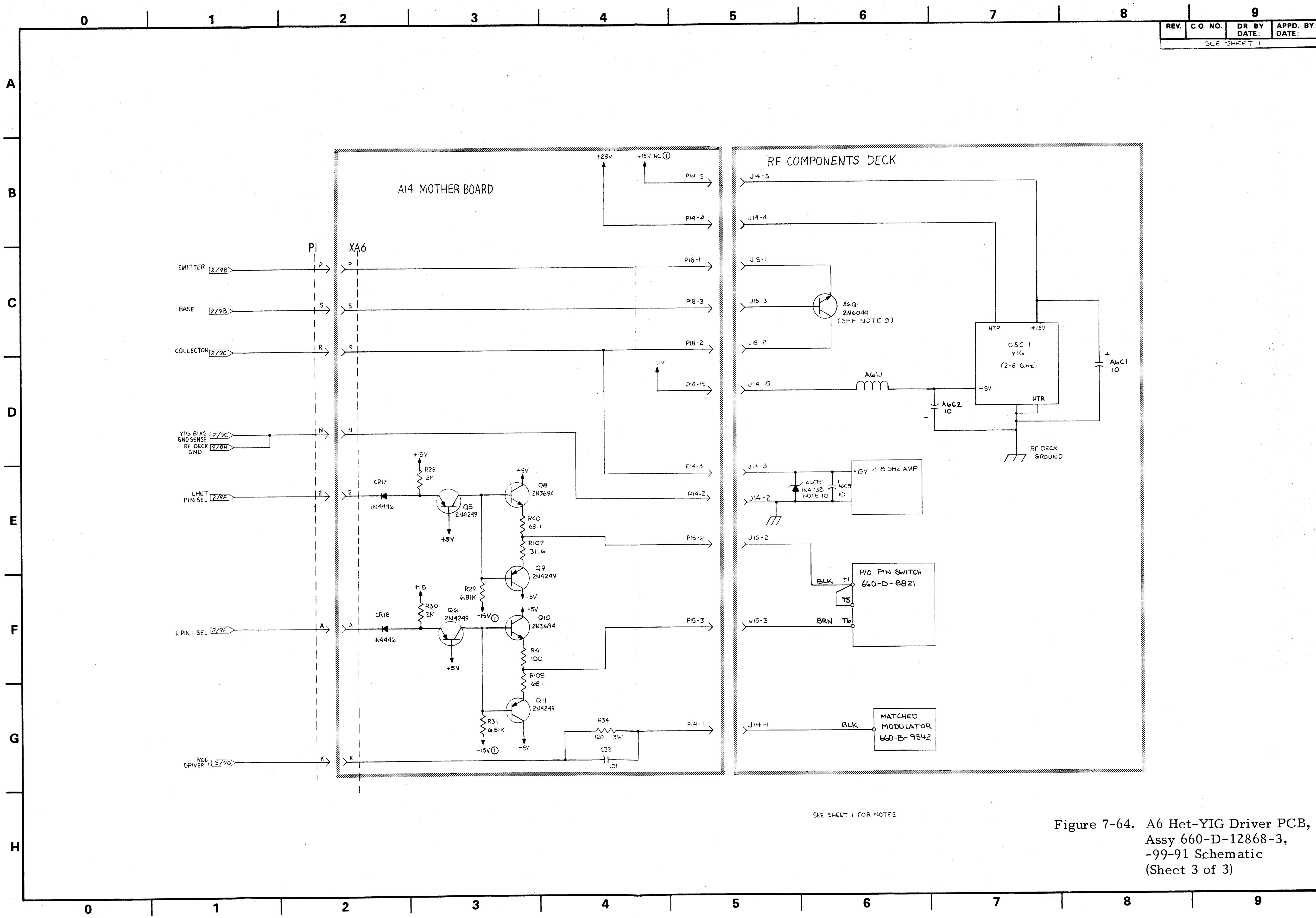
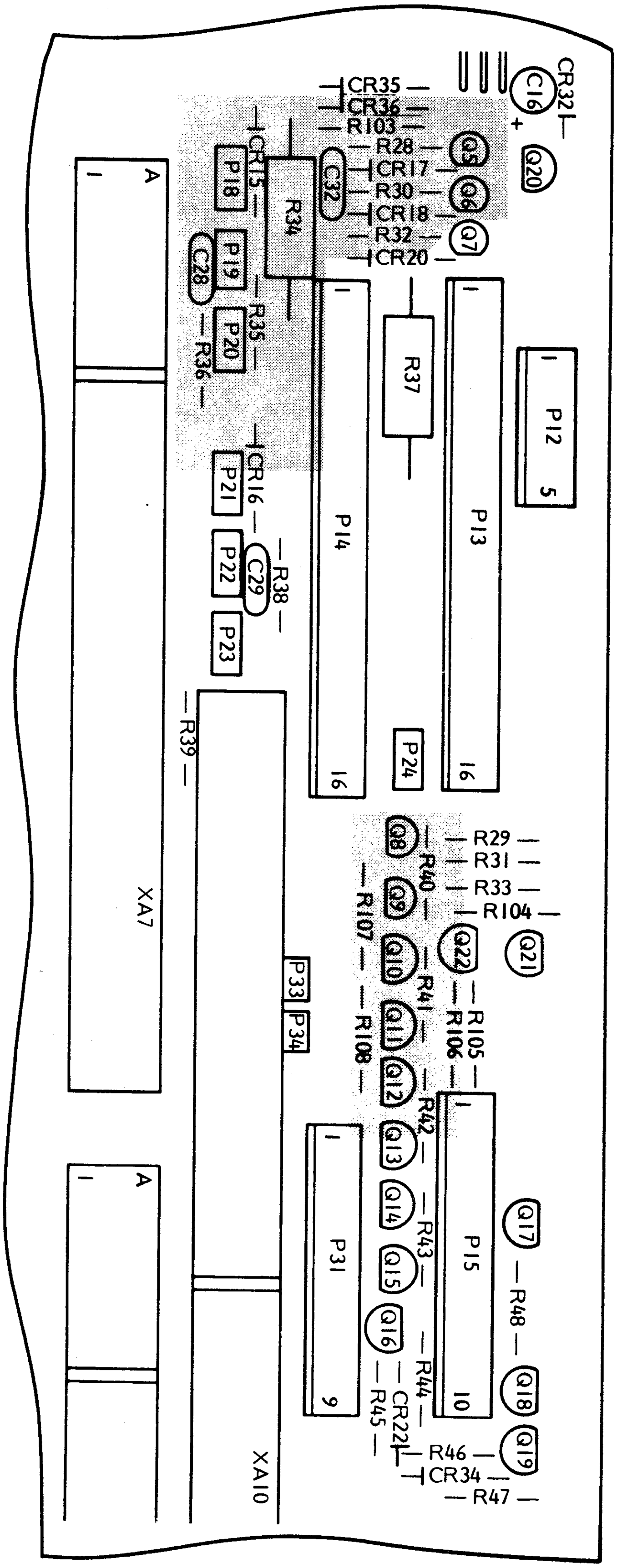
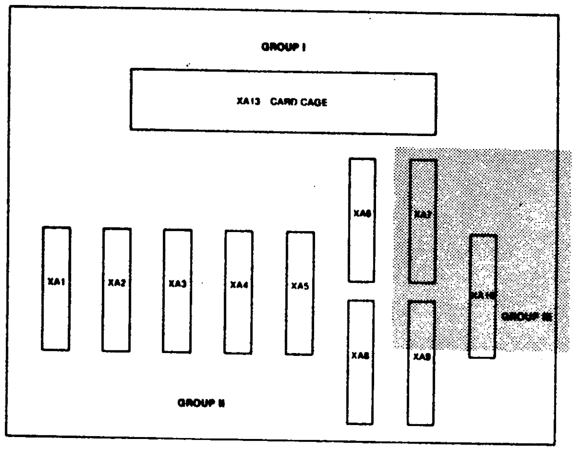


Figure 7-64. A6 Het-YIG Driver PCB, Assy 660-D-12868-3, -99-91 Schematic (Sheet 3 of 3)





Osc 1 YIG, PIN Driver, and PIN/Modulator Parts Locator Diagram

7-12.4 Assy 660-D-8007-4 Het/YIG Driver PCB, Circuit Description

The Het/YIG Driver PCB provides the drive current and bias voltage for the 4.61 to 6.6 GHz YIG oscillator, which is heterodyned with a 4.6 GHz fixed oscillator to generate the .01 to 2 GHz output frequency. The A6 PCB also provides the following:

- A modulating current for the MOD 1 (Modulator) component.
- A switching current for the MOD 2 (PIN Switch) component.
- Linearizing ROM output data. (A linearizing ROM, if installed, provides frequency correction data for making the frequency characteristics of the YIG oscillator linear.)

A block diagram for the Het/YIG Driver PCB is shown in Figure 7-65. A simplified schematic of the E/I (voltage to current) Converter circuit is shown in Figure 7-66. And the PCB schematic (3 sheets) is provided in Figure 7-67.

The F **CEN, ΔF>50 MHz,** and F **CORR** signals generated on the A5 PCB are summed together at the E/I Converter (Figure 7-65) and used to generate the YIG tuning coil current. The output of this YIG is a sweeping frequency, 4.61 to 6.6 GHz. This sweeping output is applied to a mixer in the Heterodyne Converter Assembly, where it is beat with a 4.6 GHz oscillator. The mixer product, a sweep .01 to 2 GHz, is amplified and applied to the RF output circuit (paragraph 7-14).

As shown in Figure 7-66, the three A5 voltage signals – along with a heterodyne offset voltage via R12 – are applied to U4. The output from U4 controls the current through the YIG tuning coil, via transistor A6Q2 (located on the RF Deck). (-38V is applied to the emitter of A6Q2 via A6Q3, which is used as a voltage switch in other 6600A Series models.) The current through the YIG coil develops a proportional voltage drop across sense resistor (R SENSE) R15.

The remaining input to the E/I Converter is the **CW FILTER** line. When the microprocessor commands that the CW filter be inserted, relay K1 is activated. (The CW filter is inserted when the sweep width is ≤50 MHz or when a CW mode has been selected from the front panel.) When K1 is activated, the R27-C16 network creates an alternate negative-feedback path around the YIG oscillator. This path reduces the noise current flowing through the coil; thereby quieting the YIG oscillator frequency output.

As shown in Figure 7-65, the voltage developed across R15 provides the input for the Tracking Filter Voltage Generator (U2A-U2D). This circuit is not presently used with the 6609A.

The PIN/YIG Select Logic circuit (Figure 7-65) (U1A, U1B, U1C, U10A, U10B) controls the logic states of the **L YIG SEL, L HET YIG SEL, L HET PIN SEL,** and **L PIN SELECT** lines. The **L YIG FM COIL SEL** line is always TRUE. The **L HET YIG SEL** line is always TRUE. And the **L HET PIN SEL** and **L PIN SELECT** lines may be either TRUE or FALSE, depending upon the logic states of the input **L RF OFF** and **L PIN SW OFF** lines. The **L RF OFF** input is from the microprocessor, via a latch on the A4 PCB. The **L PIN SW OFF** input is from the Sq Wave Sample/Hold Logic circuit on the A4 PCB (paragraph 7-11.1g). When either of these two logic inputs goes TRUE, both the **L HET PIN SEL** and **L PIN SEL** lines go FALSE.

When the **L HET PIN SEL** line is FALSE, it reverse-biases A14CR17 (Figure 7-67, Sheet 3). Reverse-biasing CR17 causes A14Q5 to turn on, A14Q8 to turn on, and A14Q9 to turn off. When on, Q8 sources current into the MOD (PIN Switch).

Conversely, when the **L HET PIN SEL** Line is TRUE, CR17 is forward-biased. Forward-biasing CR17 causes Q5 to turn off, Q8 to turn off, and Q9 to turn on. When on, Q9 sinks current from the MOD (PIN Switch).

Sourcing current into MOD 2 (PIN Switch) effectively "opens" the RF output circuit. Conversely, sinking current from the switch "closes" the circuit. This switch is used to apply square-wave modulation to the RF output energy.

Para. 7-12.4 (cont'd.)

The inputs to the Linearizing ROM (U5) are the **ROM Bus** lines from the microprocessor, via the A14U6 latch on the motherboard. The Linearizing ROM is enabled by the TRUE state of the **L ROM SEL** line from the Bandswitch Logic circuit. This ROM outputs eight bits of data to the A5 PCB. This circuitry is not presently used with the 6609A.

The input to the PIN Driver (ALC) circuit (U7, U8, Q6, Q7) is from the A4 PCB. This circuit has two functions: (1) It provides the ALC-loop-gain adjustment, and (2) it makes linear the relationship between the A4 PCB Level Amp output in Vdc (paragraph 7-11.1) and the RF power output in dBm. The output from this circuit is a current: **MOD DRIVER.** This current is supplied to MOD 1 on the RF Deck, via A14R34 (Figure 7-65, Sheet 3).

The input to the -5V Bias Supply (U7A, U8A, Q3, Q4, Q5) is the control line, **L RF OFF.** When the front panel RF ON switch is disengaged (out), the microprocessor sets this line TRUE. When **L RF OFF** is TRUE, the -5V Bias Supply is turned off, thus turning off the YIG oscillator.

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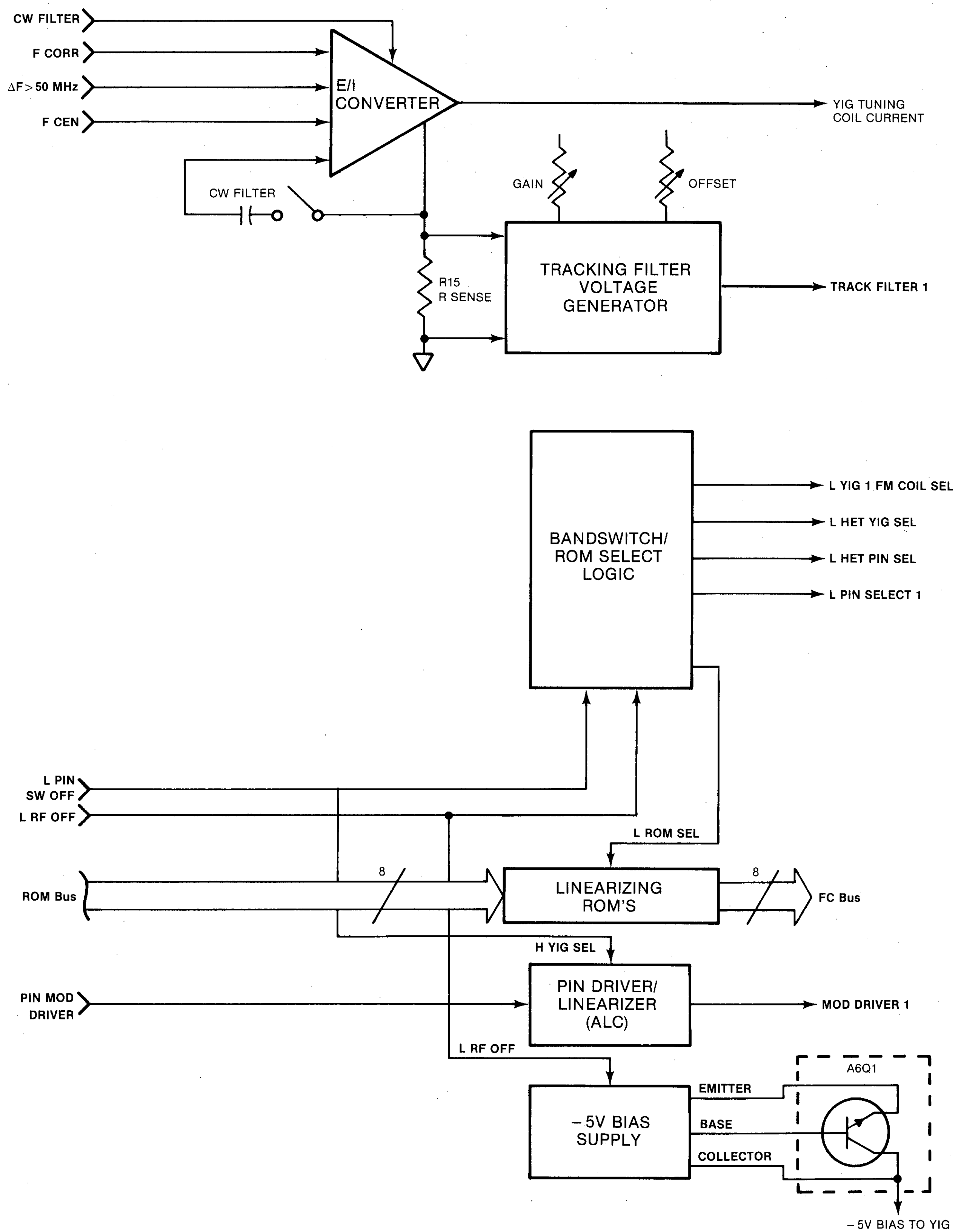


Figure 7-65. Assy 7007-4 YIG Driver PCB Overall Block Diagram

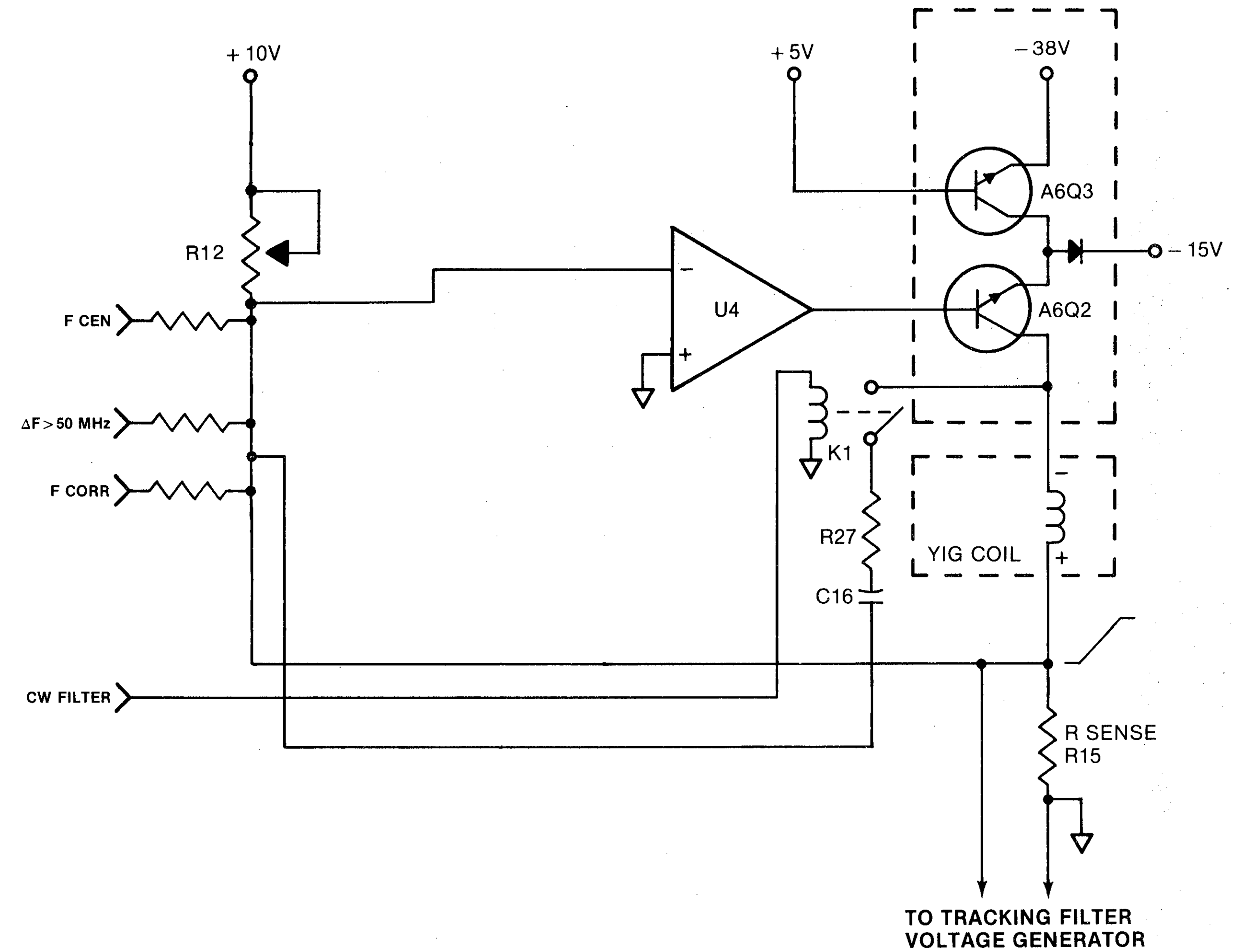
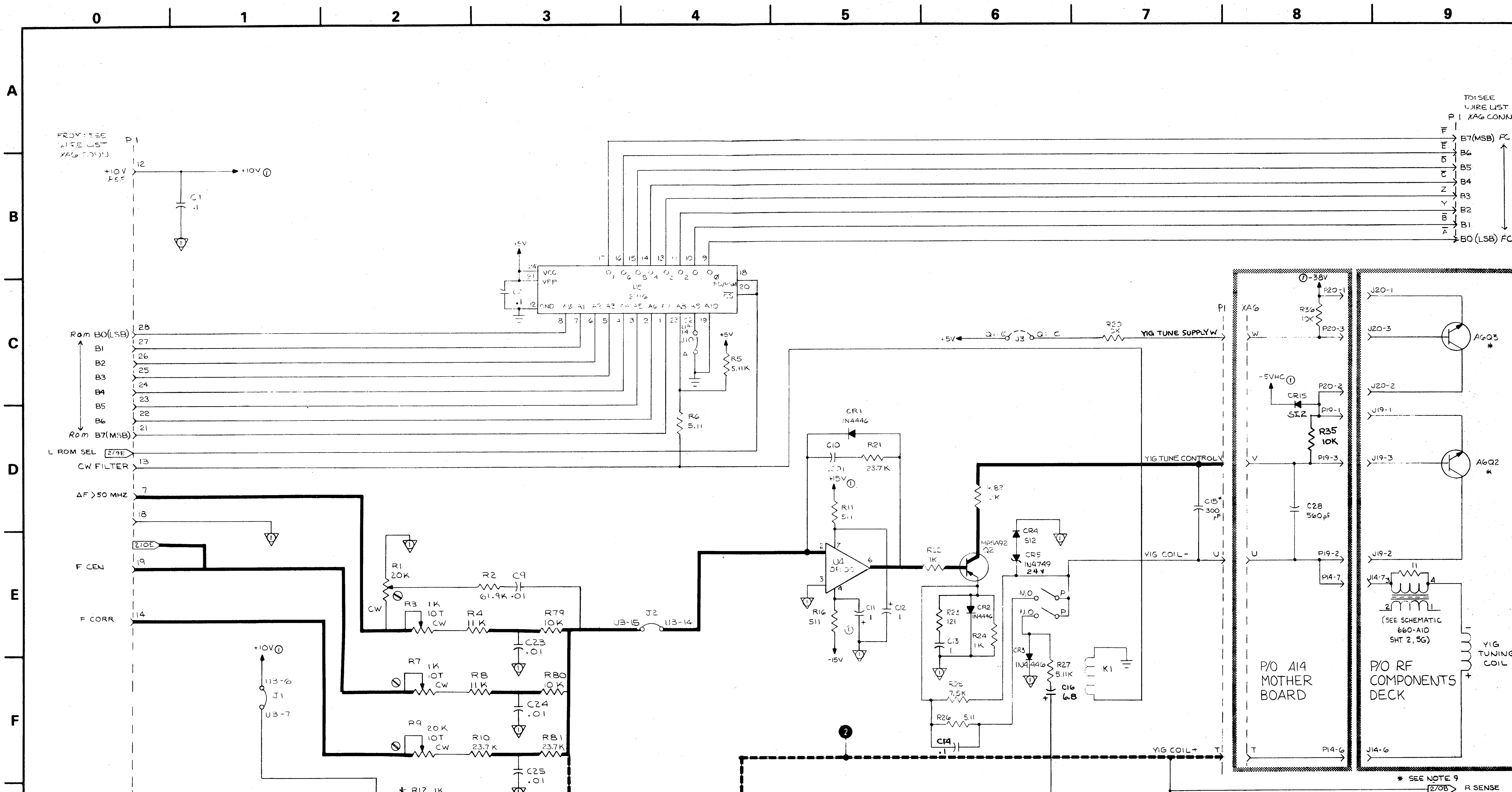


Figure 7-66. Assy. 8007-4 E/I Converter Simplified Schematic

Figure 7-65



NOTES: UNLESS OTHERWISE SPECIFIED

1) RESISTANCES ARE IN OHMS.
CAPACITANCES ARE IN MICROFARADS.
INDUCTANCES ARE IN MICROHENRIES.

2) 2/0C MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.

3) ⊘ DENOTES SCREWDRIVER ADJUST.

4) ❾ DENOTES TEST POINTS.

5) ▬▬ DENOTES PRIMARY SIGNAL PATH.

6) ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.

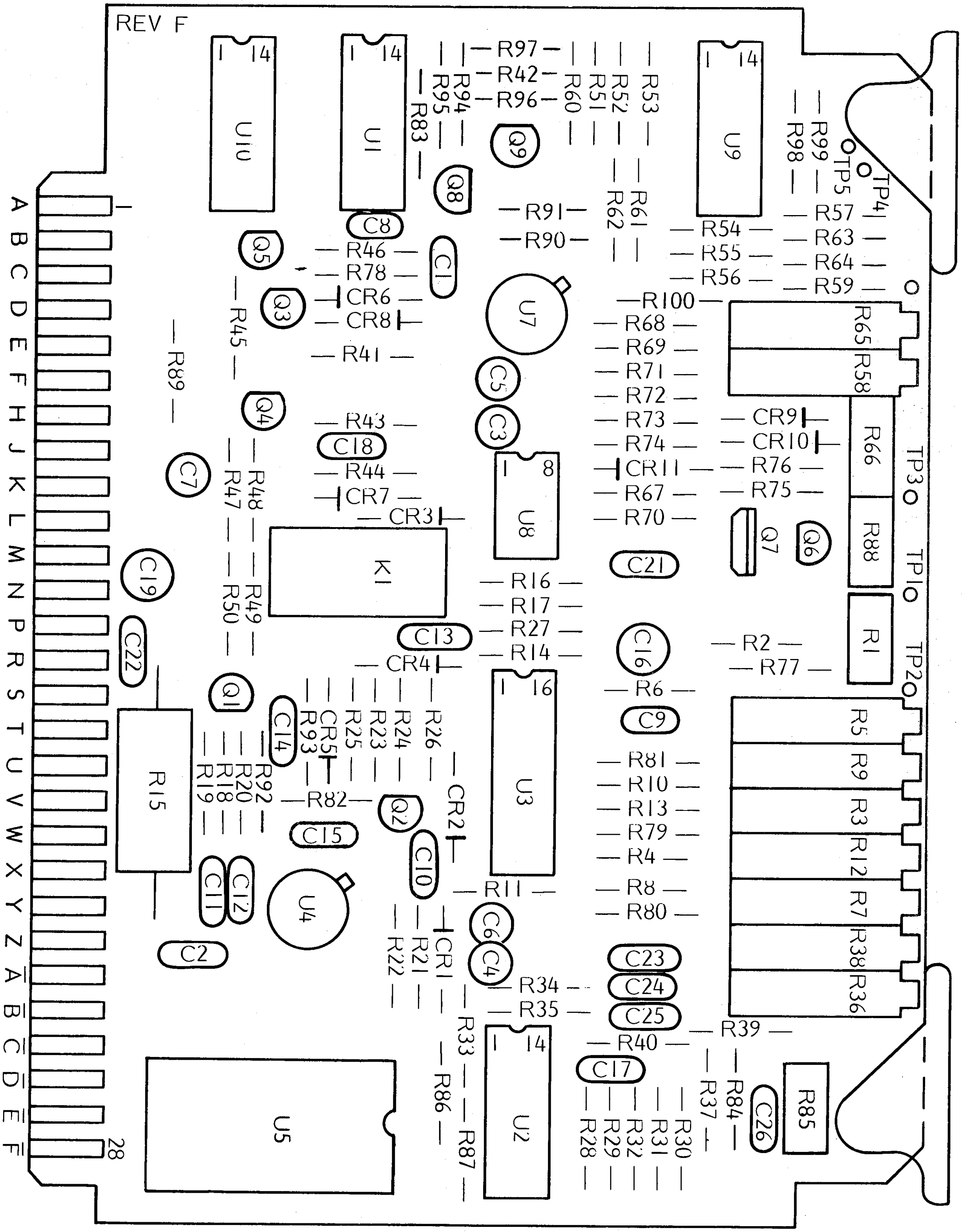
7) DENOTES +5V RETURN.

8) DENOTES ANALOG GROUND 1, AND $-V_{(1)}$ DENOTES RELATIVE VOLTAGES.

9) TRANSISTORS A6Q1, Q2, AND Q3 ARE PART OF THE OSCILLATOR ASSEMBLY DWG NO. 660-C-8172

LAST USED	NOT USED
U10 R89 C25 CR11 Q9 K1 TP5 J10	R28-40, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 68, 69, 83, 84, 85, 86, 87, U1, U2, U3, U6, U7, U9, C17, C20

Figure 7-67. A6 HET/YIG Driver PCB, Assy. 660-D-8007-4, Schematic (Sheet 1 of 3)



A6 PCB Parts Locator Diagram

Figure 7-67
(Sheet 1 of 3)

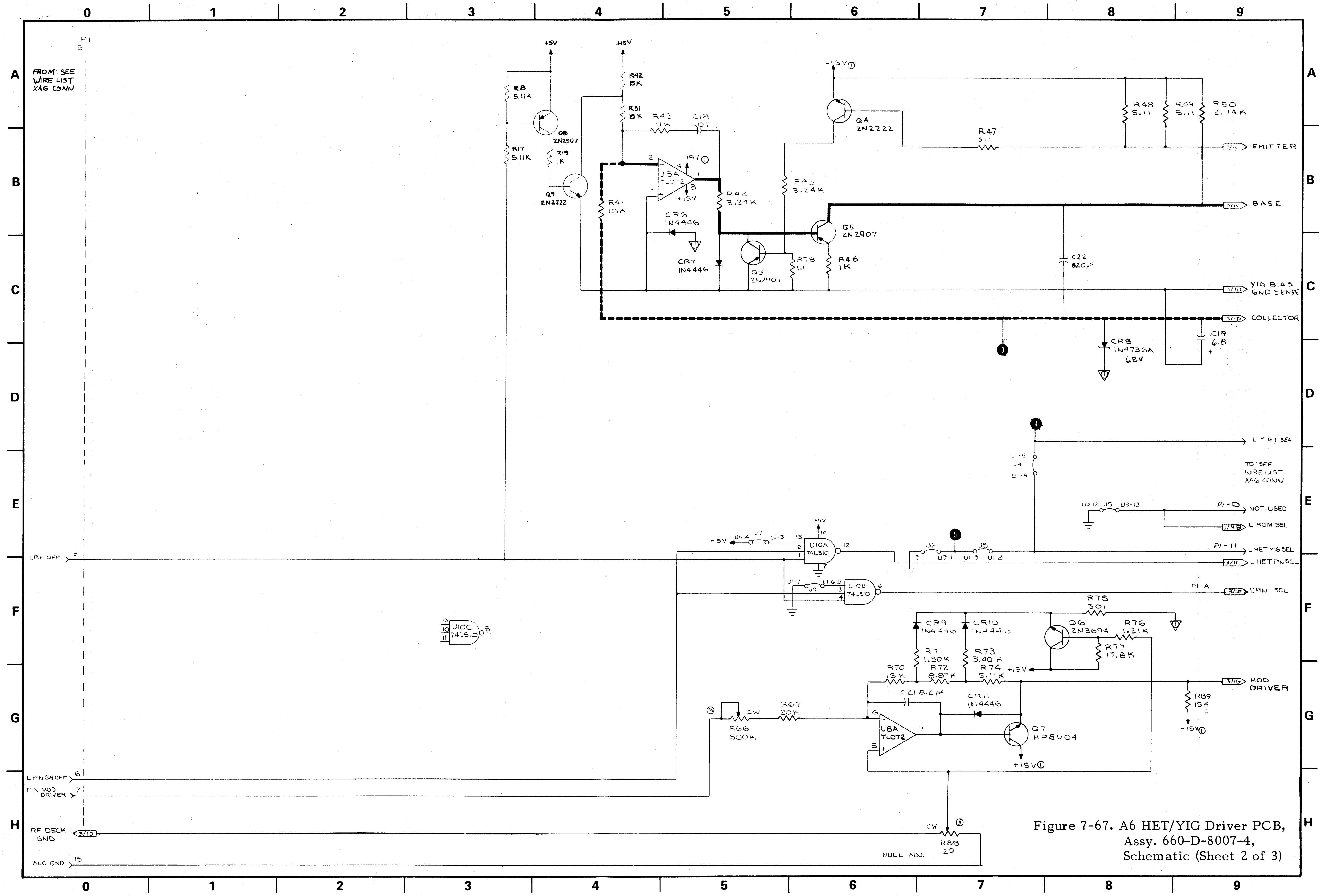


Figure 7-67. A6 HET/YIG Driver PCB, Assy. 660-D-8007-4, Schematic (Sheet 2 of 3)

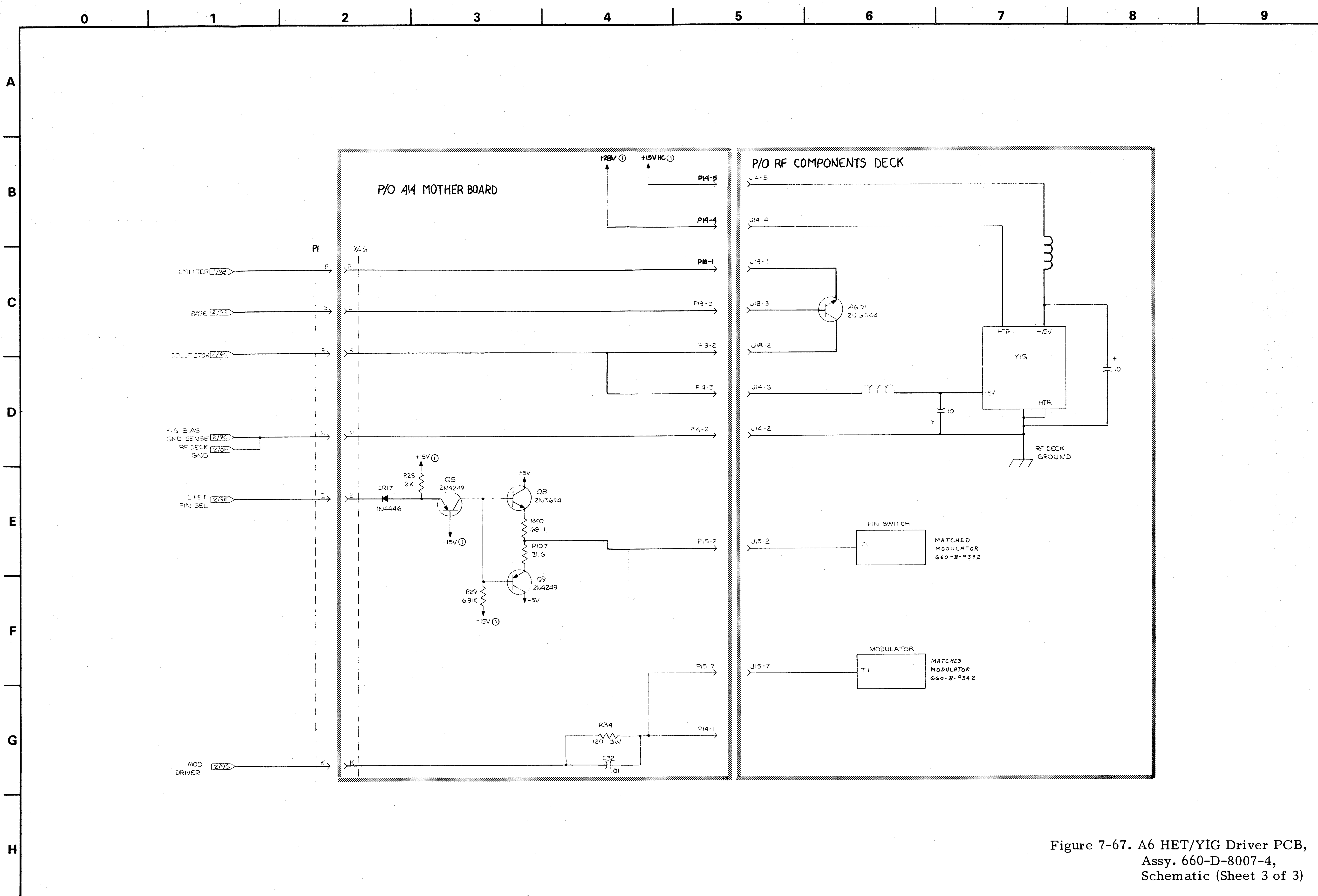
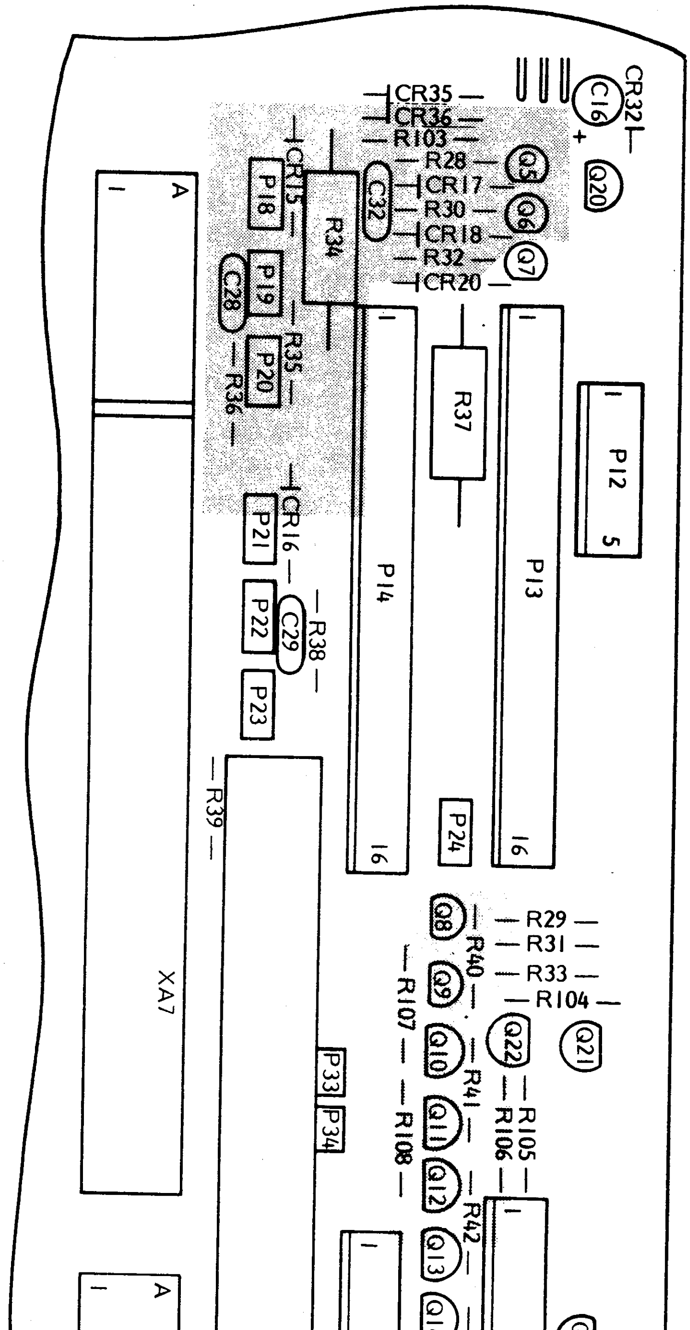
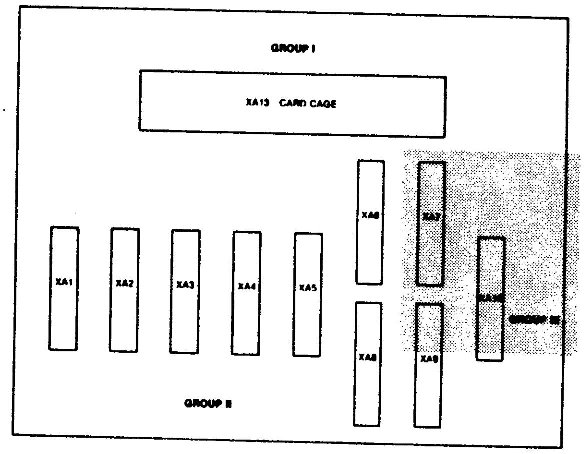


Figure 7-67. A6 HET/YIG Driver PCB, Assy. 660-D-8007-4, Schematic (Sheet 3 of 3)





Osc 1 YIG, PIN Driver, and PIN/Modulator Parts Locator Diagram

7-12.5 Assy 660-D-8007-6 Het/YIG Driver PCB, Circuit Description

The Het/YIG Driver PCB generates the drive current and bias voltage for the 2 to 8 GHz YIG oscillator. The PCB also provides the following:

- A modulating current for the MOD (Modulator) component.
- A switching current for the DPDT (PIN) switch.
- A sweeping voltage for the tracking filter located within the YIG oscillator housing.
- Linearizing ROM output data. (The Linearizing ROM, if installed, provides frequency-correction data for making the frequency characteristics of the YIG oscillator linear.)
- Bandswitch logic voltages.

A block diagram for the Het/YIG Driver PCB is shown in Figure 7-68. A simplified schematic of the E/I (voltage to current) Converter circuit is shown in Figure 7-69. And the PCB schematic (3 sheets) is provided in Figure 7-70.

The **F CEN**, **ΔF >50 MHz**, and F **CORR** signals generated on the A5 PCB are summed together at the E/I Converter (Figure 7-68) and used to generate the YIG tuning-coil current. As shown, the three A5 voltage signals are applied to U4, via U3D. If the output frequency is <2 GHz, a heterodyne offset voltage via U3B is also summed in with the A5 voltages. This offset voltage causes the YIG to sweep between 4.61 and 6.6 GHz. When this 4.61 to 6.6 GHz sweep is beat with the output from the 4.6 GHz local osicllator in the Down Converter, a 10 MHz to 2 GHz sweep results.

The output from U4 controls the current through the YIG tuning coil, via transistor A6Q2 (located on the RF Deck). The current through the coil develops a proportional voltage drop across sense resistor (R SENSE) R15.

When the output frequency goes above 2 GHz, a bandswitch occurs. The Bandswitch/ROM Select Logic (Figure 7-68) causes the **L HET YIG SEL** line to go FALSE and open U3B. When U3B opens, the heterodyne offset voltage is removed from the U4 input. The U4 output then causes the YIG to sweep between 2 and 8 GHz.

In multi-YIG sweep generators, transistors Q1 (on A6) and A6Q3 (on the RF Deck) are used to switch the A6Q2 emitter voltage from -38V to -15V when the 2-8 GHz YIG is not selected. Since the 2-8 GHz YIG is always selected in the 6617A, Q1 and A6Q3 are always switched on, thus placing the -38V on the A6Q2 emitter. Q1 is switched on by the continually FALSE state of the **L YIG SEL** control line. Three other components that have multi-YIG uses but are inactive in the 6617A are FET switch U3A and resistors R16 and R17. In multi-YIG units, these components cause the YIG to oscillate at a rest frequency of 2 GHz when the 2-8 GHz YIG is not selected.

The remaining input to the E/I Converter is the **CW FILTER** line. When the microprocessor commands that the CW filter be inserted, relay K1 is activated. (The CW filter is inserted when the sweep width is ≤50 MHz or when a CW mode has been selected from the front panel.) When K1 is activated the R27-C16 network creates an alternative path around the YIG oscillator. This path reduces the noise current flowing through the coil, thereby quieting the YIG oscillator frequency output.

As shown in Figure 7-68, the input to the Tracking Filter Voltage Generator (U2A-U2D) is the voltage ramp developed across R SENSE (R15). This R15 voltage ramp is modified in slope (gain) and offset (if necessary) and used indirectly to tune the YIG tracking filter. The circuit output, via U3C, is supplied to the A10 PCB, where it is used to develop a tuning current for the tracking filter coil. FET switch U3C is controlled by the **L YIG SEL** line. In the 6617A, this line is always TRUE, keeping U3C active and its switch contacts closed.

The inputs to the Bandswitch/ROM Select Logic circuit (U1A, U1B, U1C, U10B, U10C) are the **FCEN/VPF** and **F CEN** voltage signals from the A5 PCB.

Para. 7-12.5 (cont'd.)

The **FCEN/VPF** voltage is used for bandswitching. It is compared at U9B with a voltage representing 2 GHz. When it equals or exceeds the 2 GHz voltage, the **L HET YIG SEL, L HET PIN SEL,** and **L HET OFFSET** lines go FALSE, thus causing the output to switch from the heterodyne to the YIG band. The **FCEN/VPF** voltage is also compared at U9A with a voltage representing 8 GHz. Since no bandswitch is needed at 8 GHz, the **FCEN/VPF** voltage never exceeds the comparison voltage. Consequently, the **L PIN SELECT** lines remain TRUE and the H **SNB** (select next band) line remains FALSE.

The F **CEN** voltage is used for Linearizer ROM selection. It is compared with the 8 GHz voltage at U9C. Since no bandswitch is needed, the **F CEN** voltage never exceeds the comparison voltage. Consequently, the L **ROM** SEL line remains TRUE and the **H SNR** line remains FALSE.

In addition to the **FCEN/VPF** and **F CEN** analog voltage inputs, there are two logic control inputs to the Bandswitch/ROM Select Logic. These logic control inputs are **L RF OFF** and **L PIN SW OFF.** The **L RF OFF** input is from the microprocessor, via a latch on the A4 PCB. The L **PIN SW OFF** input is from the Sq Wave Sample/Hold Logic circuit on the A4 PCB (paragraph 7-11.1g). When either of these two logic inputs goes TRUE, both the L **HET PIN SELECT** and L **PIN SELECT** lines go FALSE.

When the L **HET PIN SELECT** line is FALSE it reverse-biases A14CR17 (Figure 7-70, Sheet 3). Reverse-biasing CR17 causes A14Q5 to turn on, A14Q8 to turn on, and A14Q9 to turn off. When on, Q8 sources current into the T1 port of the switch. When the **L HET PIN SELECT** line is TRUE (.01-2 GHz Het Band is selected), CR17 is forward-biased. Forward-biasing CR17 causes Q5 to turn off, Q8 to turn off, and Q9 to turn on. When on, Q9 sinks current from the T1 port on the DPDT (PIN) switch.

When the **L PIN SELECT** line changes states, the circuit composed of A14CR18, A14Q6, A14Q10, and A14Q11 sources current into and sinks current from the DPDT (PIN) Switch's T2 port – in the same manner described for the **L HET PIN SEL** circuit above.

Sinking current from the T1 port while at the same time sourcing it into the T2 port causes (1) the YIG output to be switched into the Heterodyne Down Converter and (2) the down converter output to be switched into the RF output circuit. Conversely, sinking current from the T2 port while sourcing it into the T1 port causes the YIG output to be switched into the RF output circuit and the down converter output to be grounded.

The inputs to the Linearizing ROM (U5) are the **ROM Bus** lines from the microprocessor, via the A14U6 latch on the motherboard. The Linearizing ROM is enabled by the TRUE state of the **L ROM SEL** line from the Bandswitch Logic circuit. It outputs eight bits of data to the A5 PCB.

The input to the PIN Driver (ALC) circuit (U7A, U8B, Q6, Q7) is from the A4 PCB. This circuit has two functions: (1) It provides the ALC-loop-gain adjustment, and (2) it makes linear the relationship between the A4 PCB Level Amp output in Vdc (paragraph 7-11.1) and the RF power output in dBm. Control for the PIN Driver circuit is provided by the **H YIG SEL** line from the E/I Converter circuit. This line is always TRUE. The output from this circuit is a current: **MOD DRIVER.** This current is supplied to the MOD (Modulator) component on the RF Deck, via A14R34 (Figure 7-70, Sheet 3).

The input to the -5V Bias Supply (U7B, U8A, Q3, Q4, Q5) is the control line **L RF OFF.** When the front panel RF ON switch is disengaged (out), the microprocessor sets this line TRUE. When **L RF OFF** is TRUE, the -5V Bias Supply is turned off, thus turning off the Band 1 YIG oscillator.

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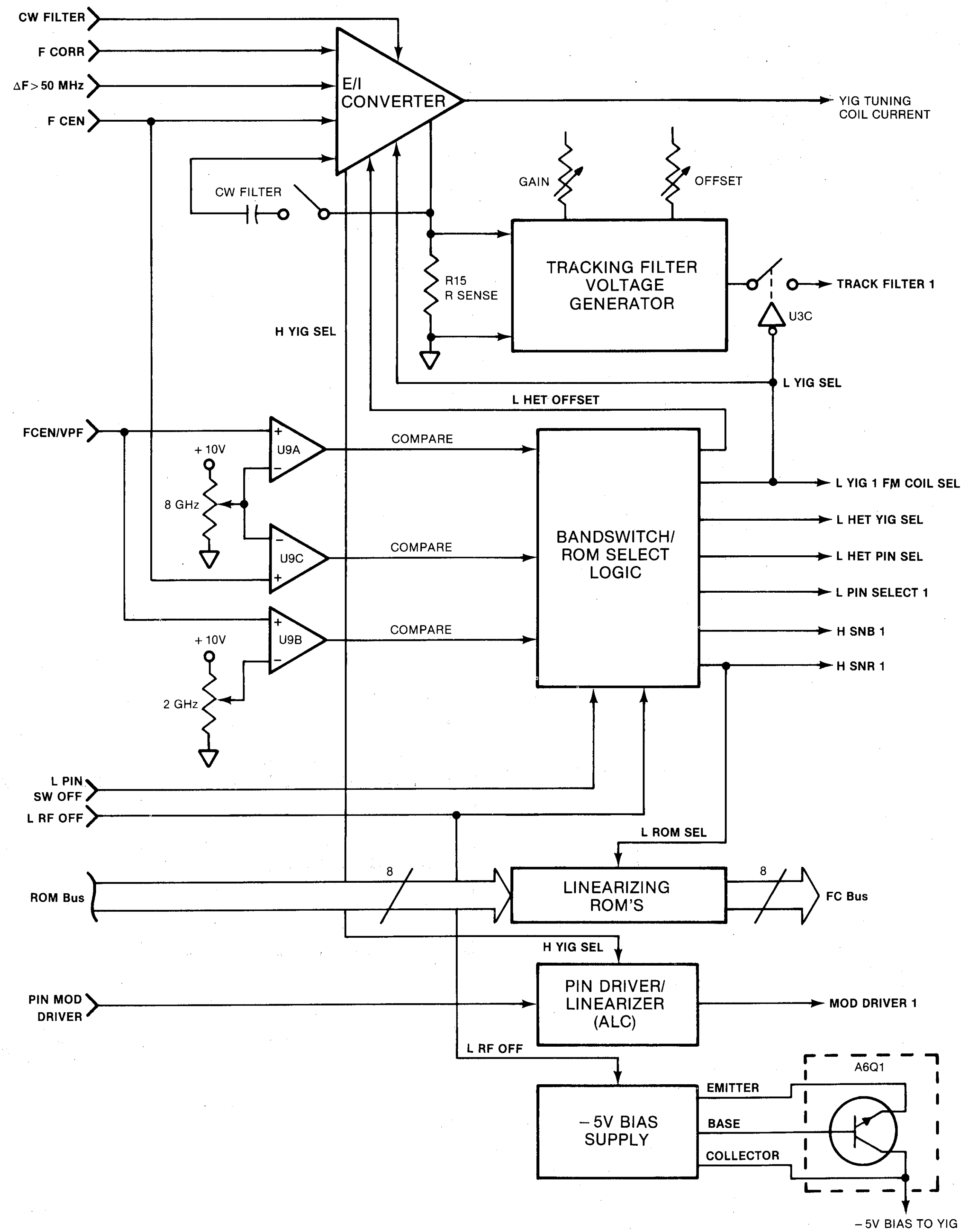


Figure 7-68. Assy 8007-6 Het/YIG Driver PCB Overall Block Diagram

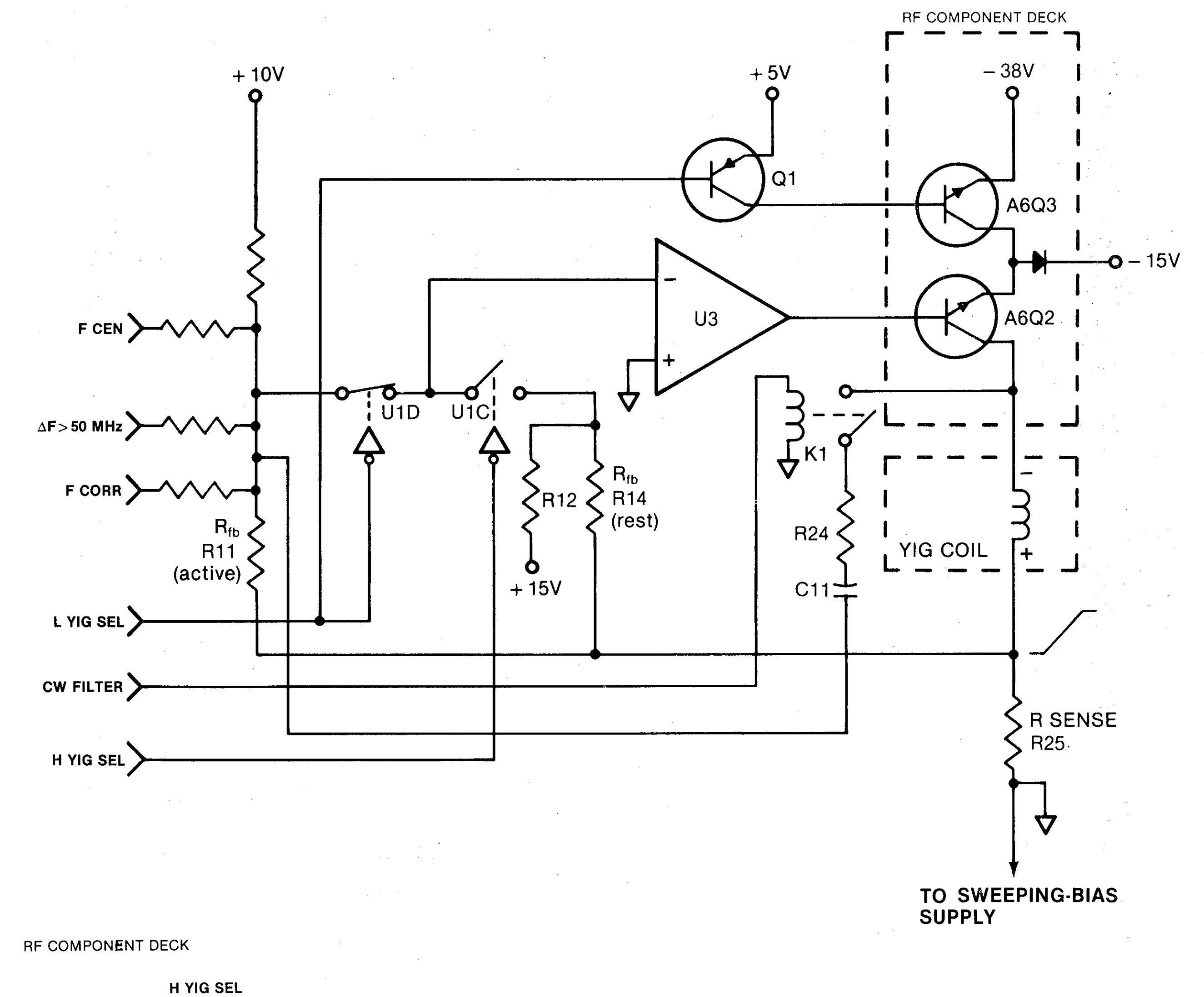
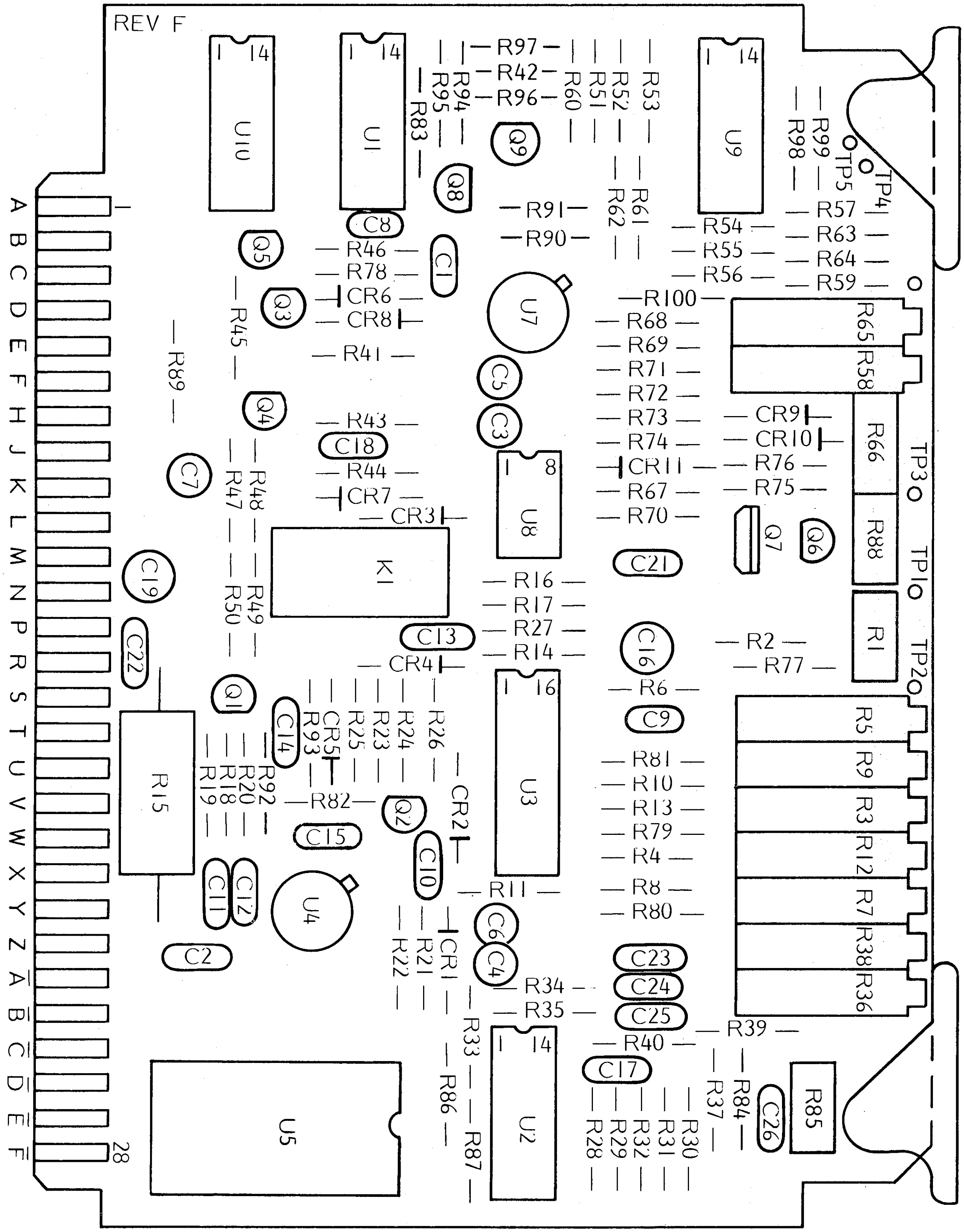


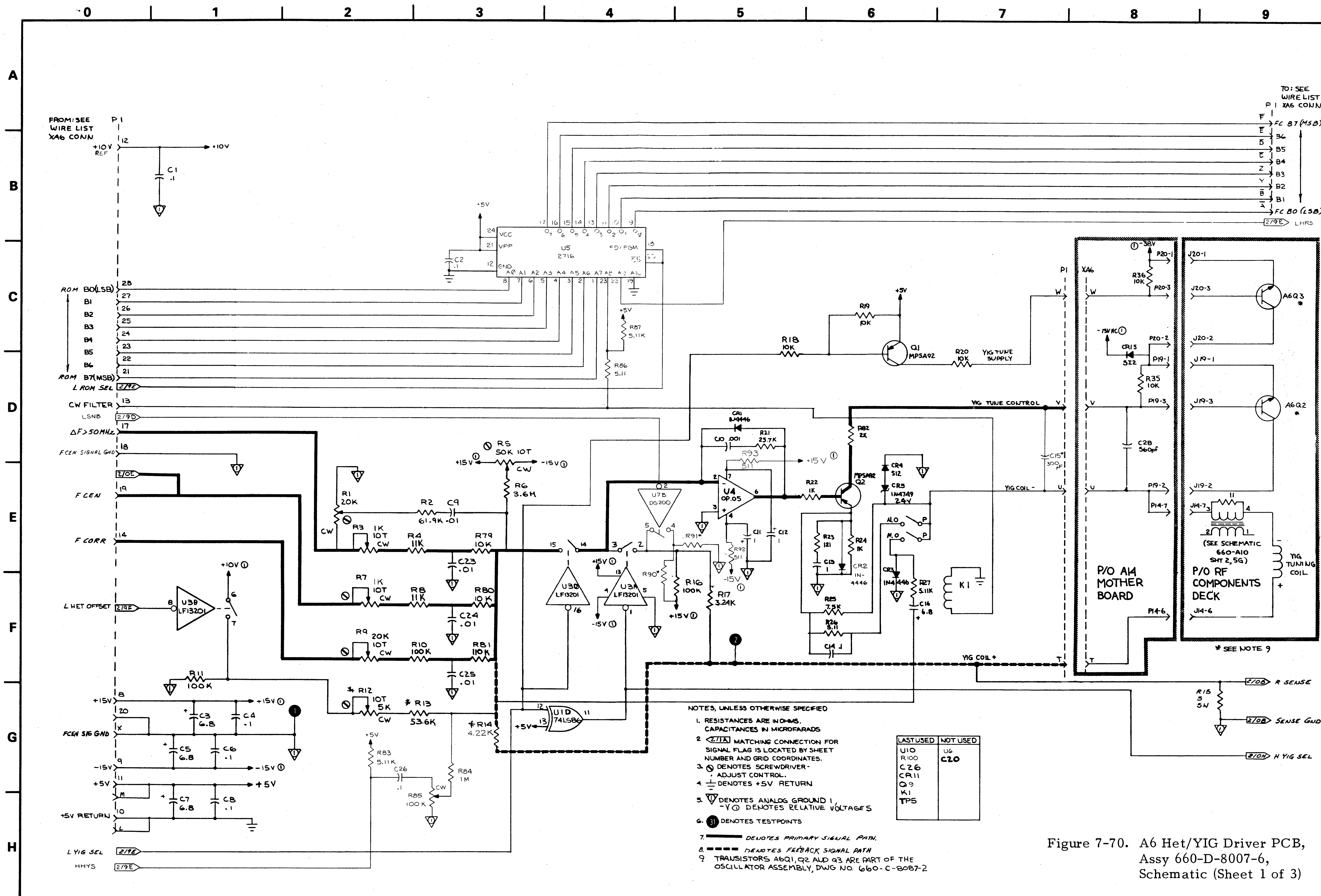
Figure 7-69. Assy 8007-6 Het/YIG Driver PCB E/I Converter Simplified Schematic

Figure 7-68



A6 PCB Parts Locator Diagram

Diagram



NOTES, UNLESS OTHERWISE SPECIFIED

1. RESISTANCES ARE IN OHMS, CAPACITANCES IN MICROFARADS
2. 2/1A MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
3. ⦸ DENOTES SCREWDRIVER-ADJUST CONTROL.
4. ⏚ DENOTES +5V RETURN
5. ▽ DENOTES ANALOG GROUND 1, -V① DENOTES RELATIVE VOLTAGES
6. ❶ DENOTES TESTPOINTS
7. ▬▬ DENOTES PRIMARY SIGNAL PATH.
8. ▬ ▬ DENOTES FEEDBACK SIGNAL PATH
9. TRANSISTORS A6Q1, Q2 AND Q3 ARE PART OF THE OSCILLATOR ASSEMBLY, DWG NO. 660-C-8087-2

LAST USED	NOT USED
U10	U6
R100	C20
C26	
CR11	
Q3	
K1	
TP5	

Figure 7-70. A6 Het/YIG Driver PCB, Assy 660-D-8007-6, Schematic (Sheet 1 of 3)

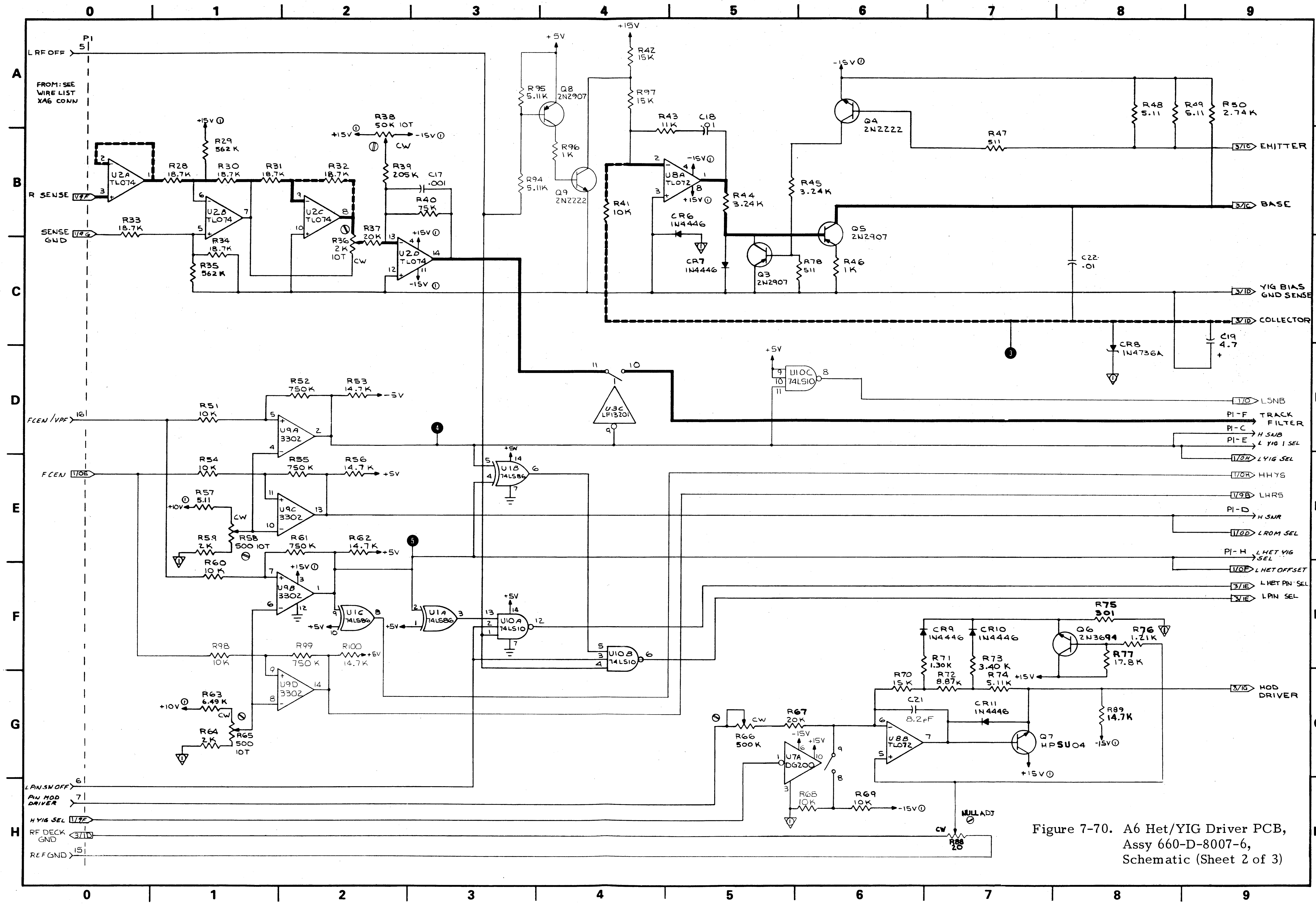


Figure 7-70. A6 Het/YIG Driver PCB, Assy 660-D-8007-6, Schematic (Sheet 2 of 3)

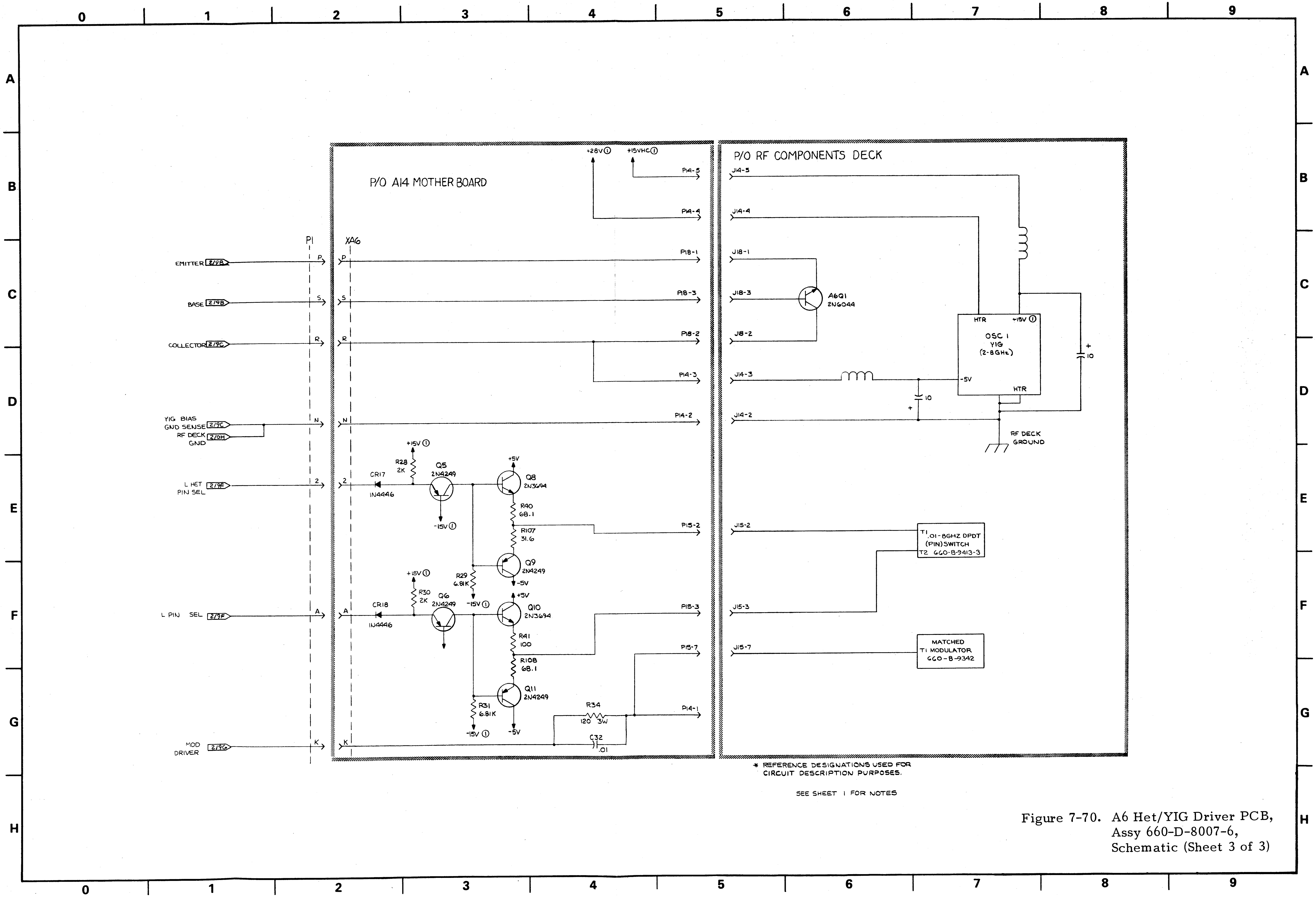
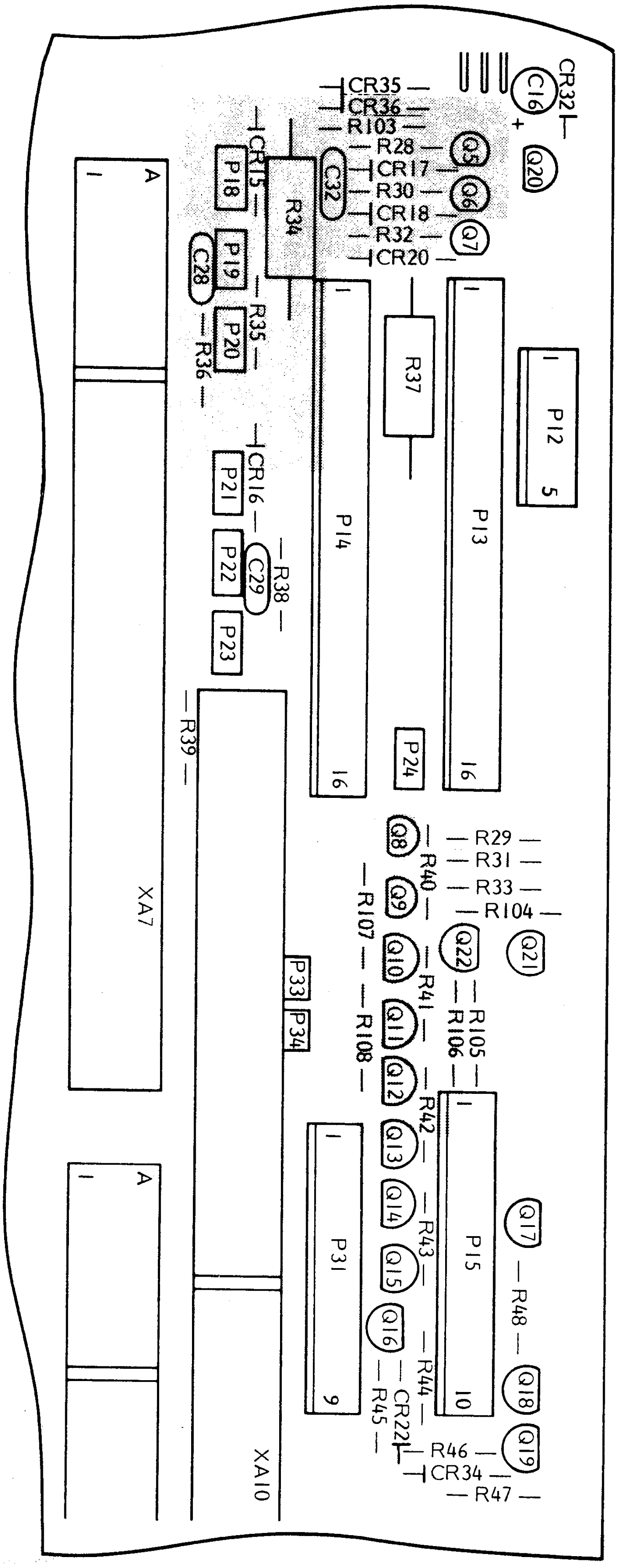
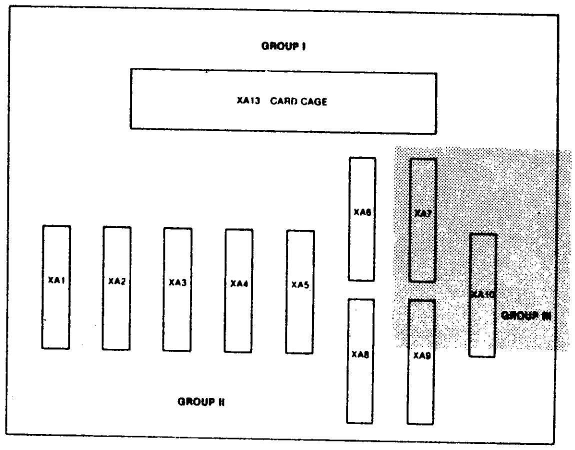


Figure 7-70. A6 Het/YIG Driver PCB, Assy 660-D-8007-6, Schematic (Sheet 3 of 3)





Osc 1 YIG, PIN Driver, and PIN/Modulator Parts Locator Diagram

7-12.6 Assy 660-D-8190 and 8191 YIG Driver PCB, Circuit Description

The 8190 and 8191 YIG Driver PCBs are identical, except for the polarity of their sweeping-bias supply outputs: The 8190 provides a positive-bias output, and the 8191 provides a negative-bias output. Both assemblies generate the following currents and voltages:

- Tuning current for the YIG.
- Sweeping-bias current for the YIG.
- Modulating current for the PIN Modulator attenuator.
- Linearizer ROM output data.
- Bandswitch logic voltages.

A block diagram of the YIG Driver PCB, which is drawn to accommodate both the 8190 and 8191, is shown in Figure 7-71. A simplified schematic for the PCB's E/I Converter is shown in Figure 7-72. The schematic for the 8190 PCB is shown in Figure 7-73. And the schematic for the 8191 A6 PCB is shown in Figure 7-74.

The F **CEN**, **ΔF >50 MHz**, and F **CORR** signals generated on the A5 PCB are summed together at the E/I Converter (Figure 7-72) and used to generate the YIG tuning-coil current. As shown, the three A5 voltage signals are applied to U3, via U1D. At present, the switch contacts of U1D are always making in these models. The output from U3 controls the current through the YIG tuning coil, via transistor A6Q2. The current through the coil develops a proportional voltage drop across sense resistor (R SENSE) R25.

In multi-YIG sweep generators, transistors Q1 (on A6) and A6 or A7Q3 (on the RF Deck) are used to switch the A6 or A7Q2 emitter voltage from -38V to -15V when that YIG is not selected to supply the output frequency. Since the 8190 and 8191 have only one YIG, it is always selected; consequently, -38V is always supplied to the A6 or A7Q2 emitter from a saturated A6 or A7Q3. The bias voltage that causes A6 or A7Q3 to become saturated is via Q1, which is switched on via the continually FALSE state of L **YIG SEL.**

Three other components that have multi-YIG uses but are inactive in the 8190 and 8191 are FET switch U1C and resistors R12 and R14. In multi-YIG units, these components cause the YIG to oscillate at a rest frequency when it is not selected.

The input to the Sweeping-Bias Supply (U7A-U7D, Q5-Q8, U1B) (Figure 7-71) is from the R Sense resistor (R25). The operation of this bias supply is similar for both the 8190 and 8191 assemblies. The only operational difference is in the polarity of the bias-voltage signal as it goes through the various voltage generation stages. The other circuit differences between the two assemblies are in the values and types of some of the components used: Several resistors have different values and all of the transistors are opposite in type (NPN on one assembly and PNP on the other).

NOTE

> Some YIG oscillator types do not require a sweeping bias. When one of these oscillator-types is installed, the output from the sweeping-bias supply will be a fixed voltage.

The inputs to U2C, the optional PIN-switch control-gate, are the L **RF OFF** and L **PIN SW OFF** lines from the A4 PCB and the **H YIG SEL** line from the Bandswitch Logic. When all three of these inputs are HIGH, the L **PIN SEL** line is TRUE. The RF **OFF** line is HIGH when the front panel RF ON switch is depressed (On). The **PIN SW OFF** line is HIGH during the forward sweep and goes LOW at the start of the sweep retrace (provided RETRACE RF is not On). The **YIG SEL** line is for the A6 PCB when the Osc 1 YIG is supplying the output frequency, and for the A7 PCB when the Osc 2 YIG is supplying the output frequency.

For A6 when the L **PIN SEL** line is TRUE, CR17 is forward-biased (Figure 7-73 or 7-74, Sheet 3). Such biasing causes Q6 to turn off, Q10 to turn off, and Q11 to turn on. When on, Q11 sinks current from the optional PIN switch. When **L PIN SEL** is FALSE, CR18 is reverse-biased, thus causing Q6 to be turned on, Q10 to be turned on, and Q11 to be turned

Para. 7-12.6 (cont'd.)

off. When off, Q11 sources current into the PIN switch. Sourcing current into the PIN switch turns the switch off, whereas sinking current from the switch turns it on. This on/off action provides for square-wave modulation.

For the A7 PCB, when L **PIN SEL** is TRUE, CR20 is forward-biased (Figure 7-73, Sheet 3). Such biasing causes Q7 to turn on. When on, Q12 sinks current from the optional PIN switch. When L **PIN SEL** is FALSE, CR20 is reverse-biased, thus causing Q7 to be turned on, Q12 to be turned off, and Q13 to be turned off. When off, Q13 sources current into the PIN switch. Sourcing current into the PIN switch turns the switch off, whereas sinking current from the switch turns it on. This on/off action provides for square-wave modulation.

The input to the PIN Driver/Linearizer (ALC) circuit (U4A, U4B, U1A, Q3, and Q4) is from the A4 PCB. This circuit has two functions: (1) It provides the ALC-loop-gain adjustment, and (2) it makes linear the relationship between the A4 PCB Level Amp output in Vdc (paragraph 7-11.1) and the RF power output in dBm. Control for the PIN Driver/Linearizer circuit is provided by the **H YIG SEL** line, which is always TRUE in these models. The output from this circuit is a current, **MOD DRIVER**. This current is supplied to the MOD (Modulator) component on the RF Deck, via A14R34 (Figure 7-73 or 7-74, Sheet 3) for the A6 YIG or via A14R37 for the A7 YIG.

The inputs to the Bandswitch/ROM Select (U8A-U8D) are as follows:

- The **FCEN/VPF** and F **CEN** voltage signals from the A5 PCB.
- The H **SNB** and **H SNR** logic control lines from the A6 PCB.

The **FCEN/VPF** and F **CEN** voltages are compared with a voltage representing 26.5 GHz. When the **FCEN/VPF** voltage equals or exceeds the comparison voltage, and if the **H SNB** line is TRUE, the following occur:

- The **L YIG SEL** and **H YIG SEL** lines go FALSE.
- The **H SNB** line goes TRUE.

When the **F CEN** voltage equals or exceeds the comparison voltage and if the **H SNR** line is TRUE, the following occur:

- The **H SNR** line goes TRUE.
- The **L ROM SEL** line goes FALSE.

The inputs to the Linearizing ROM (U5) are the **ROM Bus** lines from the microprocessor, via the A14U6 latch on the motherboard. The Linearizing ROM is enabled by the TRUE state of the **L ROM SEL** line from the Bandswitch Logic circuit. It outputs eight bits of data to the A5 PCB.

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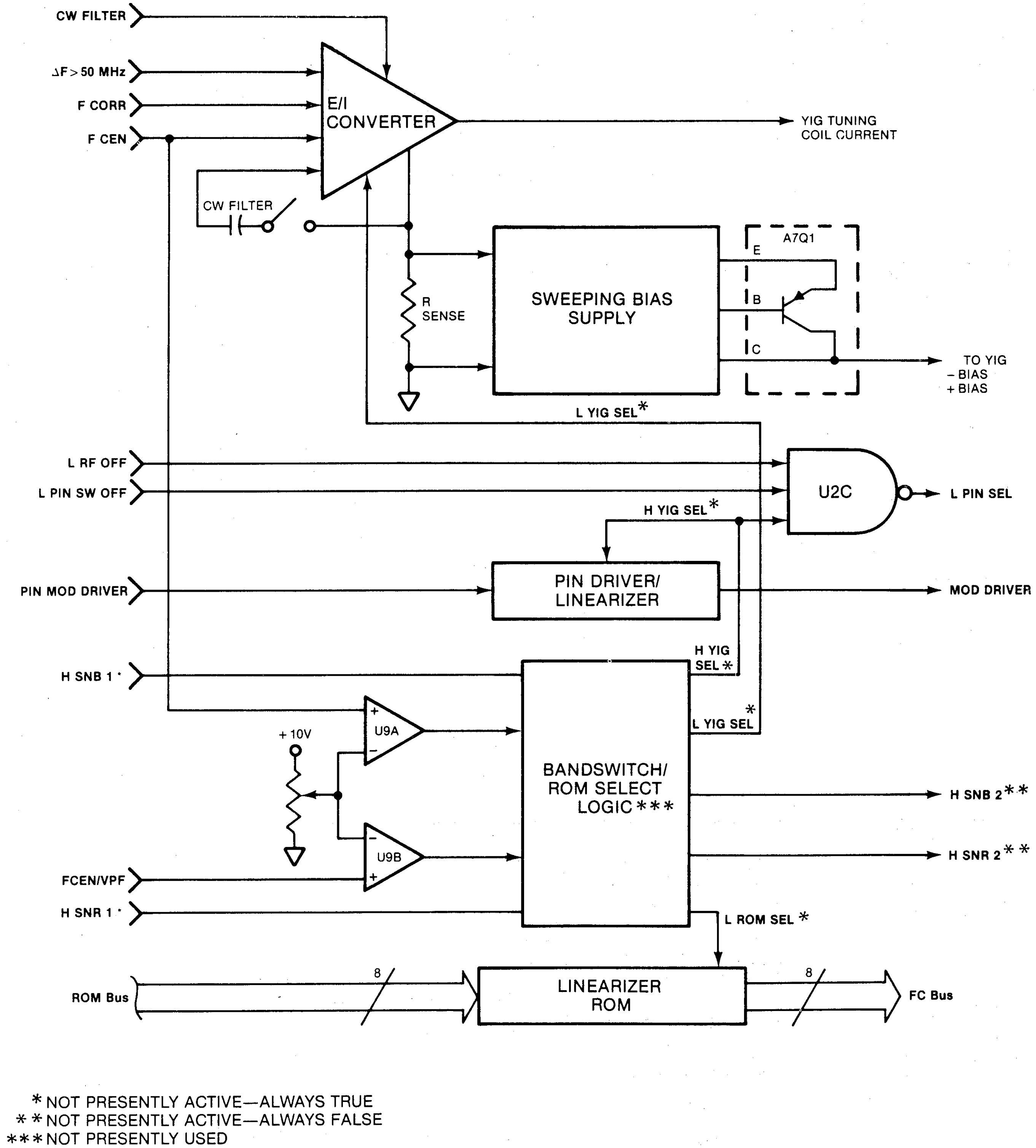


Figure 7-71. 8190/8191 YIG Driver PCB Block Diagram

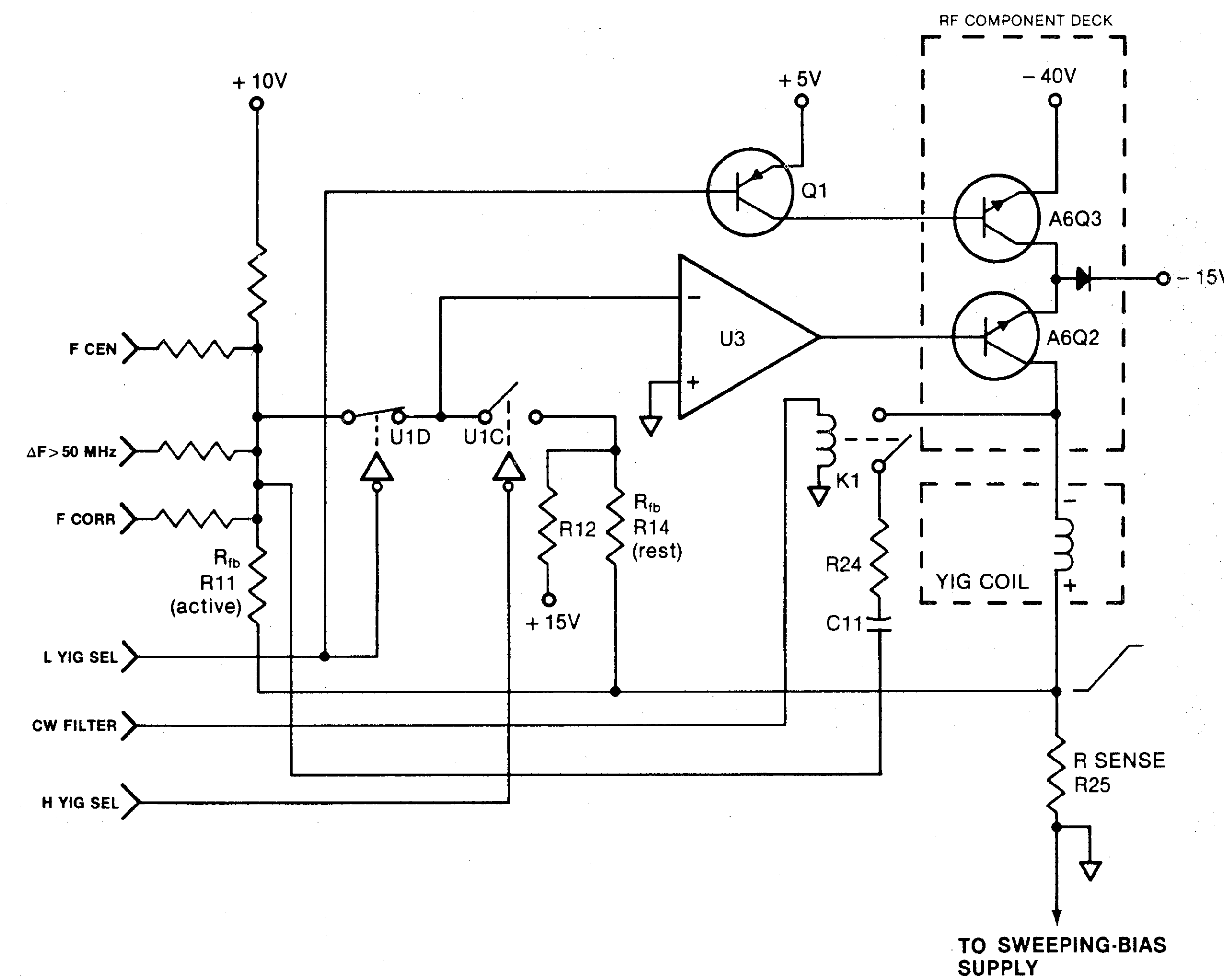


Figure 7-72. 8190/8191 YIG Driver PCB E/I Converter Circuit Simplified Schematic

Figure 7-71

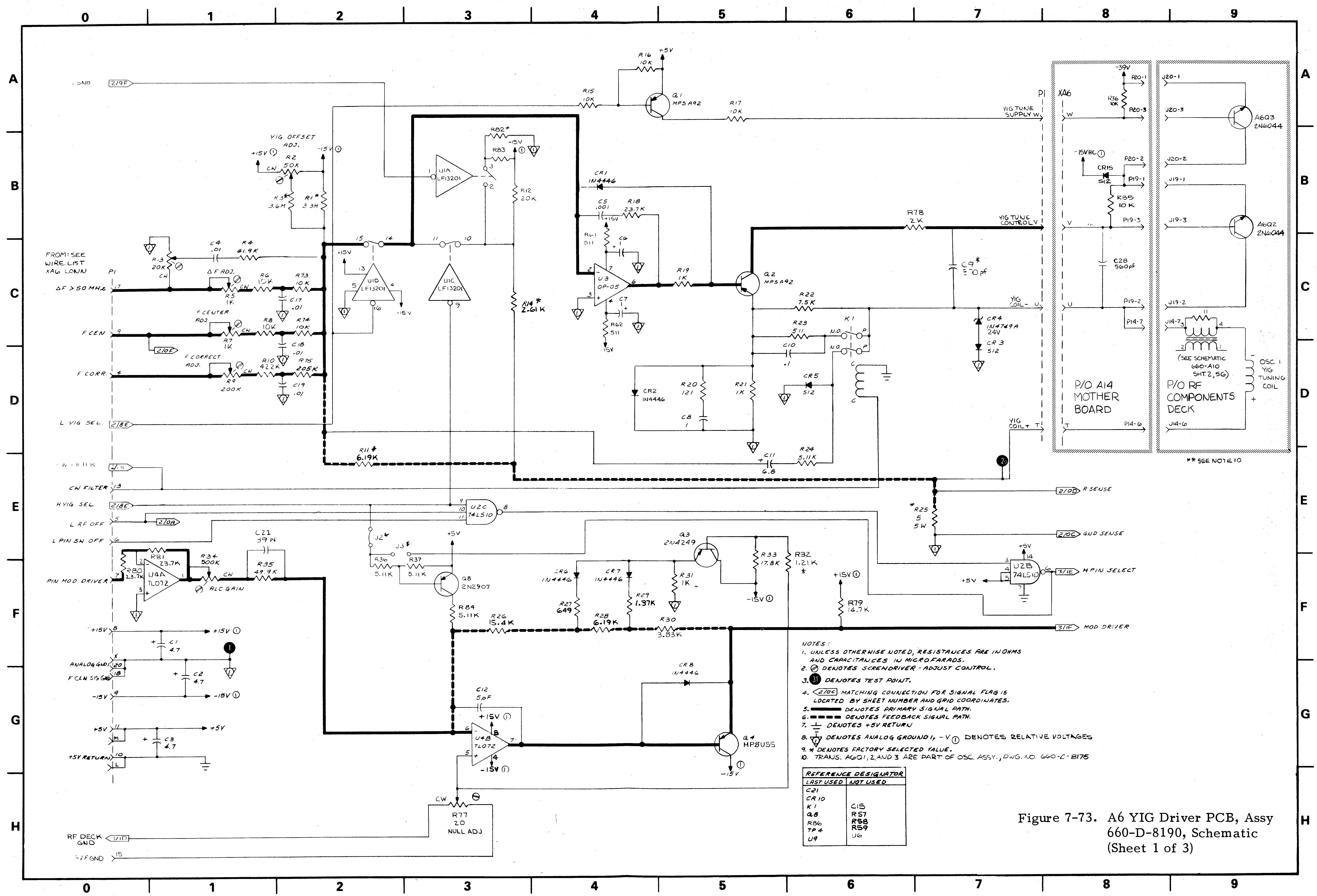
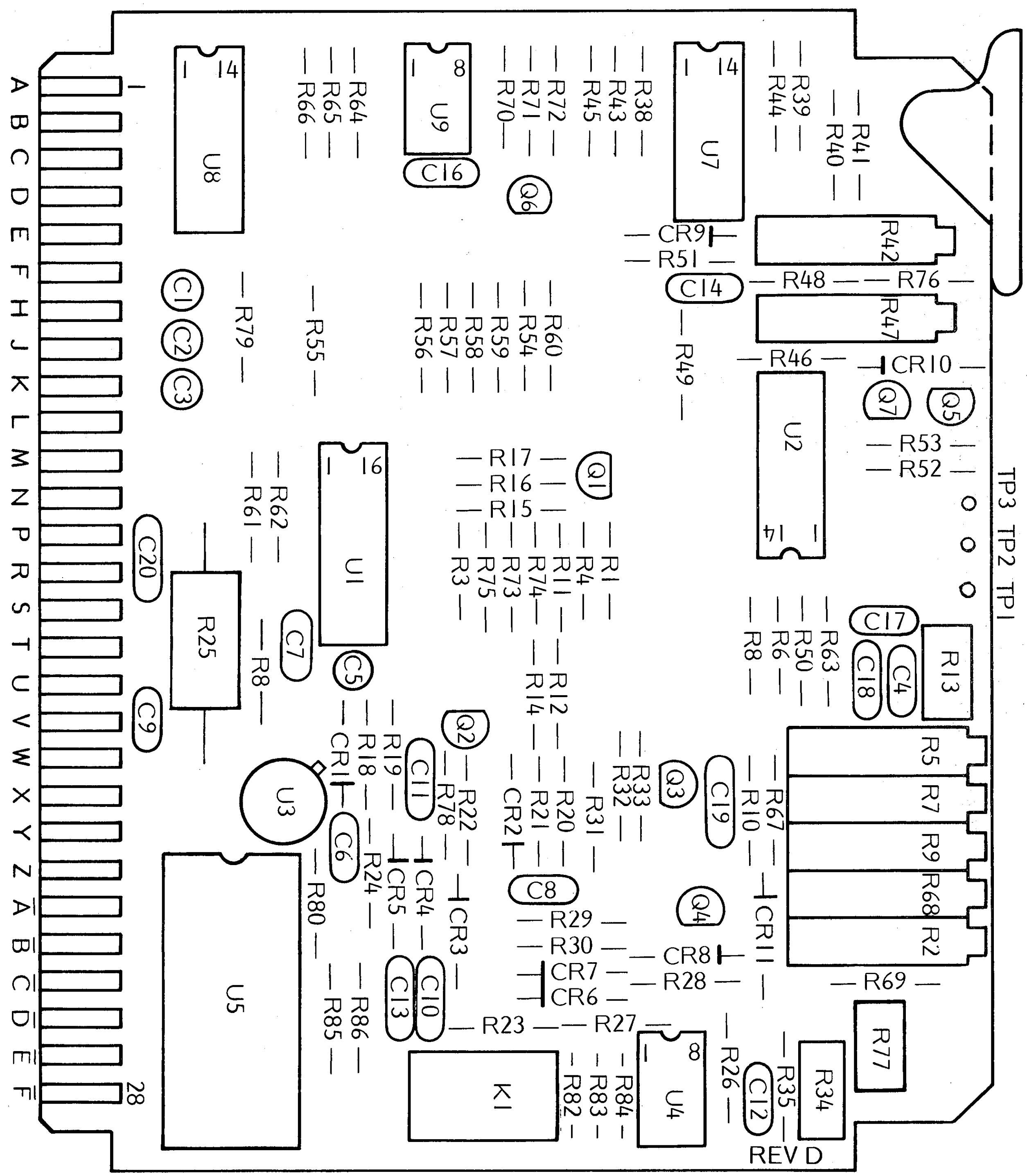


Figure 7-73. A6 YIG Driver PCB, Assy 660-D-8190, Schematic (Sheet 1 of 3)

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. ⊘ DENOTES SCREWDRIVER-ADJUST CONTROL.
3. (31) DENOTES TEST POINT.
4. 2/10C MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ▬▬ DENOTES PRIMARY SIGNAL PATH.
6. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.
7. ⏚ DENOTES +5V RETURN
8. ▽(1) DENOTES ANALOG GROUND 1, −V(1) DENOTES RELATIVE VOLTAGES
9. * DENOTES FACTORY SELECTED VALUE.
10. TRANS. A6Q1, 2, AND 3 ARE PART OF OSC. ASSY., DWG. NO. 660-C-8175

REFERENCE DESIGNATOR	
LAST USED	NOT USED
C21	
CR10	
K1	C15
Q8	R57
R86	R58
TP4	R59
U9	U6



A6 PCB Parts Locator Diagram

Figure 7-73
(Sheet 1 of 3)

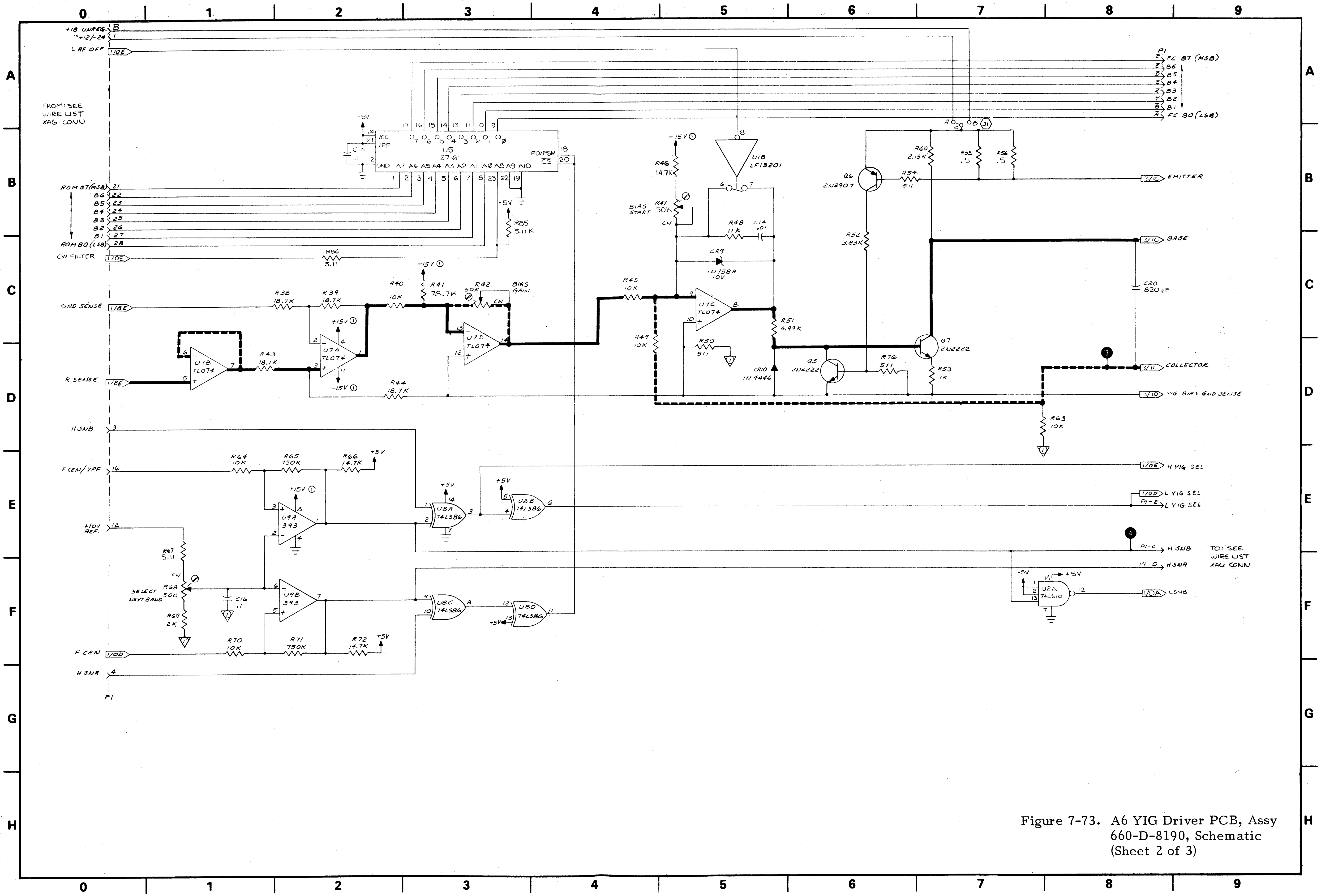


Figure 7-73. A6 YIG Driver PCB, Assy 660-D-8190, Schematic (Sheet 2 of 3)

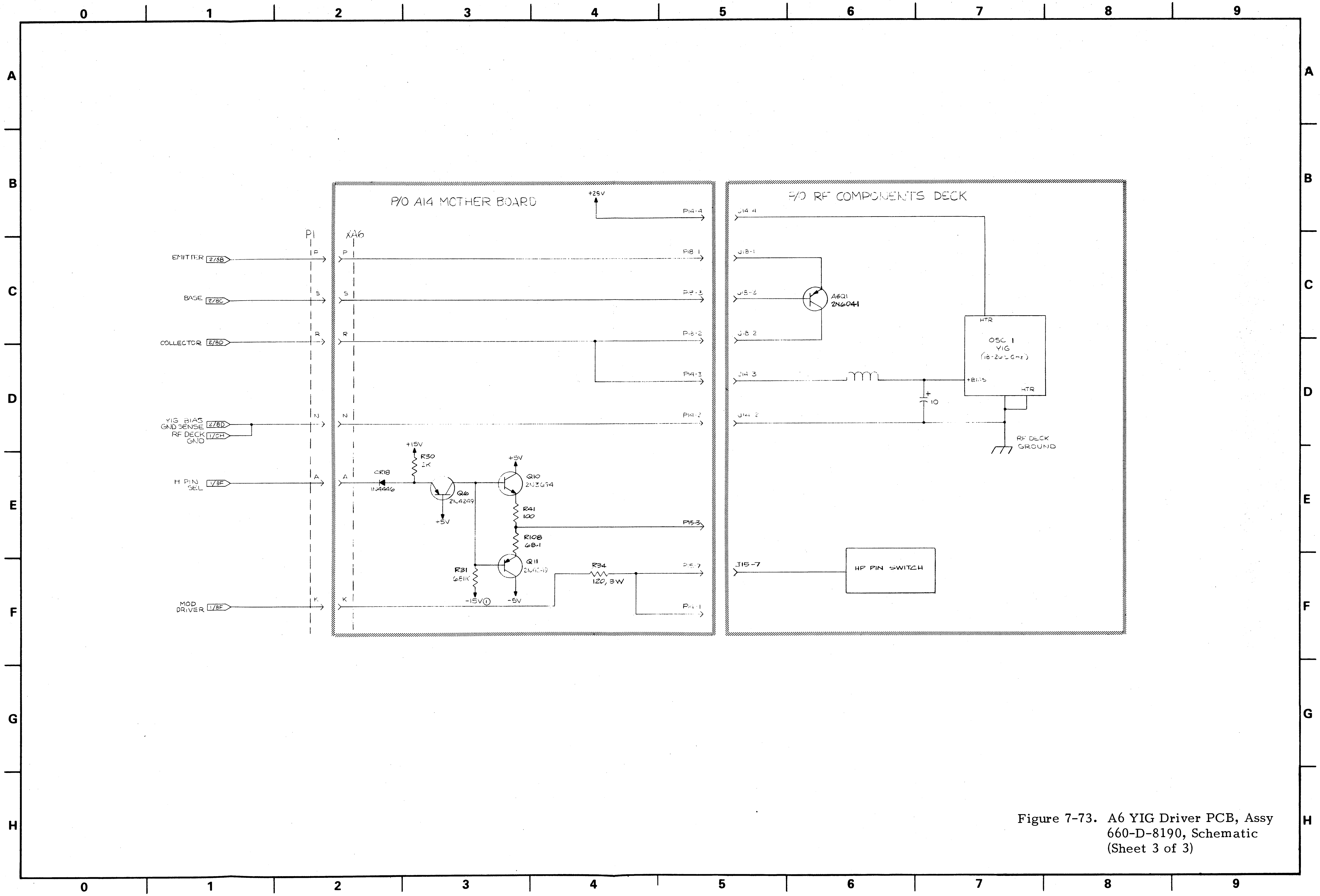
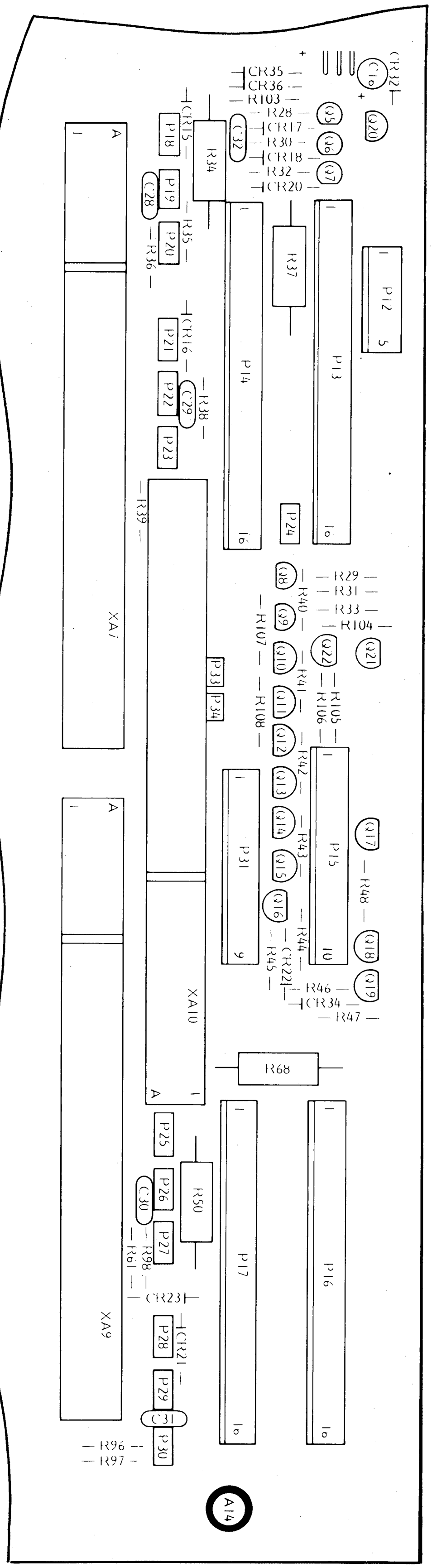
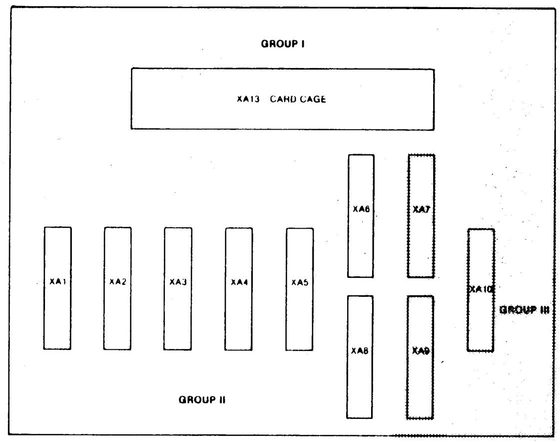
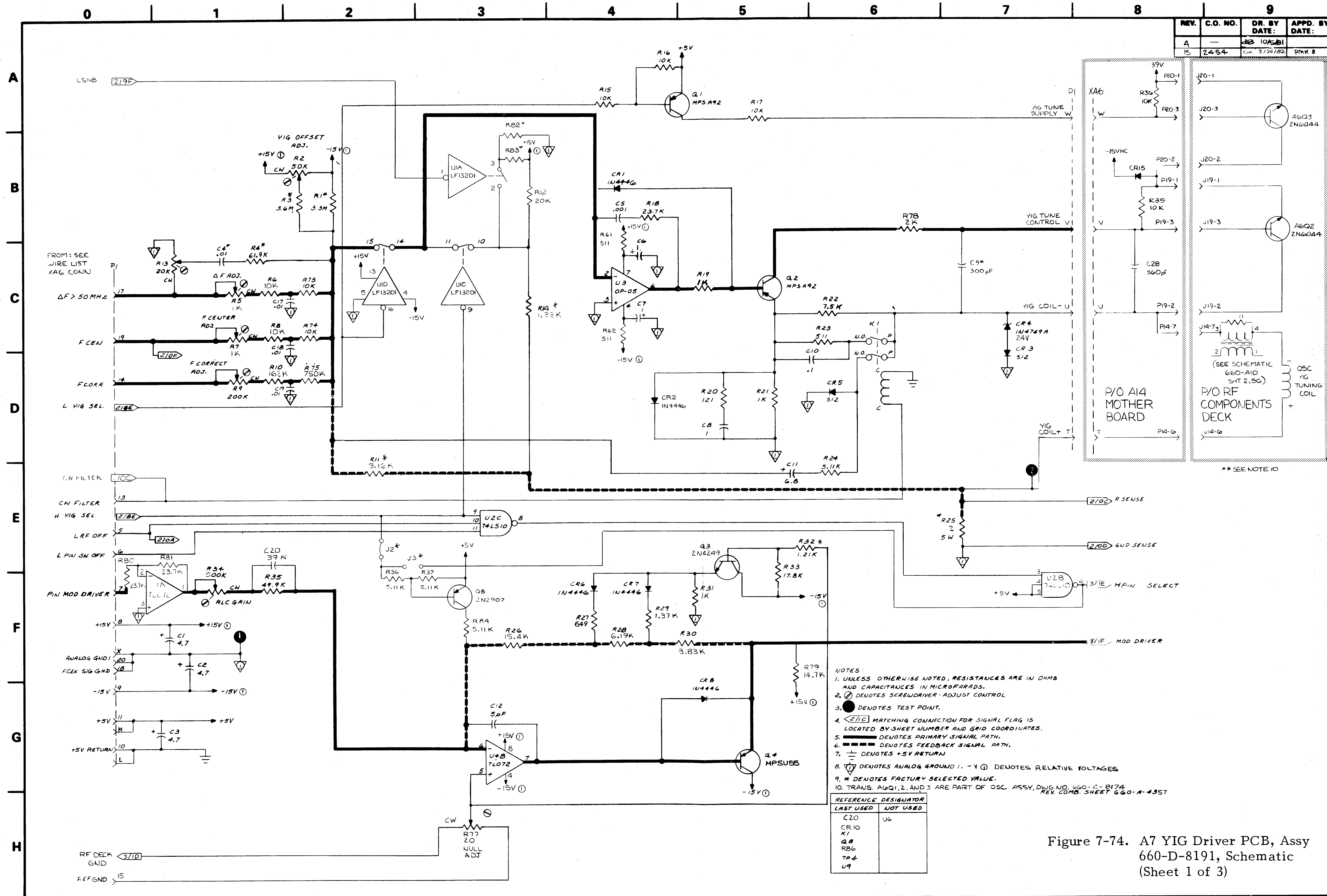


Figure 7-73. A6 YIG Driver PCB, Assy 660-D-8190, Schematic (Sheet 3 of 3)





Osc 2 and Osc 3 YIG, PIN Driver, and PIN Modulator Parts Locator Diagram



REV.	C.O. NO.	DR. BY DATE:	APPD. BY: DATE:
A	—	HB 10/5/81	
B	2454	3/26/82	

NOTES:
1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. ⊘ DENOTES SCREWDRIVER-ADJUST CONTROL
3. ● DENOTES TEST POINT.
4. 2/1C MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ▬▬ DENOTES PRIMARY SIGNAL PATH.
6. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.
7. DENOTES +5V RETURN
8. DENOTES ANALOG GROUND 1. −V ① DENOTES RELATIVE VOLTAGES
9. * DENOTES FACTORY SELECTED VALUE.
10. TRANS. A6Q1, 2, AND 3 ARE PART OF OSC. ASSY, DWG NO. 660-C-8174.

REV. COMB. SHEET 660-A-4357

REFERENCE DESIGNATOR	
LAST USED	NOT USED
C20	U6
CR10	
K1	
Q8	
R86	
TP4	
U9	

Figure 7-74. A7 YIG Driver PCB, Assy 660-D-8191, Schematic (Sheet 1 of 3)

parts locator

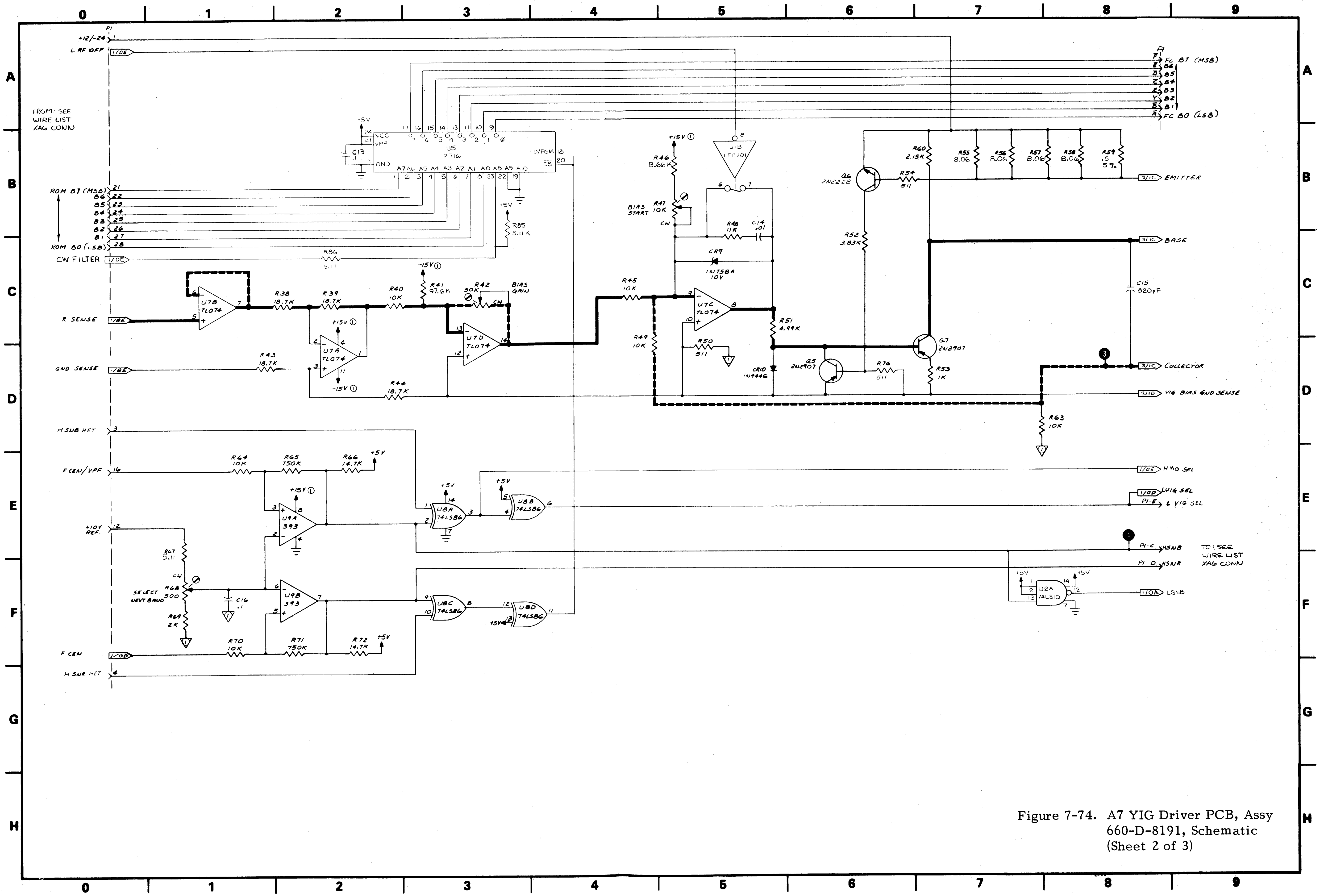
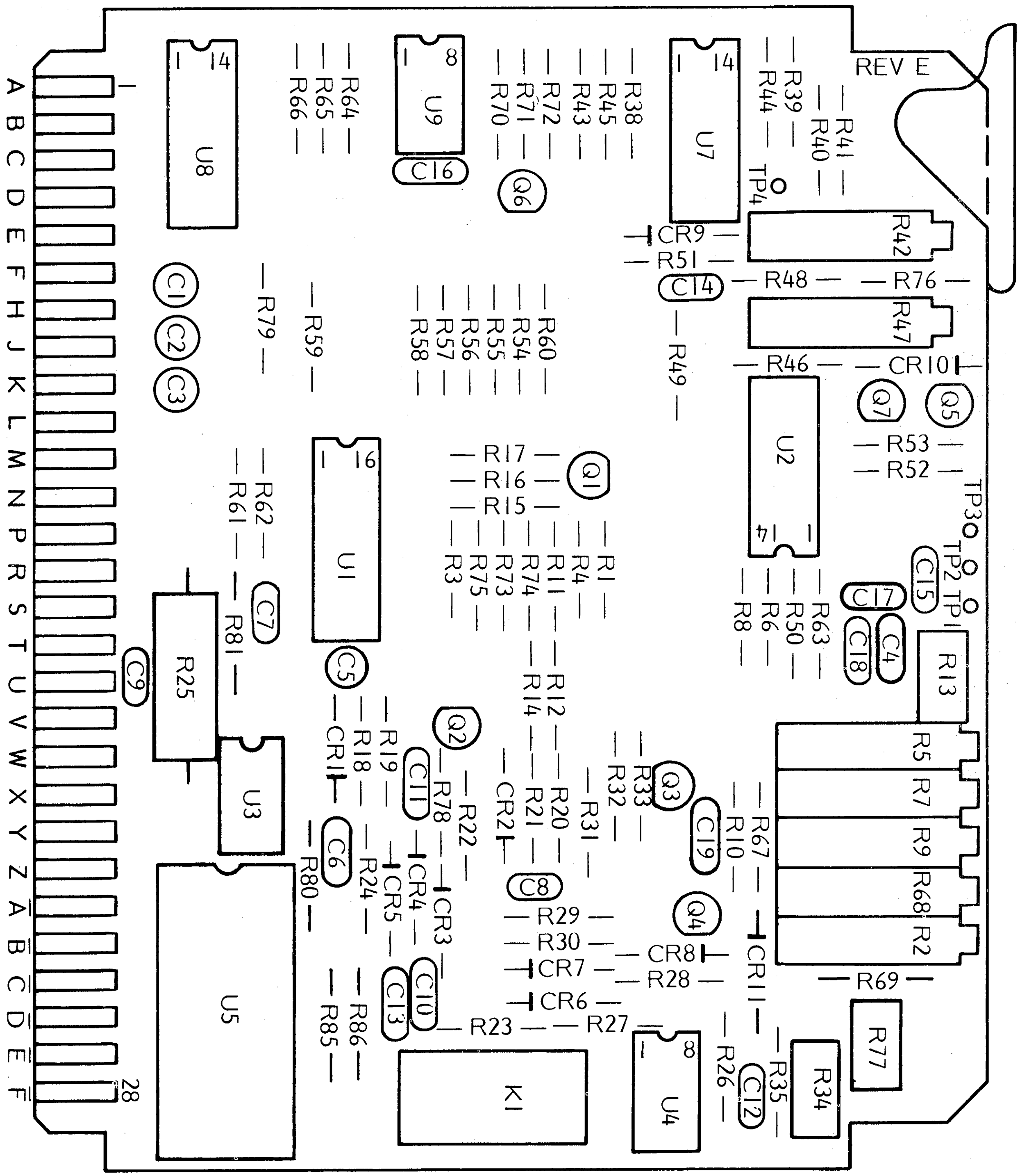


Figure 7-74. A7 YIG Driver PCB, Assy 660-D-8191, Schematic (Sheet 2 of 3)



A7/A8 PCB Parts Locator Diagram

Figure 7-74
(Sheet 2 of 3)

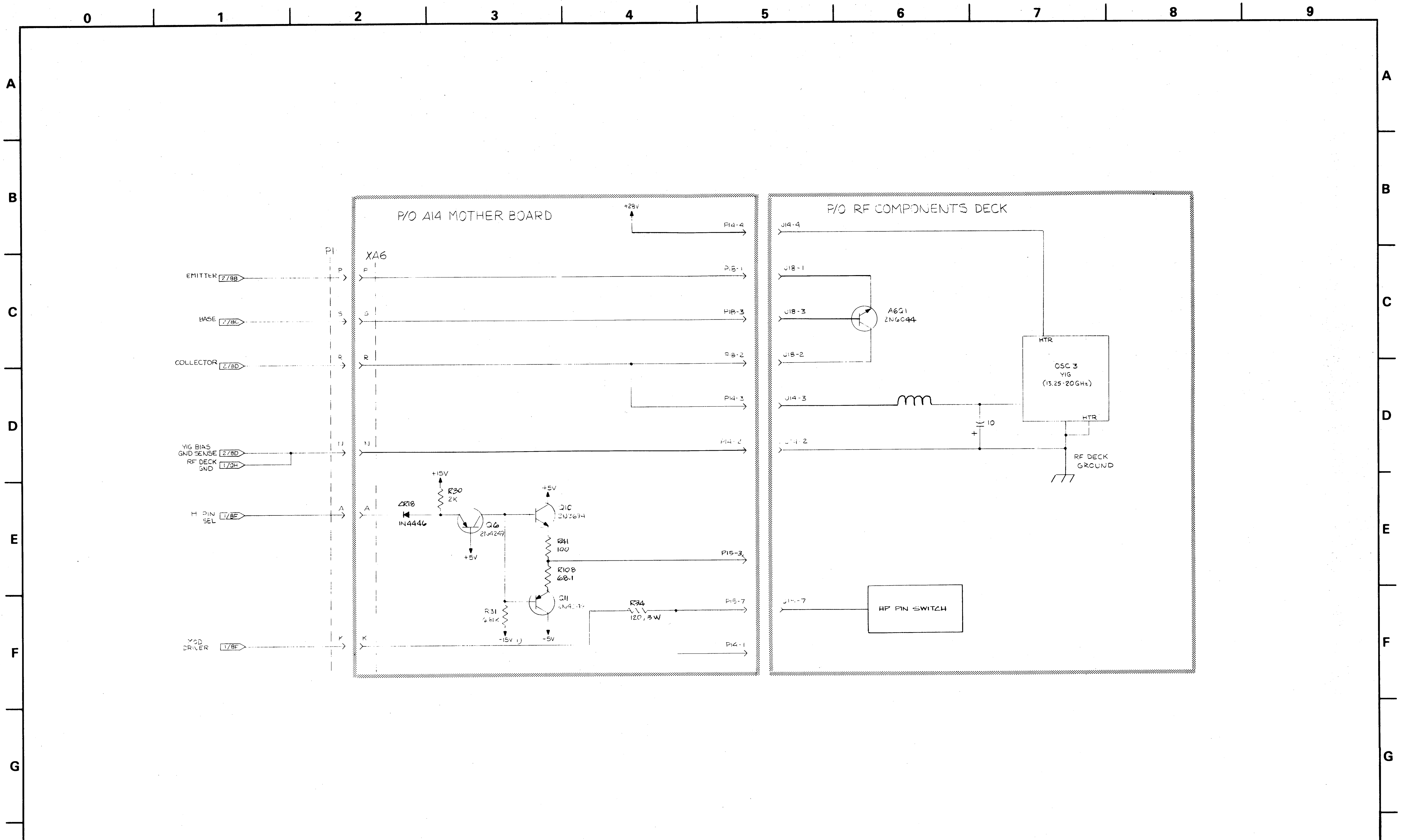
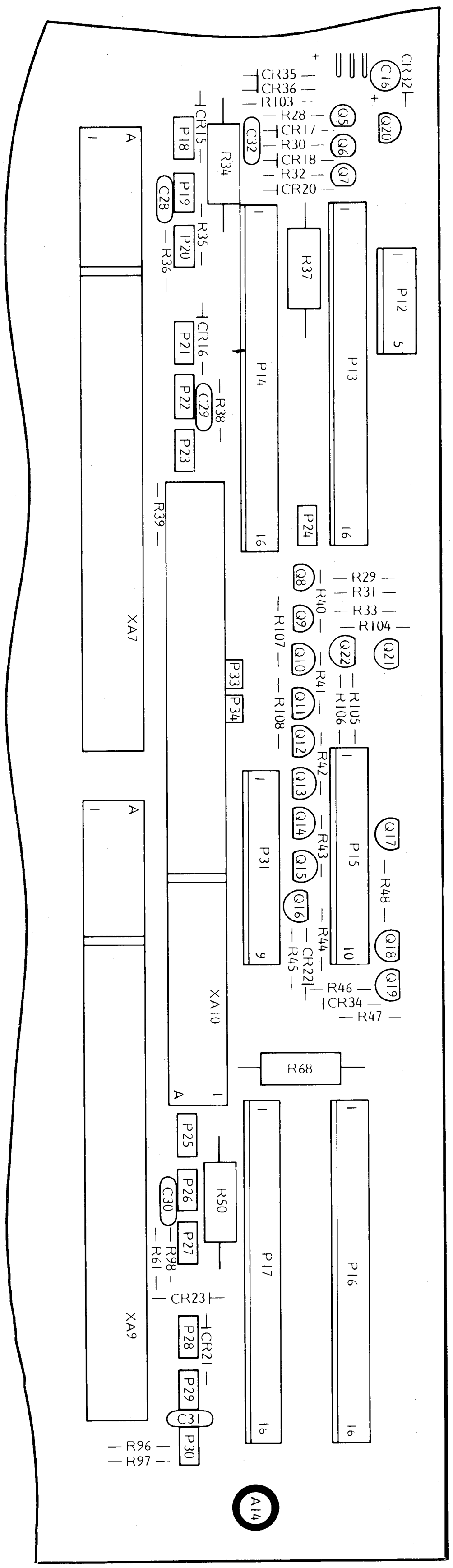
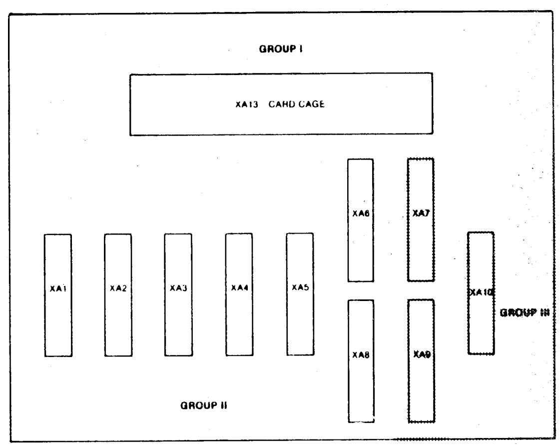


Figure 7-74. A7 YIG Driver PCB, Assy 660-D-8191, Schematic (Sheet 3 of 3)





Osc 2 and Osc 3 YIG, PIN Driver, and PIN Modulator Parts Locator Diagram

7-12.7 Assy 660-D-8008 and -8009 PCBs (All Dash Numbers), Circuit Description

The 660-D-8008 and -8009 YIG Driver PCBs are identical except for the polarity of their sweeping-bias supply outputs: The 8008 provides a negative-bias output, and the 8009 provides a positive-bias output. Both assemblies generate the following currents and voltages:

- Tuning current for the Osc 2, Osc 3, and Osc 4 YIGs.
- Sweeping-bias current for the Osc 2, Osc 3, and Osc 4 YIGs.
- Modulating Current for the Osc 2, Osc 3, and Osc 4 PIN Switch attenuators.
- Linearizer ROM output data.
- Bandswitch logic voltages.

A block diagram for the 8008 and 8009 assemblies is shown in Figure 7-75. The 8008-4, -7 schematic is shown in Figure 7-76. The -8008-15, -16, -99-90 schematic is shown in Figure 7-77. The 8009-4, -7, -6, -8 schematic is shown in Figure 7-78. The 8009-9, -12 schematic is shown in Figure 7-79. The 8009-10, -13 schematic is shown in Figure 7-80. The 8009-11 schematic is shown in Figure 7-81. And the 8009-14, -17, -99-90, and -99-92 schematic is shown in Figure 7-82.

As shown in Figure 7-75, the **F CEN, ΔF>50 MHz**, and **F CORR** signals from the A5 PCB are summed together at the E/I Converter. The operation of this converter is similar to that described for the E/I Converter on the 8007-3 PCB. The 8008 and 8009 E/I Converters differ from the 8007's by having no heterodyne offset and by having different rest frequencies. The rest frequency is 8 GHz for the A7 YIG, 12.4 GHz for the A8 YIG, and 18 GHz for the A9 YIG.

The input to the Sweeping-Bias Supply (U7A-U7D, Q5-Q8, U1B) is from the R Sense resistor (R25). The operation of this bias supply is similar for both the 8008 and 8009 assemblies. The only operational difference is in the polarity of the bias-voltage signal as it goes through the various voltage-generation stages. The other circuit differences between the two assemblies are in the values and types of some of the components used: Several resistors have different values and all of the transistors are opposite in type (NPN on one assembly and PNP on the other).

NOTE

> Some YIG oscillator types do not require a swept bias. When one of these oscillator-types is installed, the output from the sweeping-bias supply will be a fixed voltage.

The inputs to U2C, the PIN Switch control gate, are the **L RF OFF** and **L PIN SW OFF** lines from the A4 PCB and the **H YIG SEL** line from the Bandswitch Logic. When all three of these inputs are HIGH, the **L PIN SELECT** line is TRUE. The **RF OFF** line is HIGH when the front panel RF ON switch is depressed (On). The **PIN SW OFF** line is HIGH during the forward sweep and goes LOW at the start of the sweep retrace (provided RETRACE RF is not On). The **YIG SEL** line is HIGH for the A7 PCB when the Osc 2 YIG is providing the output frequency. The line is HIGH for the A8 PCB when the Osc 3 YIG is providing the output frequency, and the line is high for the A9 PCB when the Osc 4 YIG is providing the output frequency.

The changing logic states of the two **PIN SELECT** lines operate the Osc 2, Osc 3 and Osc 4 sections of the PIN Switch in a manner similar to that described in paragraph 7-12.3 for the Het Band (**L HET PIN SELECT**). The A14 PCB PIN Switch driver circuit for Osc 2 consists of CR20, Q7, Q12, Q13, and associated components (Figure 7-76, Sheet 3). The Osc 3 drive circuit consists of CR22, Q16, Q15, Q14, and associated components (Figure 7-61, Sheet 3). The Osc 4 drive circuit consists of CR34, Q19, Q18 and Q17, and associated components (Figure 7-76, Sheet 3).

The input to the PIN Driver/Linearizer (U1A, U4B, Q3, Q4) is the **PIN MOD DRIVER** voltage signal from the A4 PCB. The operation of this circuit is the same as that described for the Pin Driver/Linearizer circuit on the 8007 PCB (paragraph 7-12.3). The PIN Modulator resistor for the Osc 2 attenuator, located inside the PIN Switch, is A14R37. The Osc 3 attenuator resistor is A14R68.

The inputs to the Bandswitch/ROM Select (U8A-U8D) are as follows:

- The **FCEN/VPF** and **F CEN** voltage signals from the A5 PCB.
- The **H SNB** and **H SNR** logic control lines from the preceeding oscillator's YIG driver PCB. For example, for the A7 PCB the lines are **H SNB 1** and **H SNR 1** from the A6 PCB. And for the A8 PCB, the lines are **H SNB 2** and **H SNR 2** from the A7 PCB. And for the A9 PCB, the lines are **H SNB 3** and **H SNR 3** from the A8 PCB.

The **FCEN/VPF** and **F CEN** voltages are compared with a voltage representing 12.4 GHz for the A7 YIG and 18 GHz for the A9 YIG. When the **FCEN/VPF** voltage equals or exceeds the comparison voltage, and if the applicable **H SNB** line is TRUE, the following occur:

- The H **SNR** 2 line for the A7 PCB and **H SNR 3** line for the A8 PCB go TRUE.
- The applicable PCB's L **ROM SEL** line goes FALSE.

When the **F CEN** voltage equals or exceeds the comparison voltage and if the applicable **H SNR** line is TRUE, the following occur:

- The applicable PCB's L **YIG SEL** and H **YIG SEL** lines go FALSE.
- The H **SNB** 2 line for the A7 PCB and the **H SNB 3** line for the A8 PCB go TRUE.

The input to the Linearizing ROM (U5) is the **ROM Bus** from the microprocessor, via the A14U6 latch on the Motherboard. The operation of this circuit is the same as that described for the Linearizing ROM on the 8007 PCB (paragraph 7-12.3).

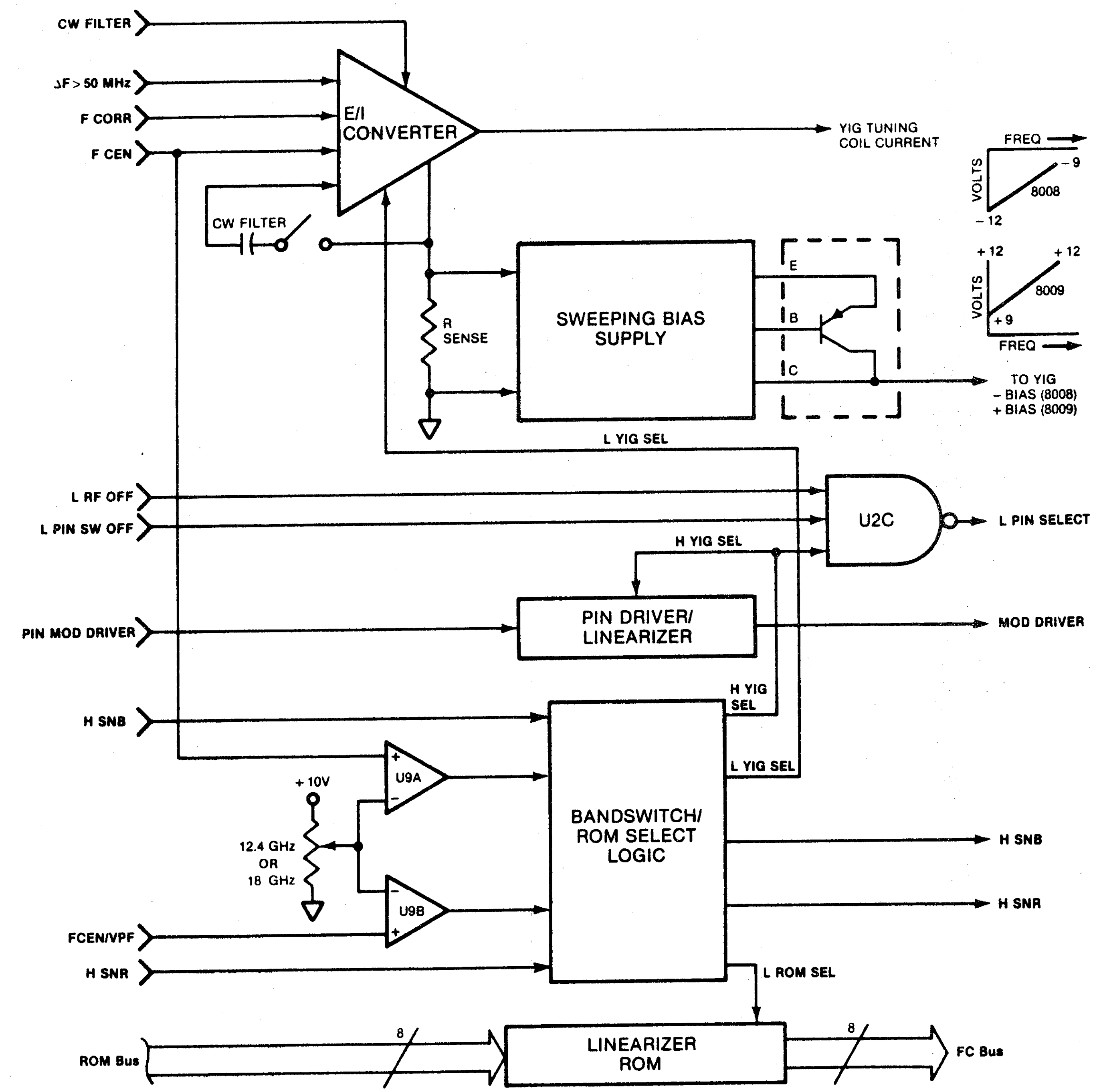
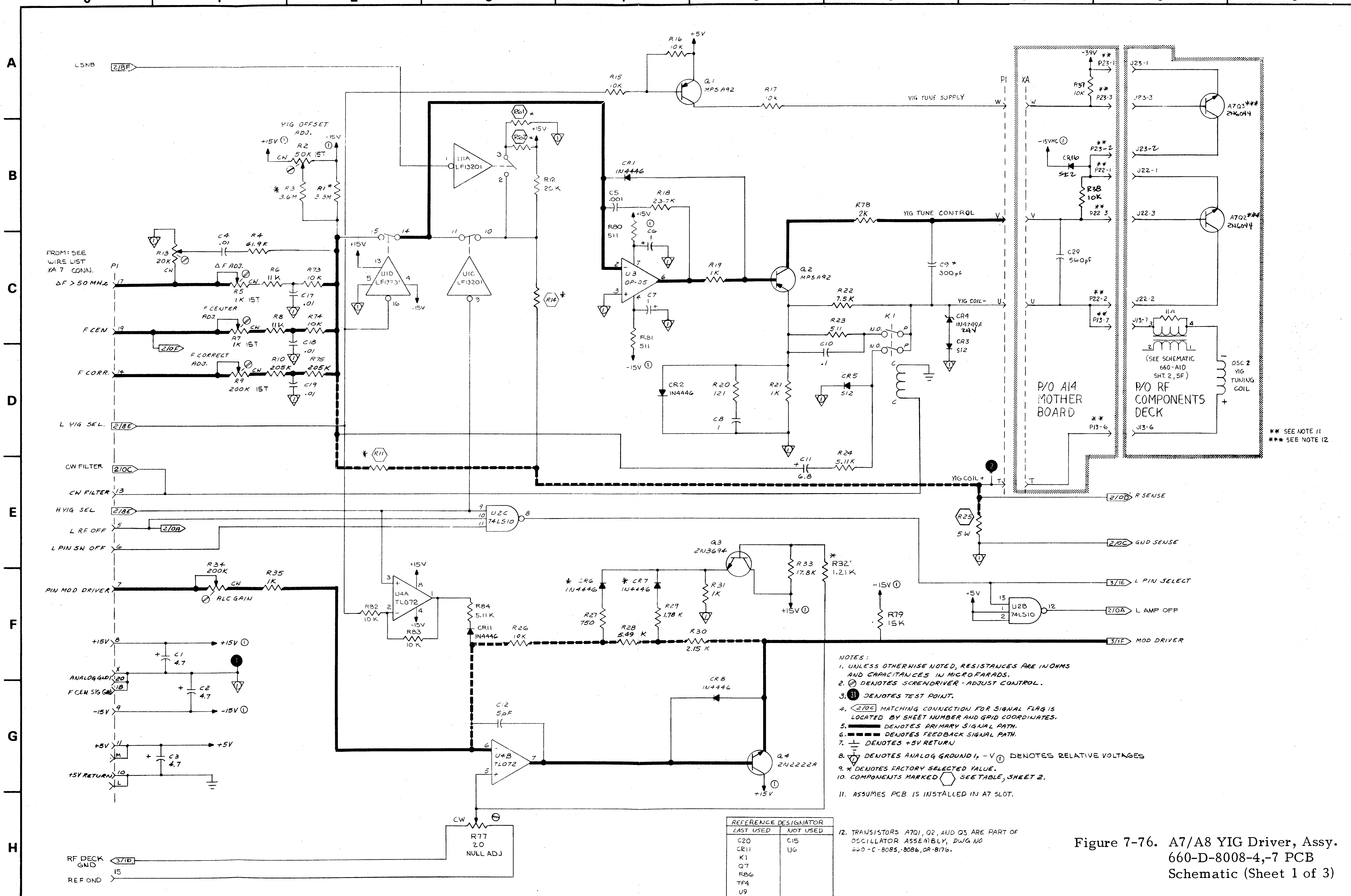


Figure 7-75. A7/A8 YIG Driver PCB (Assy 660-D-8008, -8009) Block Diagram

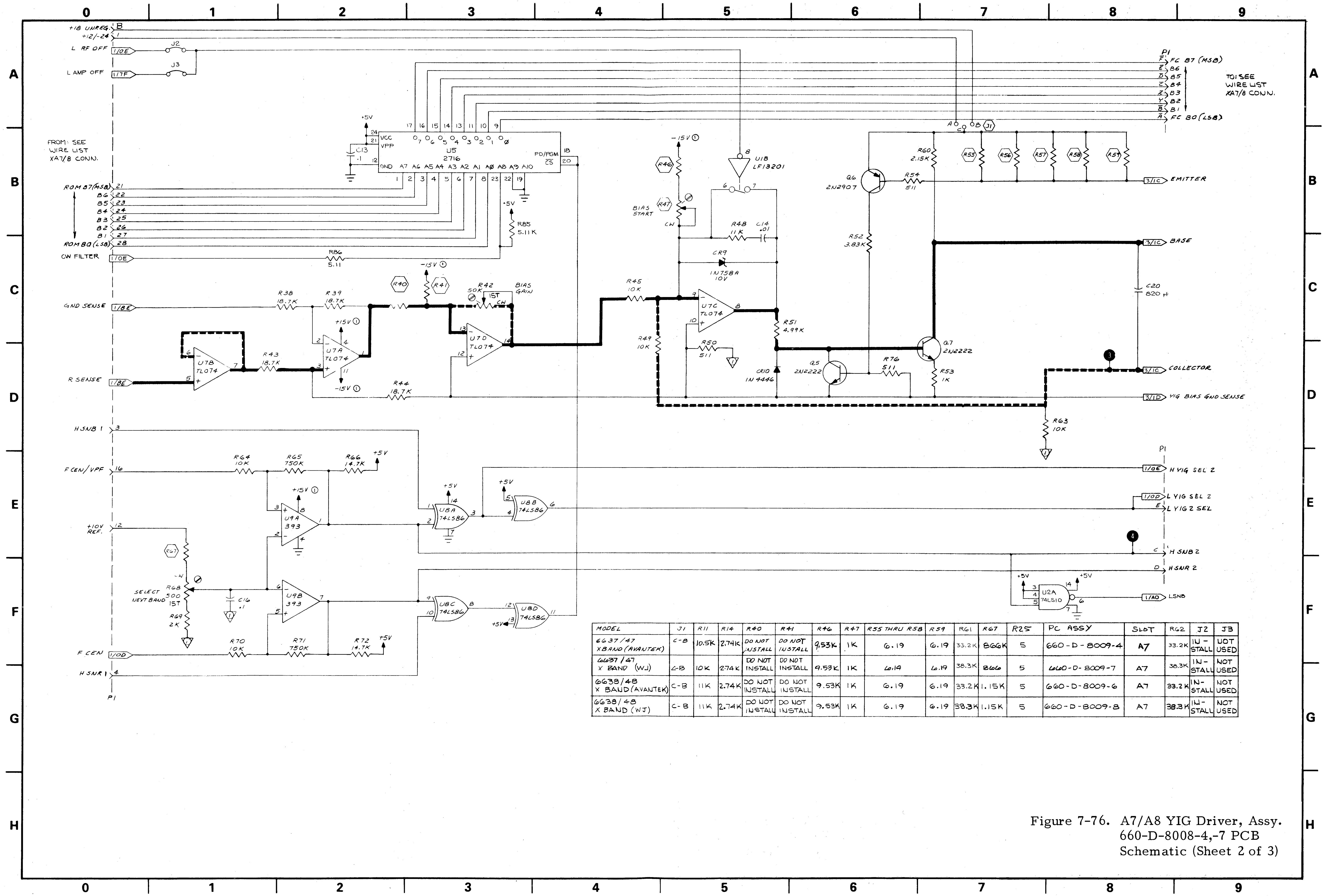


NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. (screwdriver symbol) DENOTES SCREWDRIVER-ADJUST CONTROL.
3. (31) DENOTES TEST POINT.
4. <2/0C] MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ▬▬▬ DENOTES PRIMARY SIGNAL PATH.
6. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.
7. ⏚ DENOTES +5V RETURN
8. (ground 1) DENOTES ANALOG GROUND 1, −V(1) DENOTES RELATIVE VOLTAGES
9. * DENOTES FACTORY SELECTED VALUE.
10. COMPONENTS MARKED ⬡ SEE TABLE, SHEET 2.
11. ASSUMES PCB IS INSTALLED IN A7 SLOT.
12. TRANSISTORS A7Q1, Q2, AND Q3 ARE PART OF OSCILLATOR ASSEMBLY, DWG NO 660-C-8085, -8086, OR -8176.

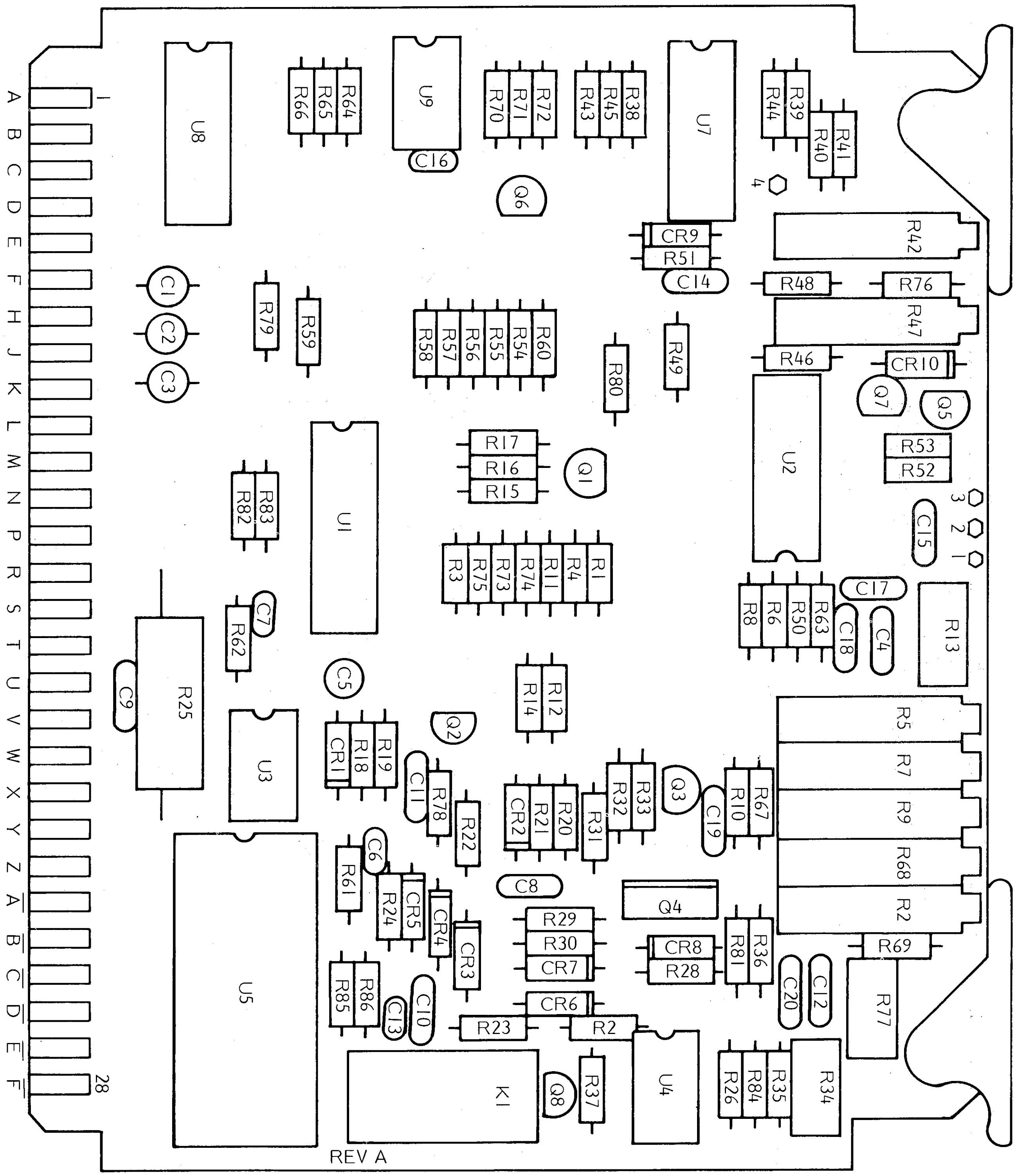
REFERENCE DESIGNATOR	
LAST USED	NOT USED
C20	C15
CR11	U6
K1	
Q7	
R86	
TP4	
U9	

Figure 7-76. A7/A8 YIG Driver, Assy. 660-D-8008-4,-7 PCB Schematic (Sheet 1 of 3)



MODEL	J1	R11	R14	R40	R41	R46	R47	R55 THRU R58	R59	R61	R67	R25	PC ASSY	SLOT	R62	J2	J3
6637/47 XBAND (AVANTEK)	C-B	10.5K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	1K	6.19	6.19	33.2K	866K	5	660-D-8009-4	A7	33.2K	IN-STALL	NOT USED
6637/47 X BAND (WJ)	C-B	10K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	1K	6.19	6.19	38.3K	866	5	660-D-8009-7	A7	38.3K	IN-STALL	NOT USED
6638/48 X BAND (AVANTEK)	C-B	11K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	1K	6.19	6.19	33.2K	1.15K	5	660-D-8009-6	A7	33.2K	IN-STALL	NOT USED
6638/48 X BAND (WJ)	C-B	11K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	1K	6.19	6.19	38.3K	1.15K	5	660-D-8009-8	A7	38.3K	IN-STALL	NOT USED

Figure 7-76. A7/A8 YIG Driver, Assy. 660-D-8008-4,-7 PCB Schematic (Sheet 2 of 3)



A7/A8 PCB Parts Locator Diagram

Figure 7-76
(Sheet 2 of 3)

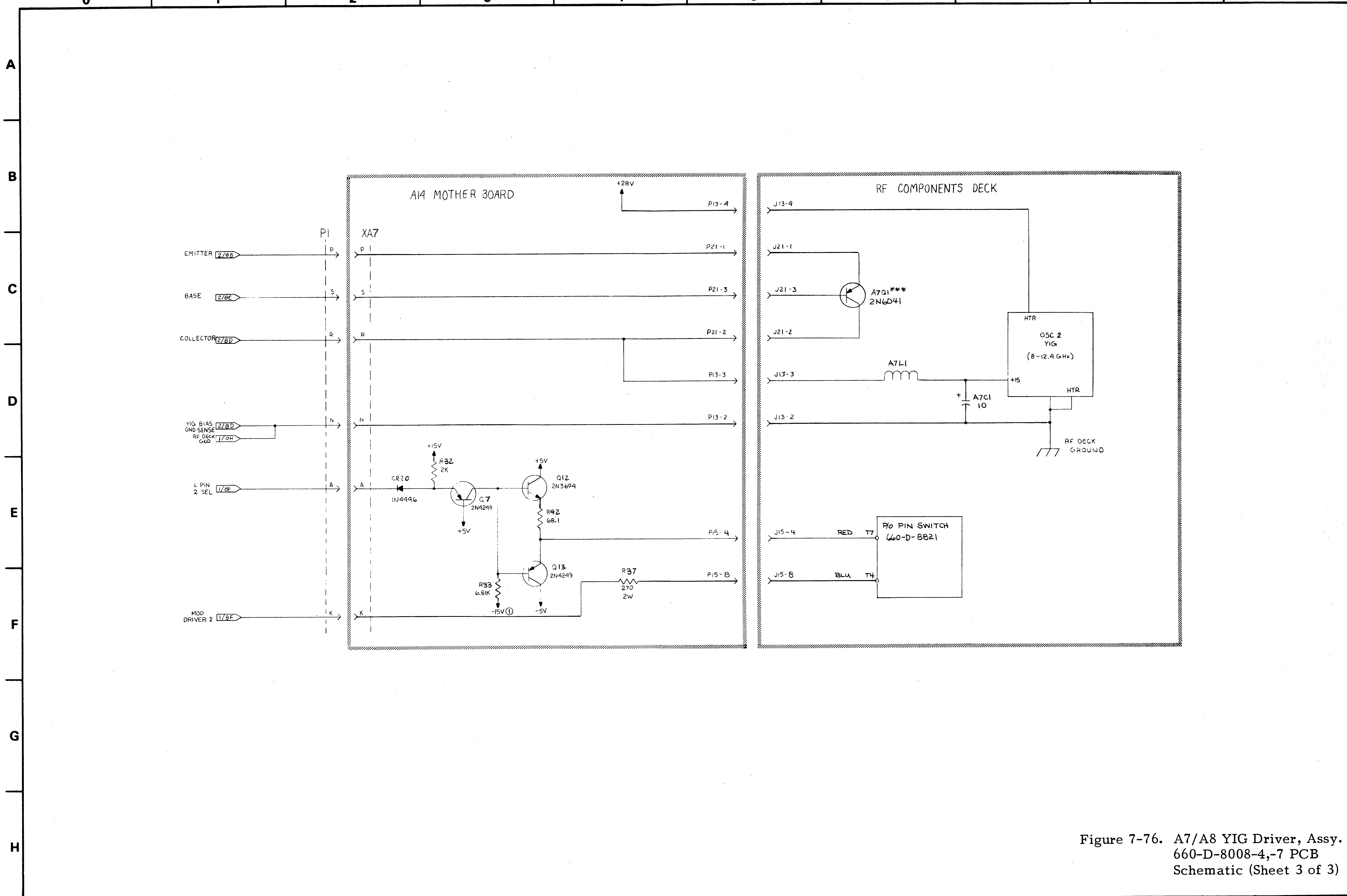
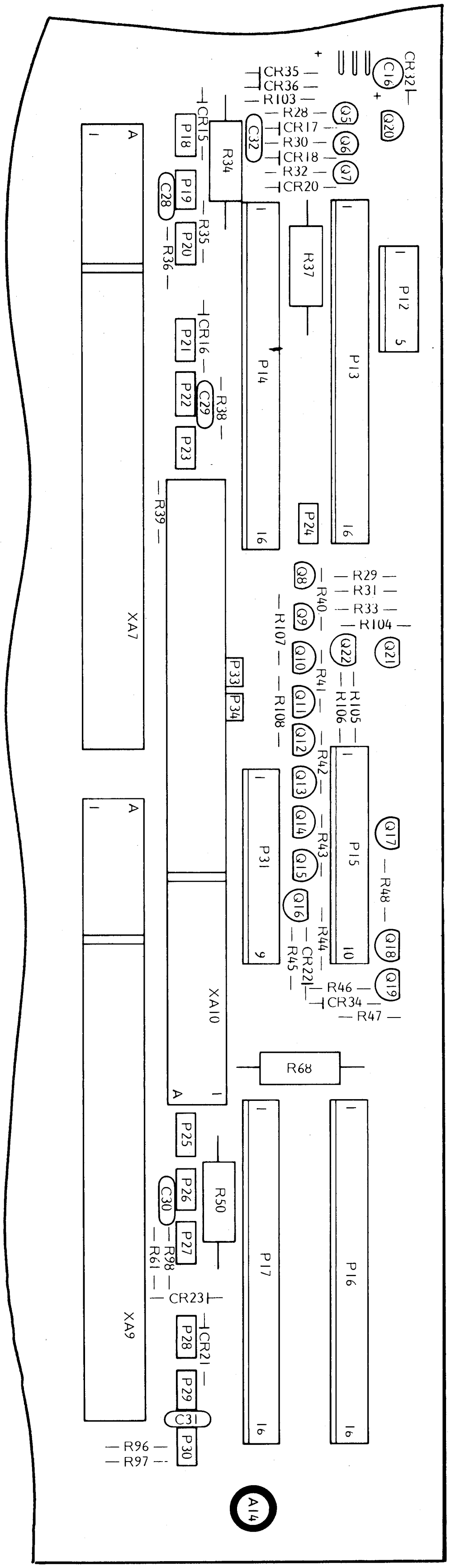
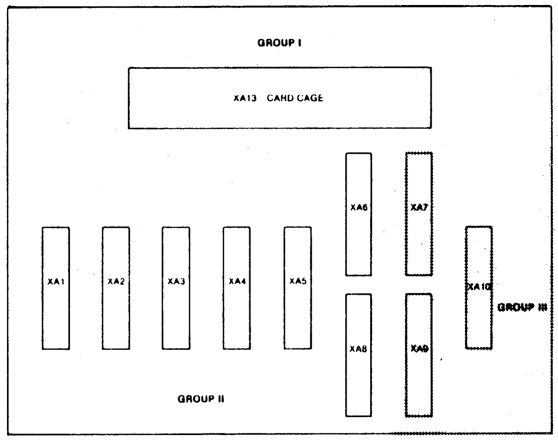


Figure 7-76. A7/A8 YIG Driver, Assy. 660-D-8008-4,-7 PCB Schematic (Sheet 3 of 3)





Osc 2 and Osc 3 YIG, PIN Driver, and PIN Modulator Parts Locator Diagram

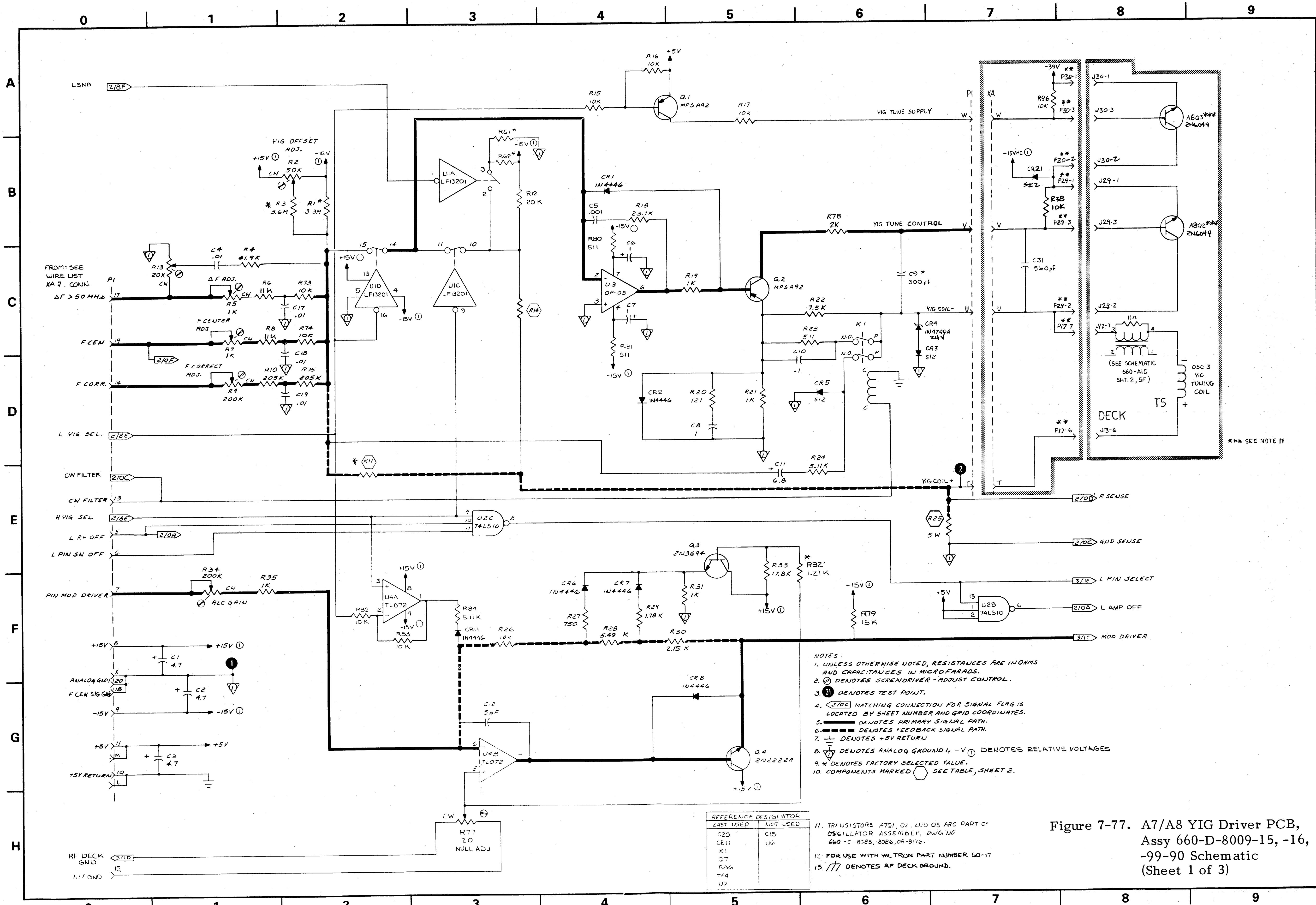
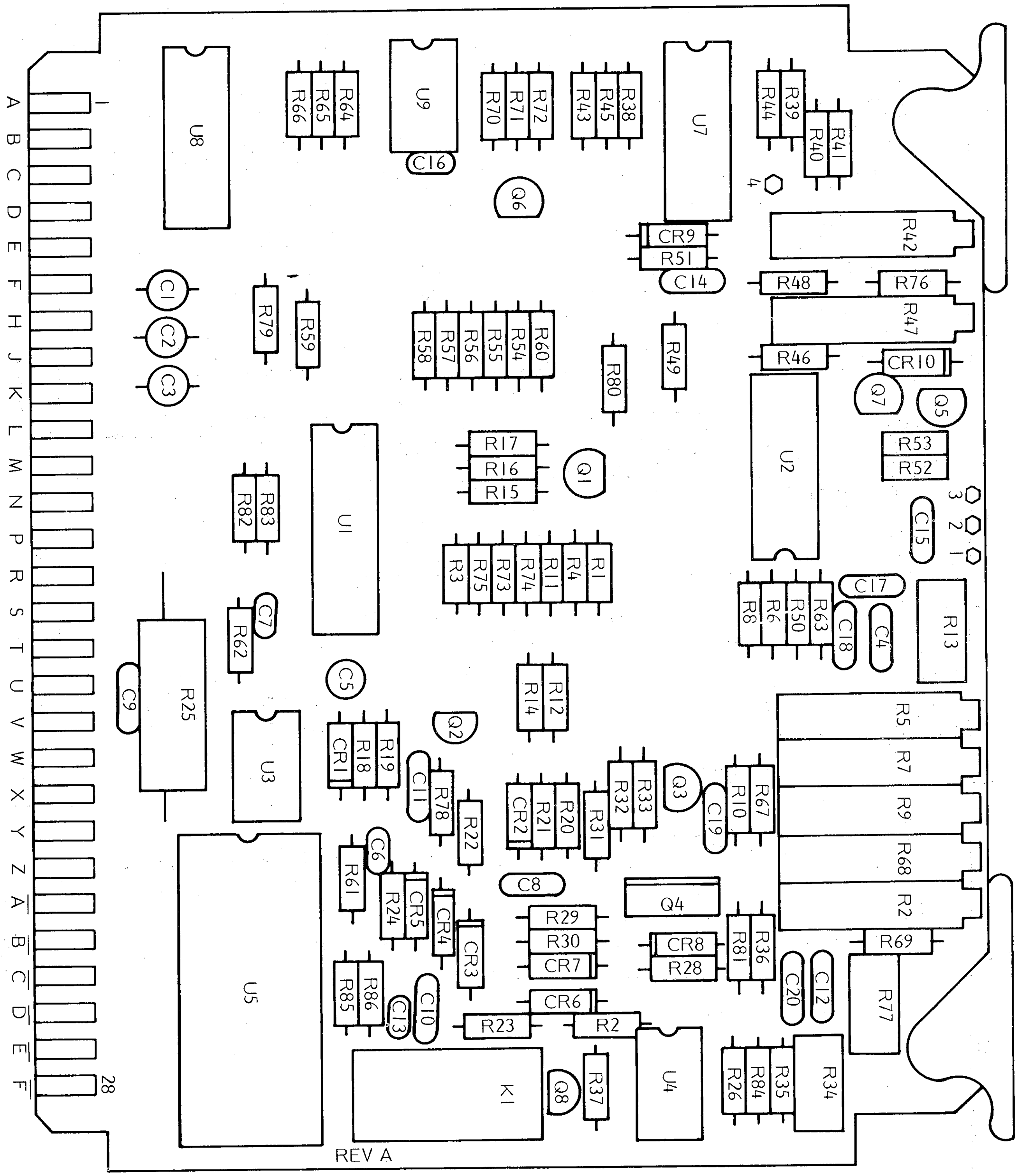
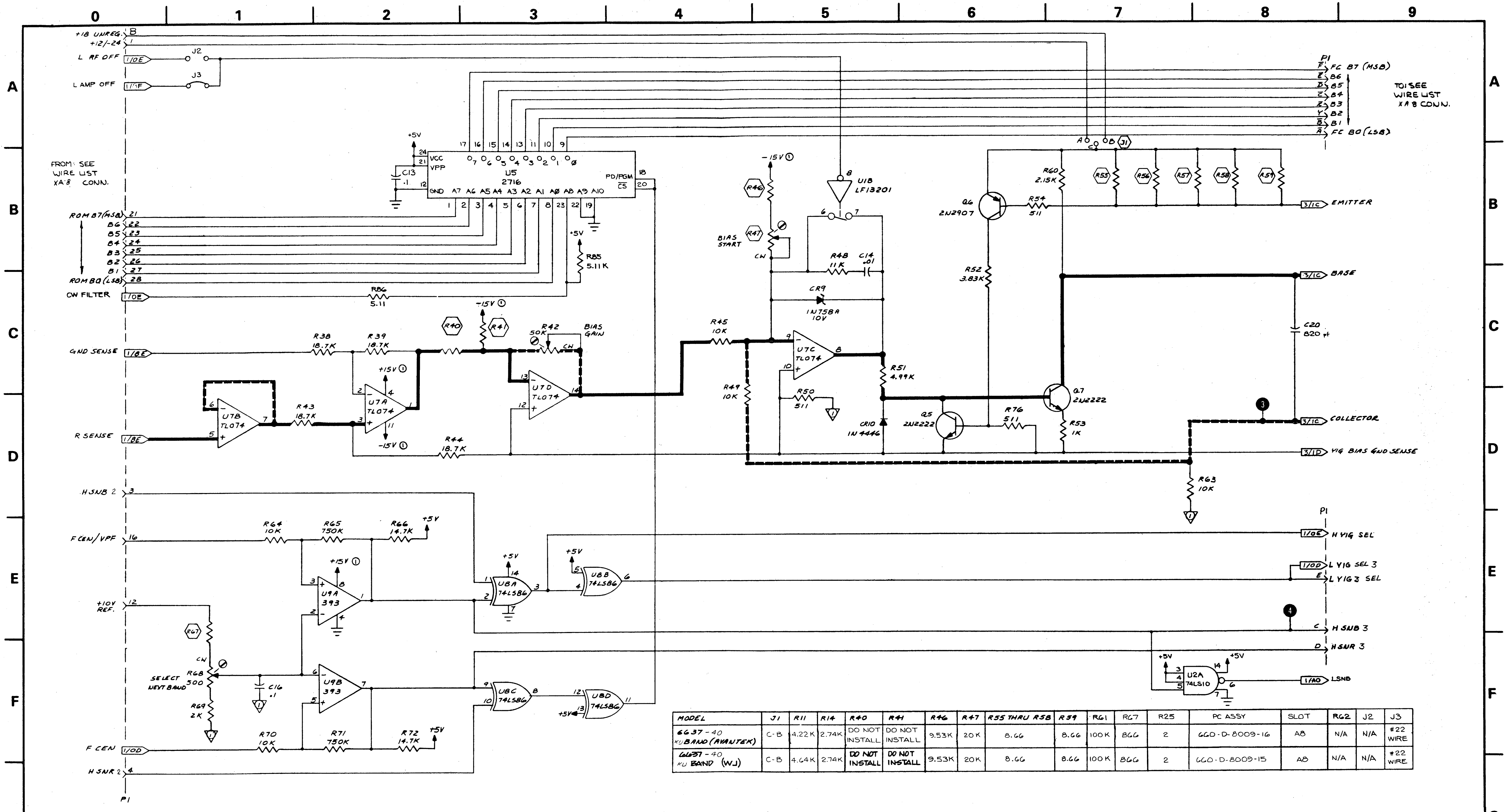


Figure 7-77. A7/A8 YIG Driver PCB, Assy 660-D-8009-15, -16, -99-90 Schematic (Sheet 1 of 3)



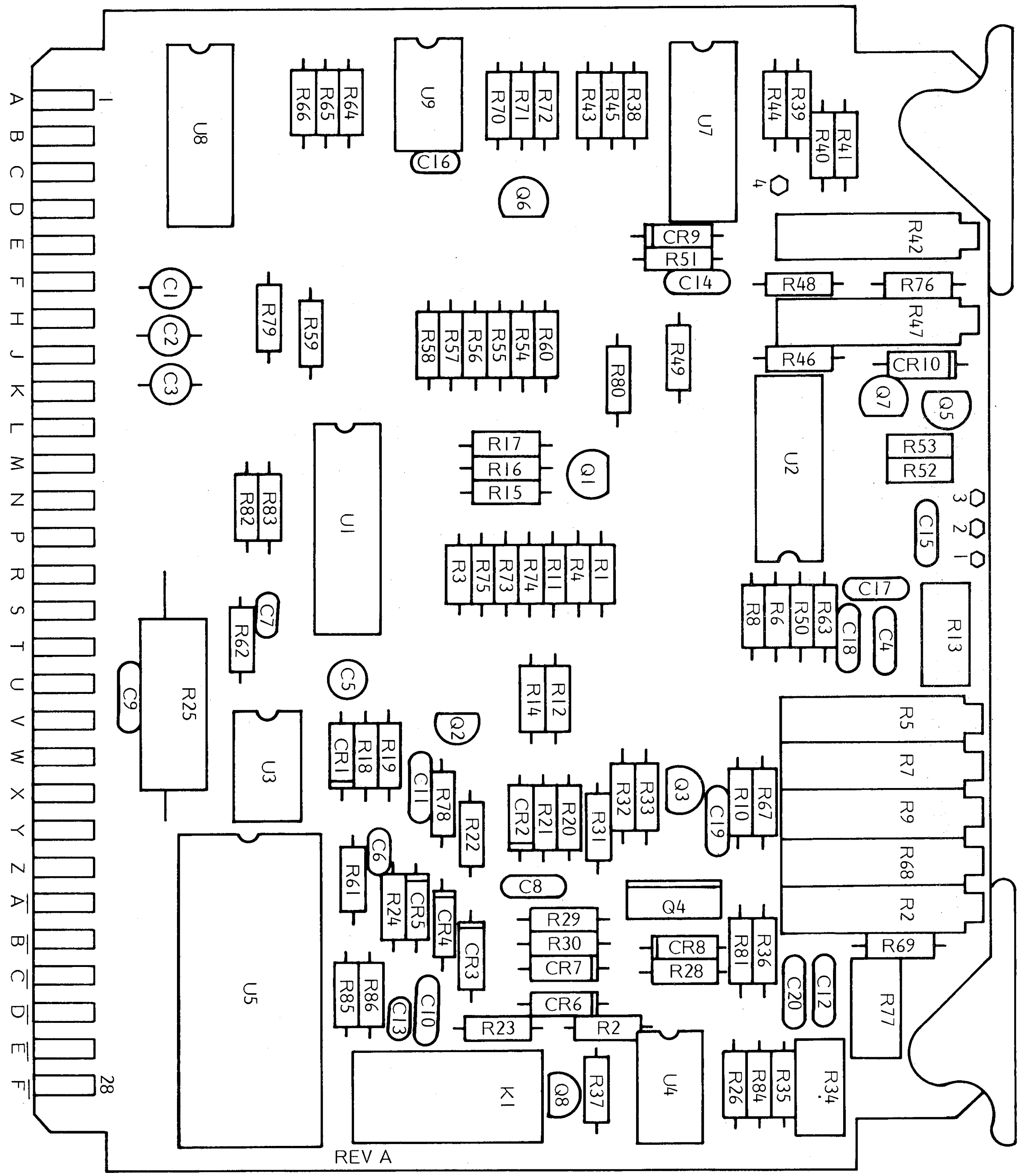
A7/A8 PCB Parts Locator Diagram

Figure 7-77
(Sheet 1 of 3)



MODEL	J1	R11	R14	R40	R41	R46	R47	R55 THRU R58	R59	R61	R67	R25	PC ASSY	SLOT	R62	J2	J3
6637-40 KU BAND (AVANTEK)	C-B	4.22K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	20K	8.66	8.66	100K	866	2	660-D-8009-16	A8	N/A	N/A	#22 WIRE
6637-40 KU BAND (WJ)	C-B	4.64K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	20K	8.66	8.66	100K	866	2	660-D-8009-15	A8	N/A	N/A	#22 WIRE

Figure 7-77. A7/A8 YIG Driver PCB, Assy 660-D-8009-15, -16, -99-90 Schematic (Sheet 2 of 3)



A7/A8 PCB Parts Locator Diagram

Figure 7-77
(Sheet 2 of 3)

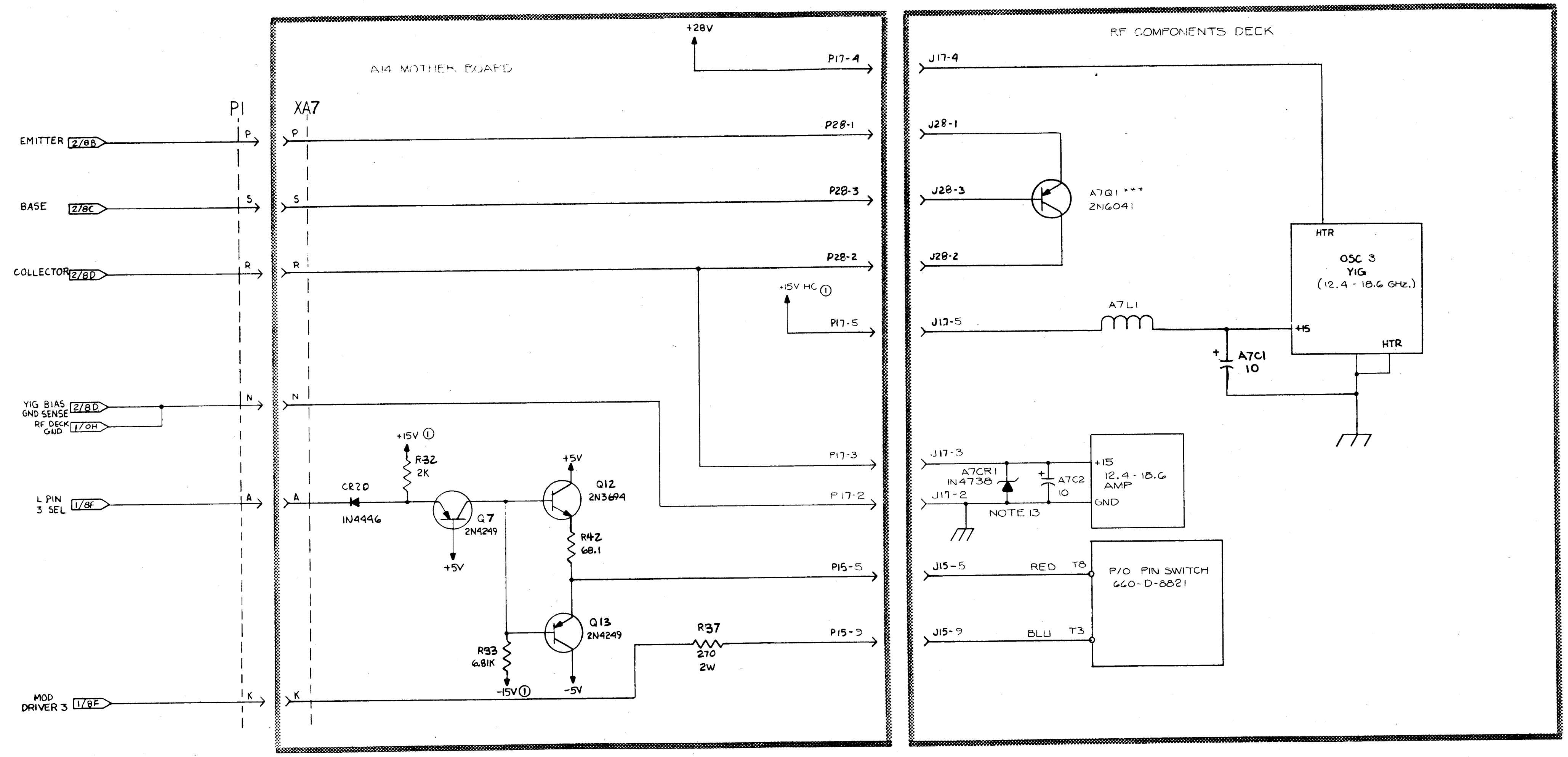
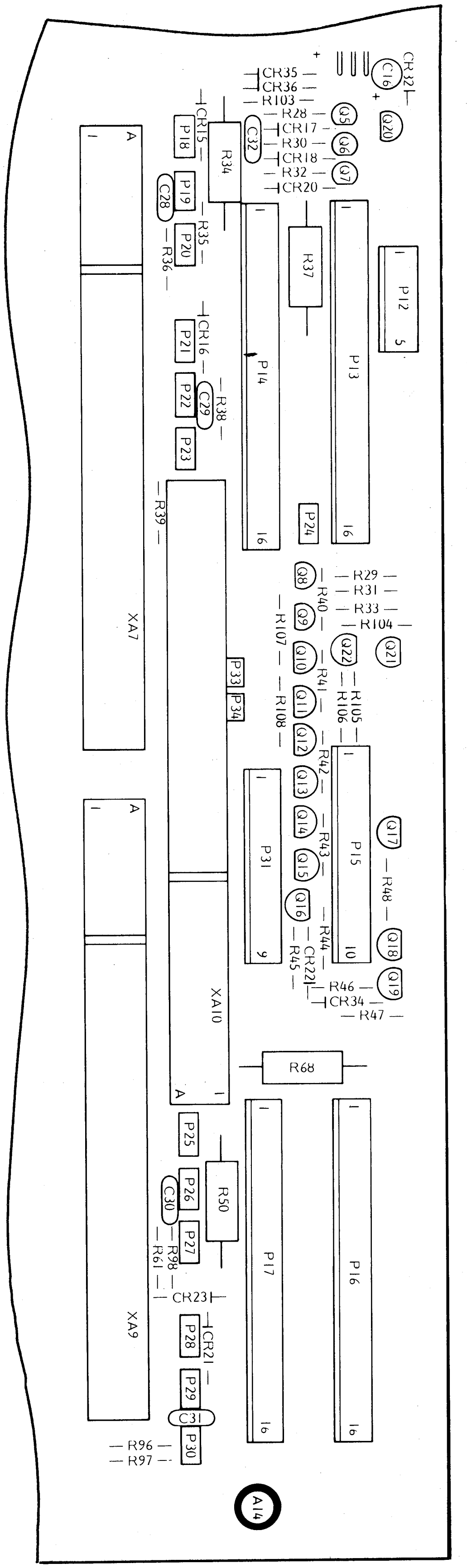
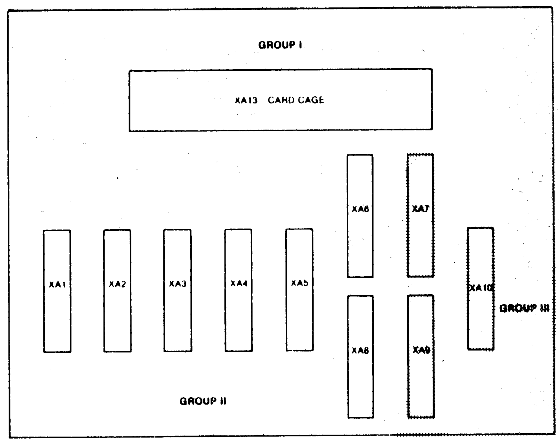


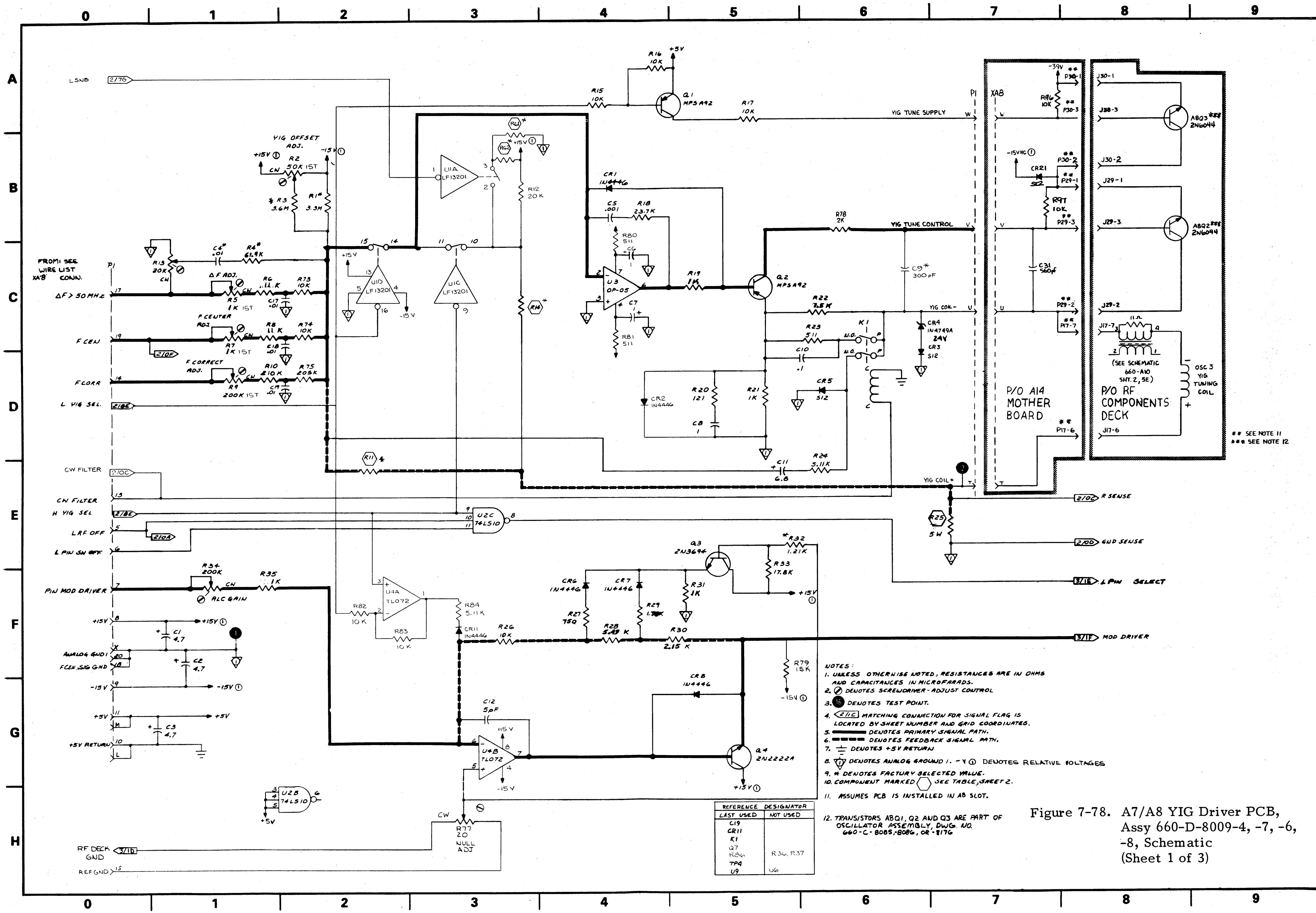
Figure 7-77. A7/A8 YIG Driver PCB, Assy 660-D-8009-15, -16, -99-90 Schematic (Sheet 3 of 3)





Osc 2 and Osc 3 YIG, PIN Driver, and PIN Modulator Parts Locator Diagram

Figure 7-77 (Sheet 3 of 3)

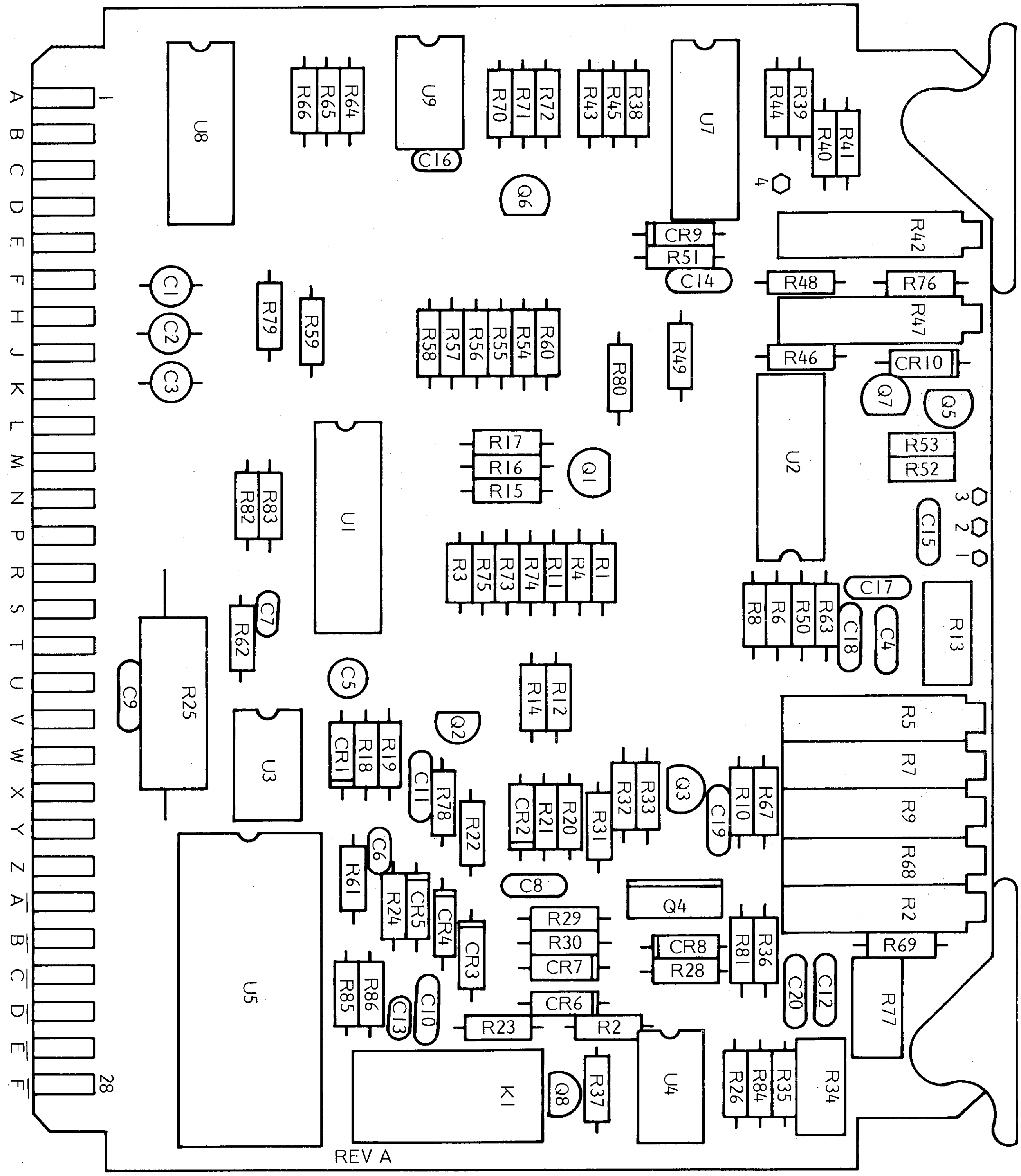


NOTES:

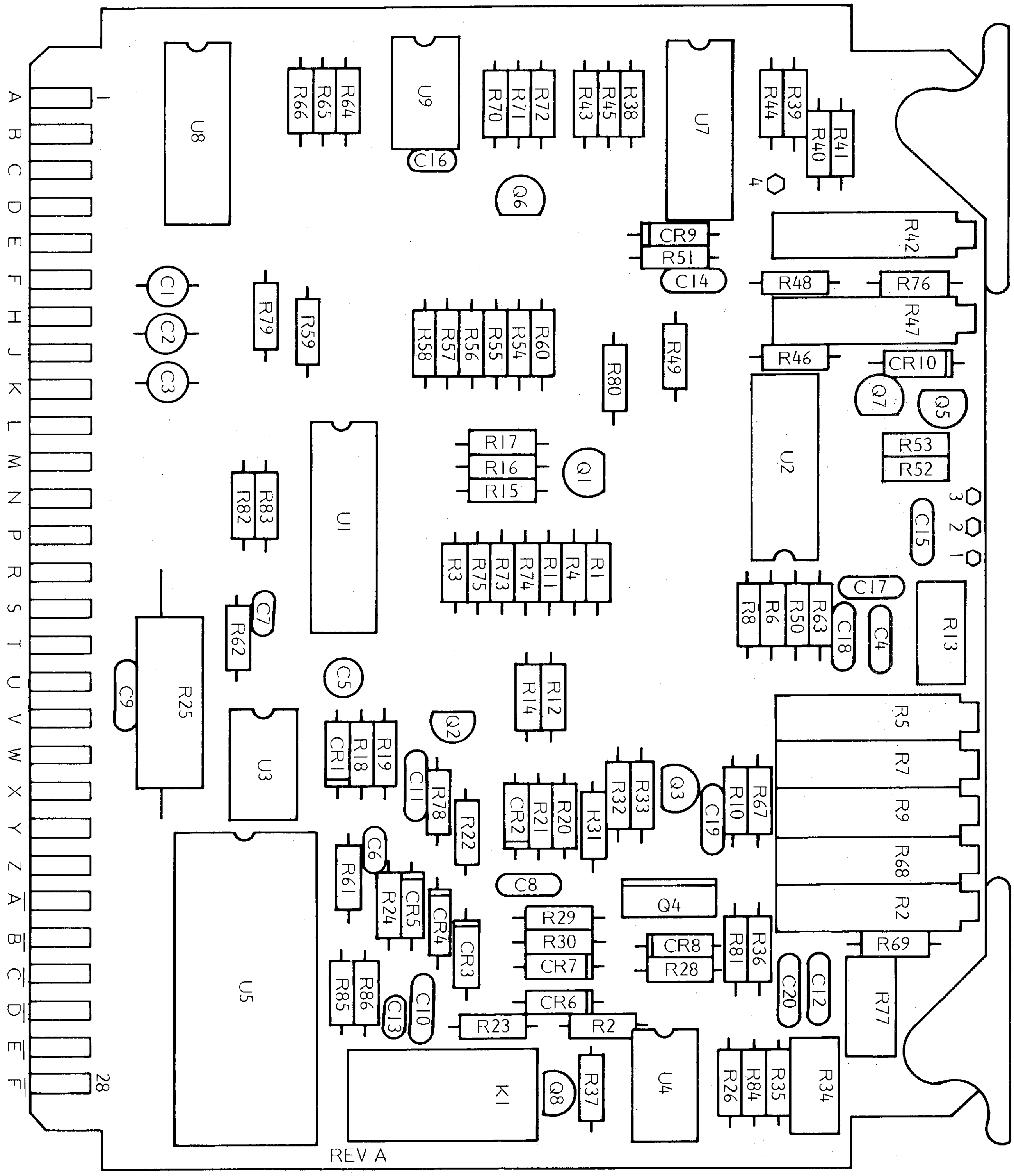
1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. ⊘ DENOTES SCREWDRIVER-ADJUST CONTROL
3. ⓰ DENOTES TEST POINT.
4. 2/1C MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ▬▬▬ DENOTES PRIMARY SIGNAL PATH.
6. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.
7. ⏚ DENOTES +5V RETURN
8. ① DENOTES ANALOG GROUND 1. -V ① DENOTES RELATIVE VOLTAGES
9. * DENOTES FACTORY SELECTED VALUE.
10. COMPONENT MARKED ⬡ SEE TABLE, SHEET 2.
11. ASSUMES PCB IS INSTALLED IN A8 SLOT.
12. TRANSISTORS A8Q1, Q2 AND Q3 ARE PART OF OSCILLATOR ASSEMBLY, DWG. NO. 660-C-8085, -8086, OR -8176

REFERENCE DESIGNATOR	
LAST USED	NOT USED
C19	
CR11	
K1	
Q7	
R86	R36, R37
TP4	
U9	U6

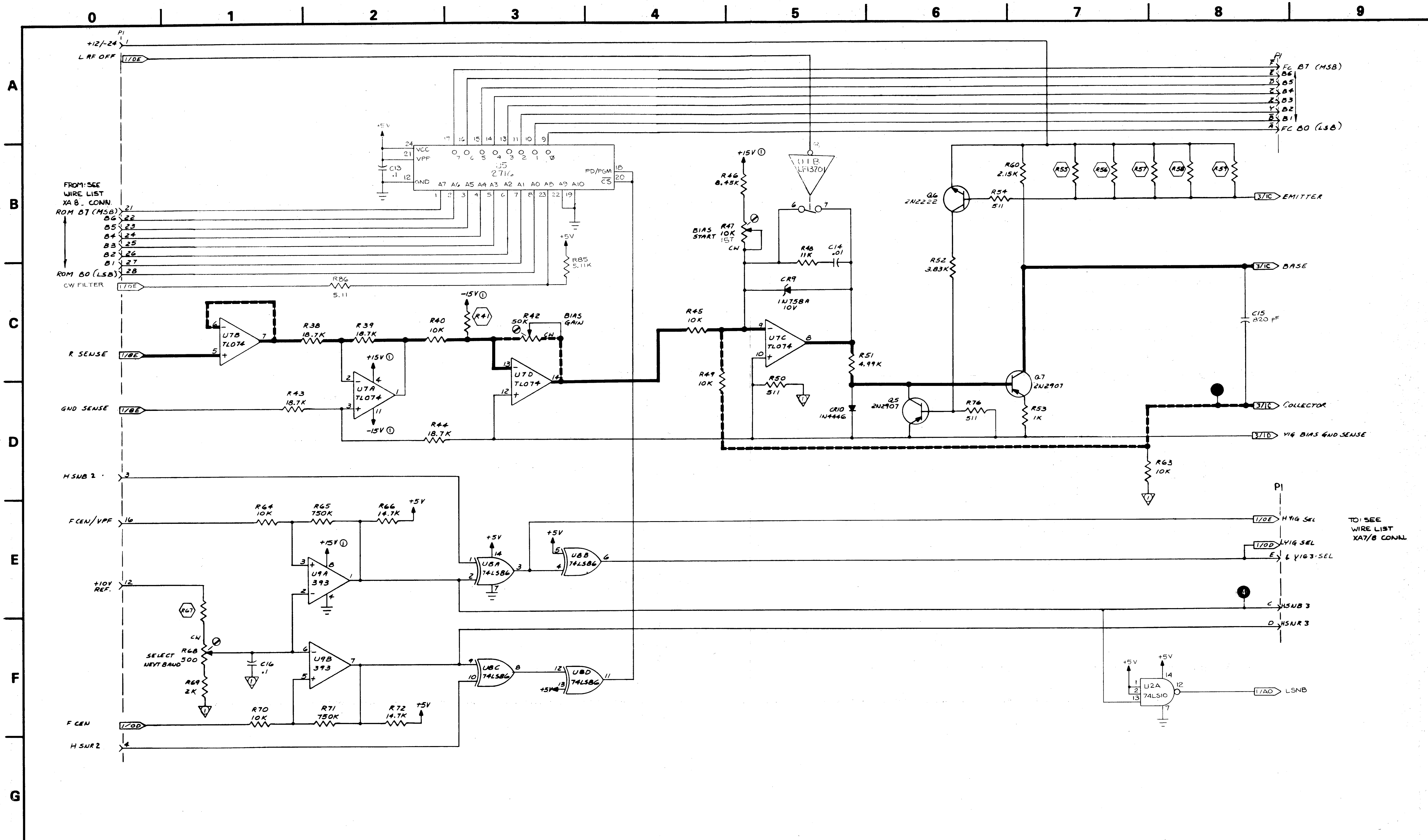
Figure 7-78. A7/A8 YIG Driver PCB, Assy 660-D-8009-4, -7, -6, -8, Schematic (Sheet 1 of 3)



A7/A8 PCB Parts Locator Diagram



A7/A8 PCB Parts Locator Diagram



MODEL	R11	R14	R41	R55 THRU R58	R61	R59	R62	R67	R25	PC ASSY.	SLOT
6637/47 KU BAND (W-J)	4.64K	1.87K	110K	8.06 Ω	110K	.5 Ω	NOT USED	5.11 Ω	3 Ω	660-D-80084	A8
6638/48 KU BAND (W-J)	5.11K	1.87K	110K	8.06 Ω	110K	.5 Ω	NOT USED	5.11 Ω	3 Ω	660-D-8008-7	A8

Figure 7-78. A7/A8 YIG Driver PCB, Assy 660-D-8009-4, -7, -6, -8, Schematic (Sheet 2 of 3)

parts locator

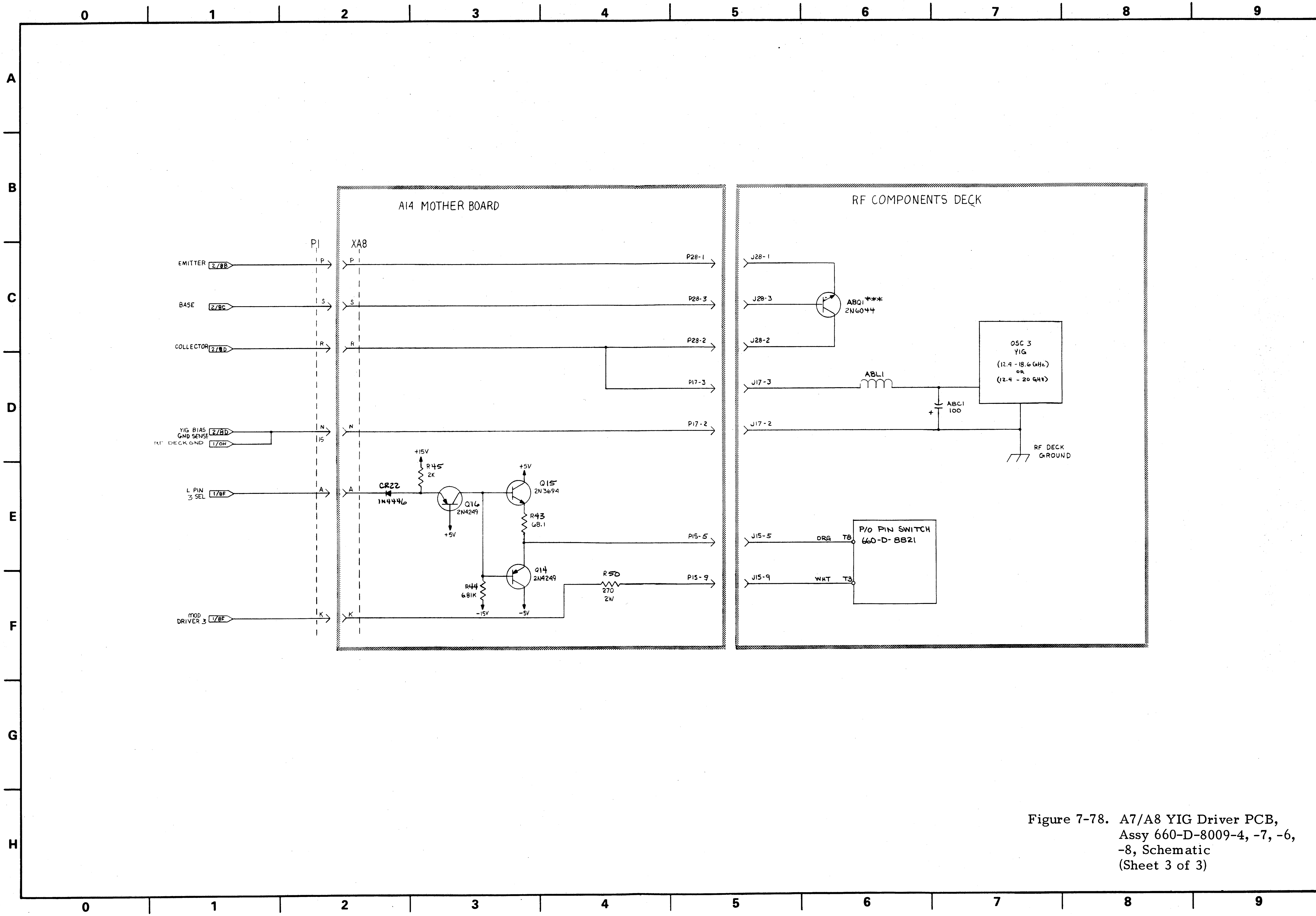
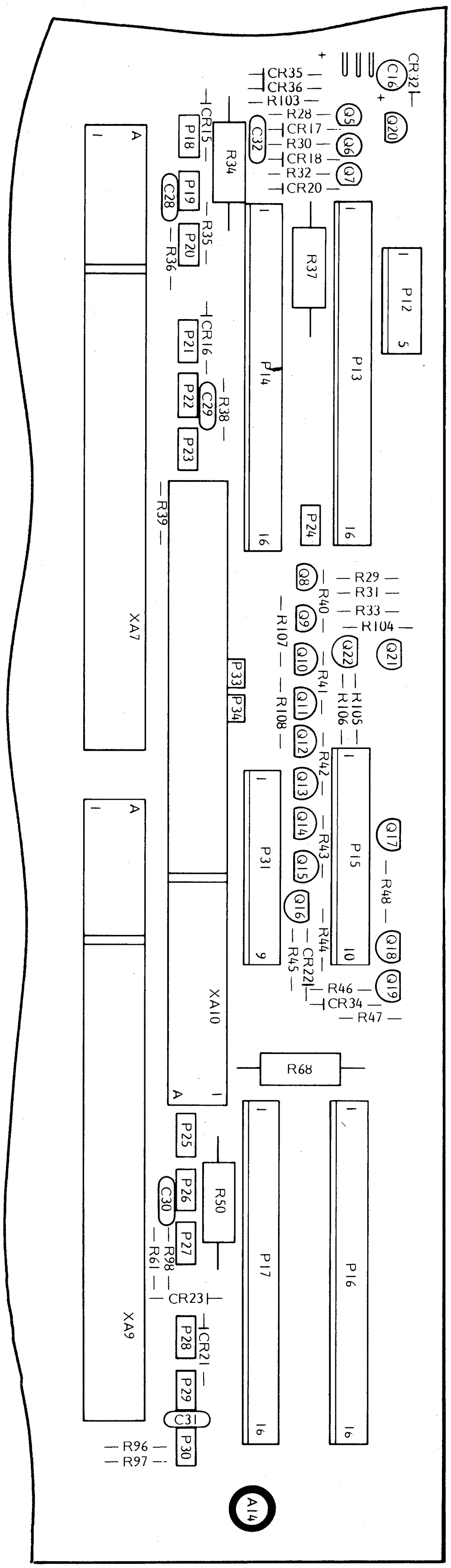
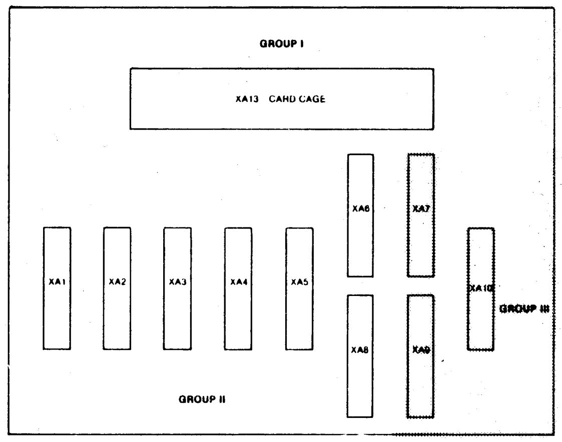


Figure 7-78. A7/A8 YIG Driver PCB, Assy 660-D-8009-4, -7, -6, -8, Schematic (Sheet 3 of 3)





Osc 2 and Osc 3 YIG, PIN Driver, and PIN Modulator Parts Locator Diagram

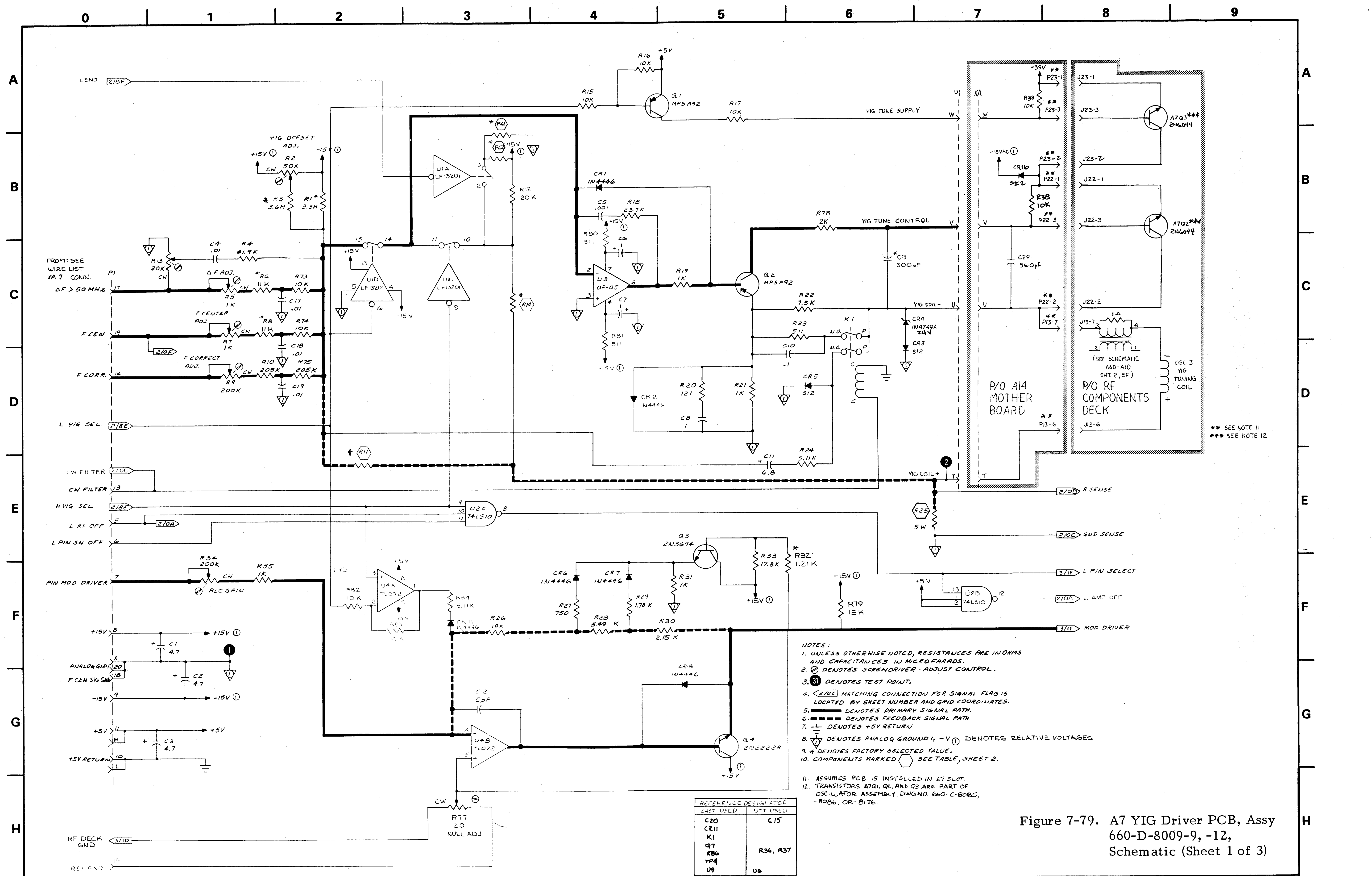
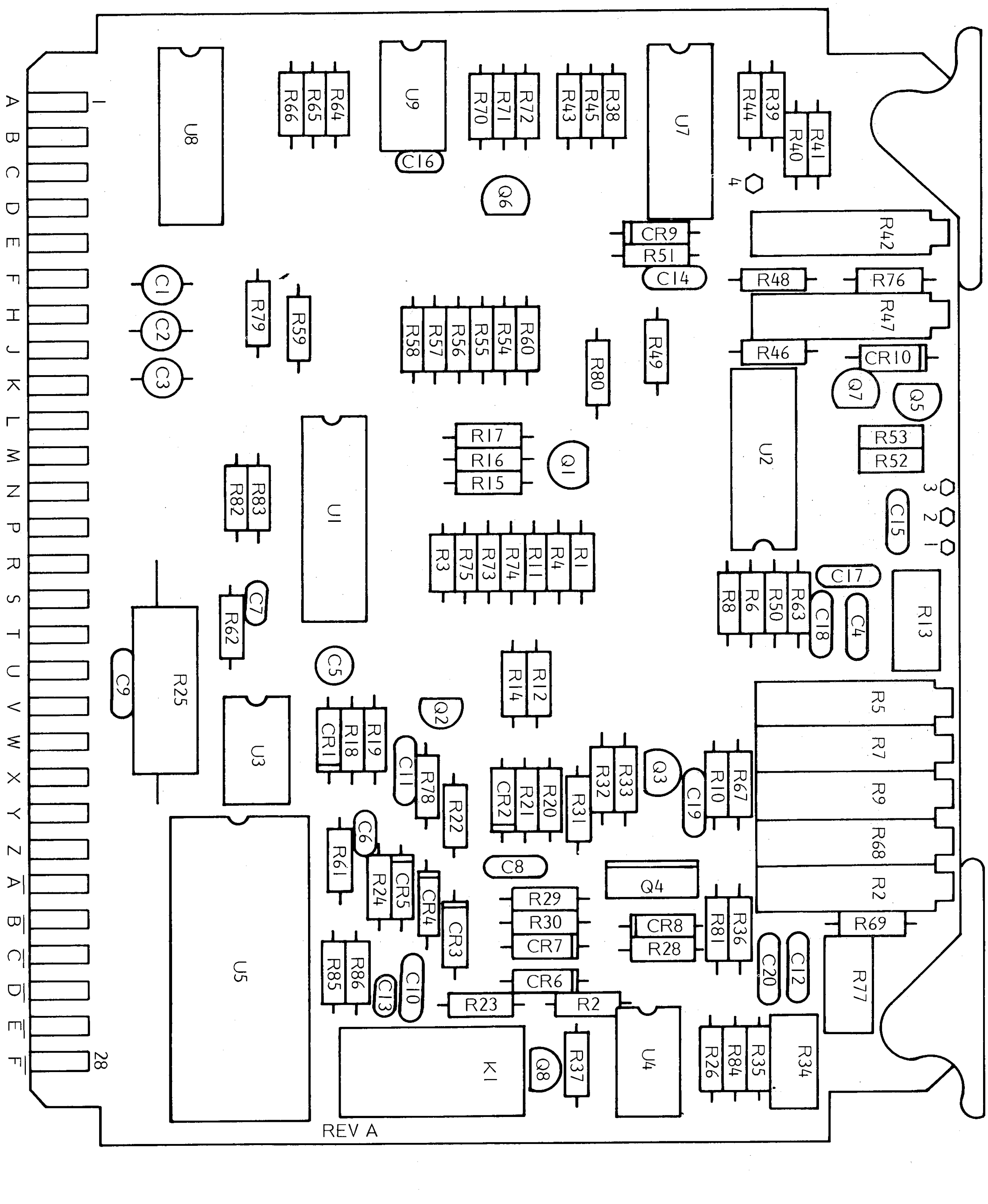
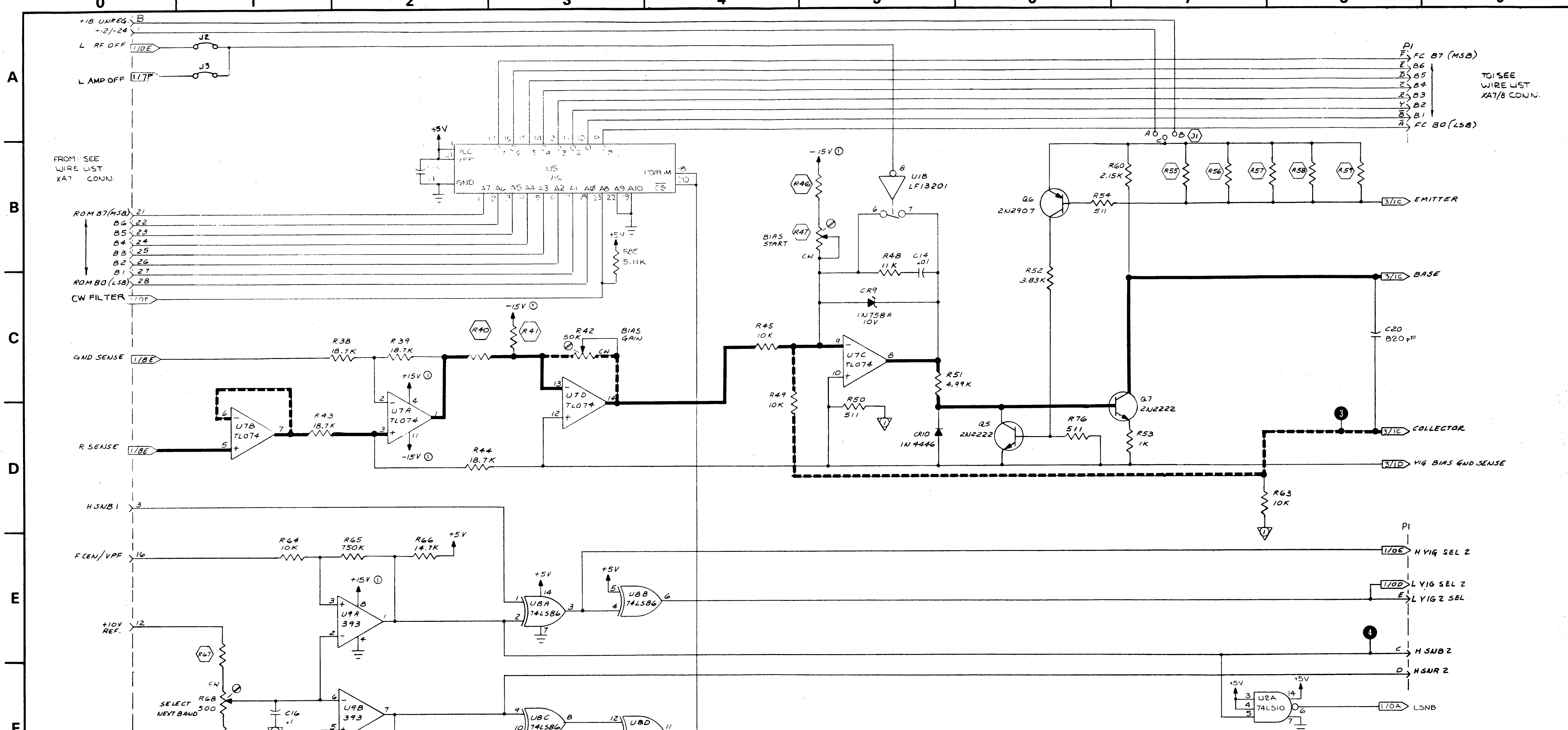


Figure 7-79. A7 YIG Driver PCB, Assy 660-D-8009-9, -12, Schematic (Sheet 1 of 3)



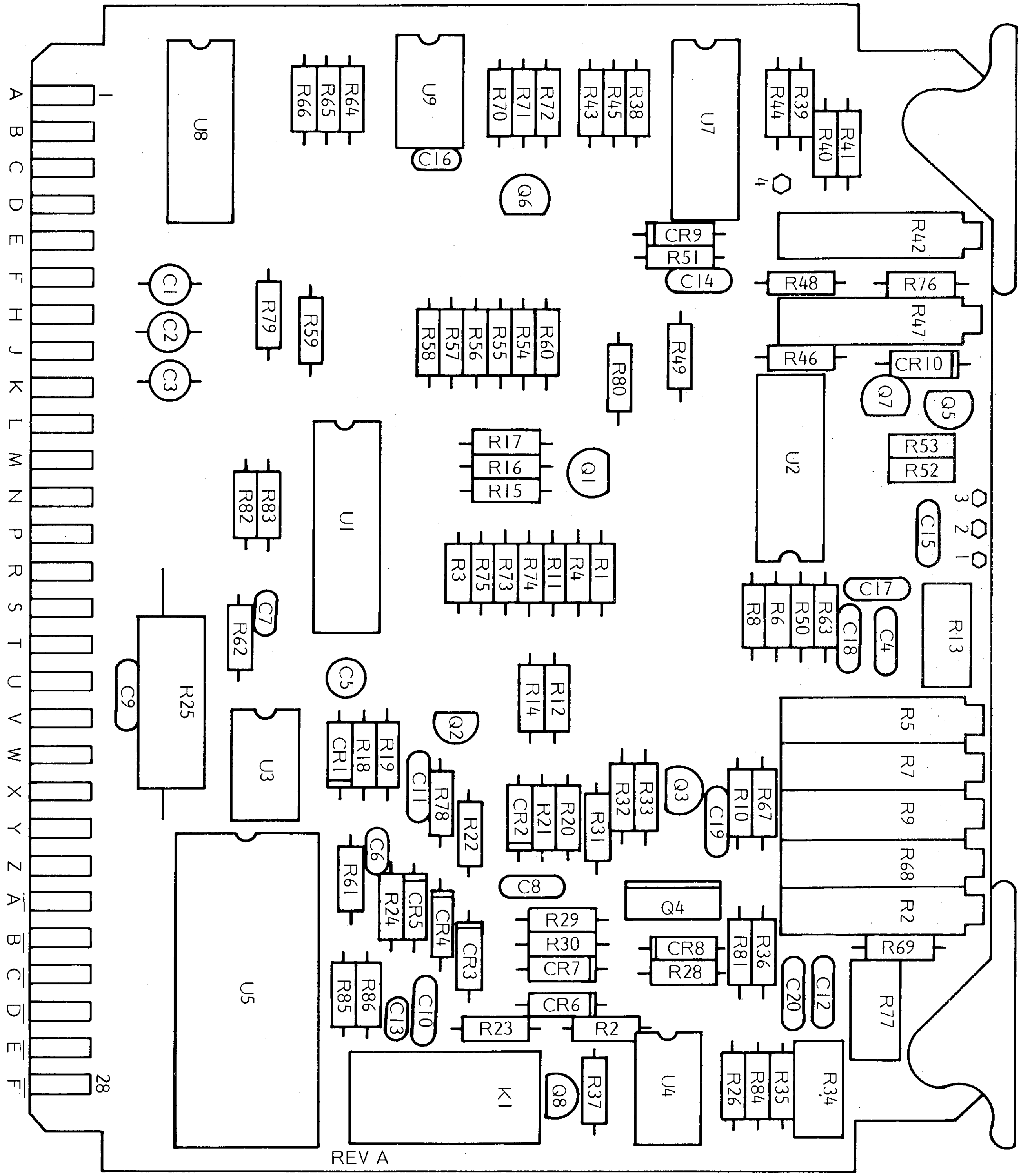
A7/A8 PCB Parts Locator Diagram

Figure 7-79
(Sheet 1 of 3)



OSC MFR	DC. ASSEMBLY	R11	R14	R61	R67	R40	R41	R46	R47	R55-58	R59	R25	J1	R62	J2	J3
AVANTEK	660-D-8009-9	14.7K	2.61K	33.2K	2.26K	N/R	N/R	9.53K	1K	6.19	6.19	5	C-B	33.2K	IN-STALL	NOT USED
WJ	660-D-8009-12	14.0K	2.61K	38.3K	2.26K	N/R	N/R	9.53K	1K	6.19	6.19	5	C-B	38.3K	IN-STALL	NOT USED

Figure 7-79. A7 YIG Driver PCB, Assy 660-D-8009-9, -12, Schematic (Sheet 2 of 3)



A7/A8 PCB Parts Locator Diagram

Figure 7-79
(Sheet 2 of 3)

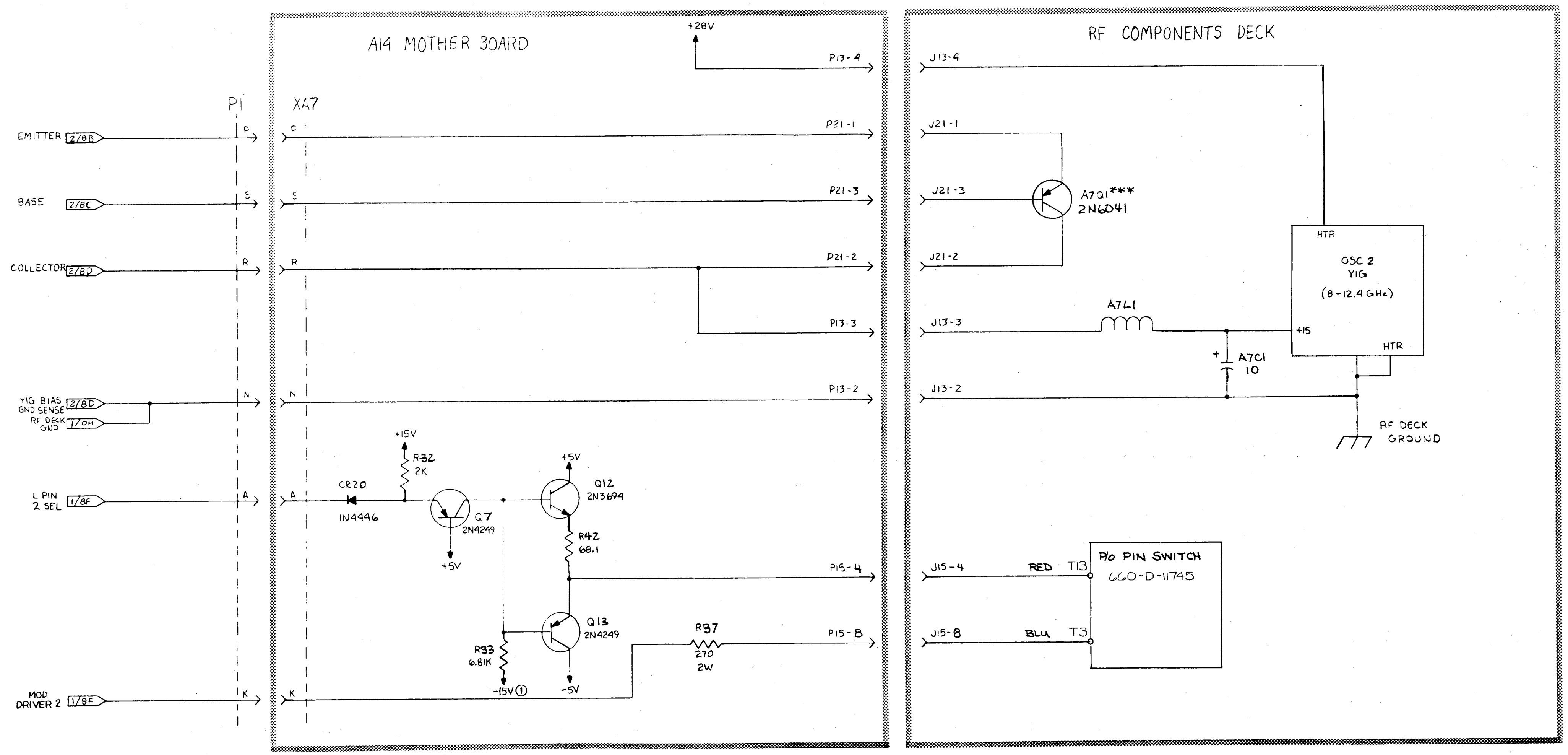
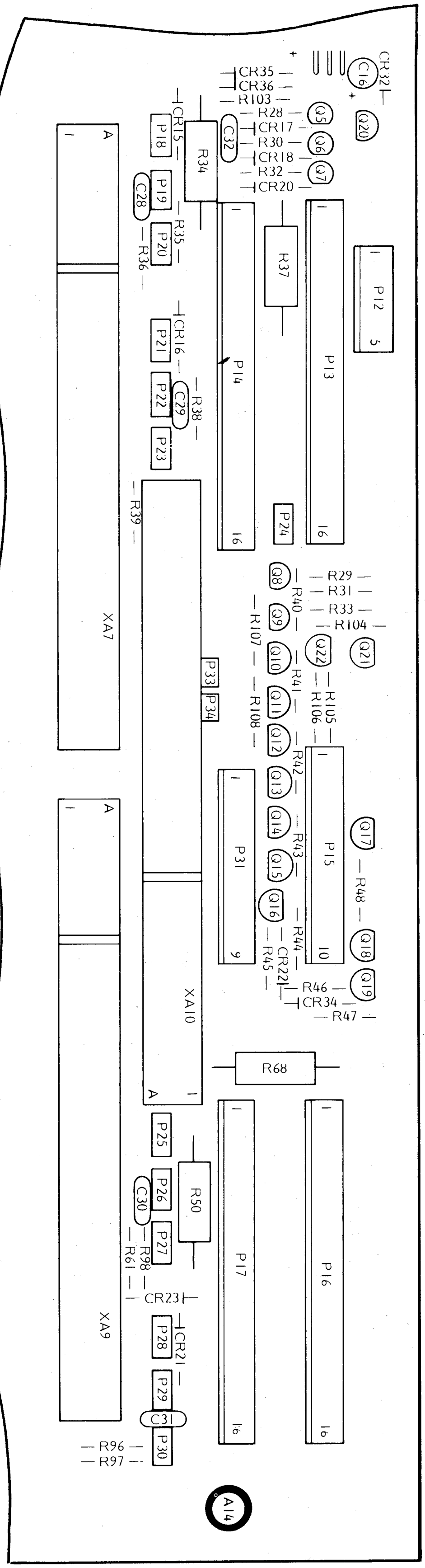
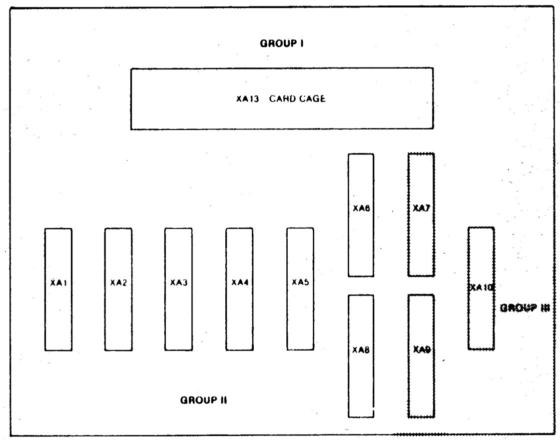


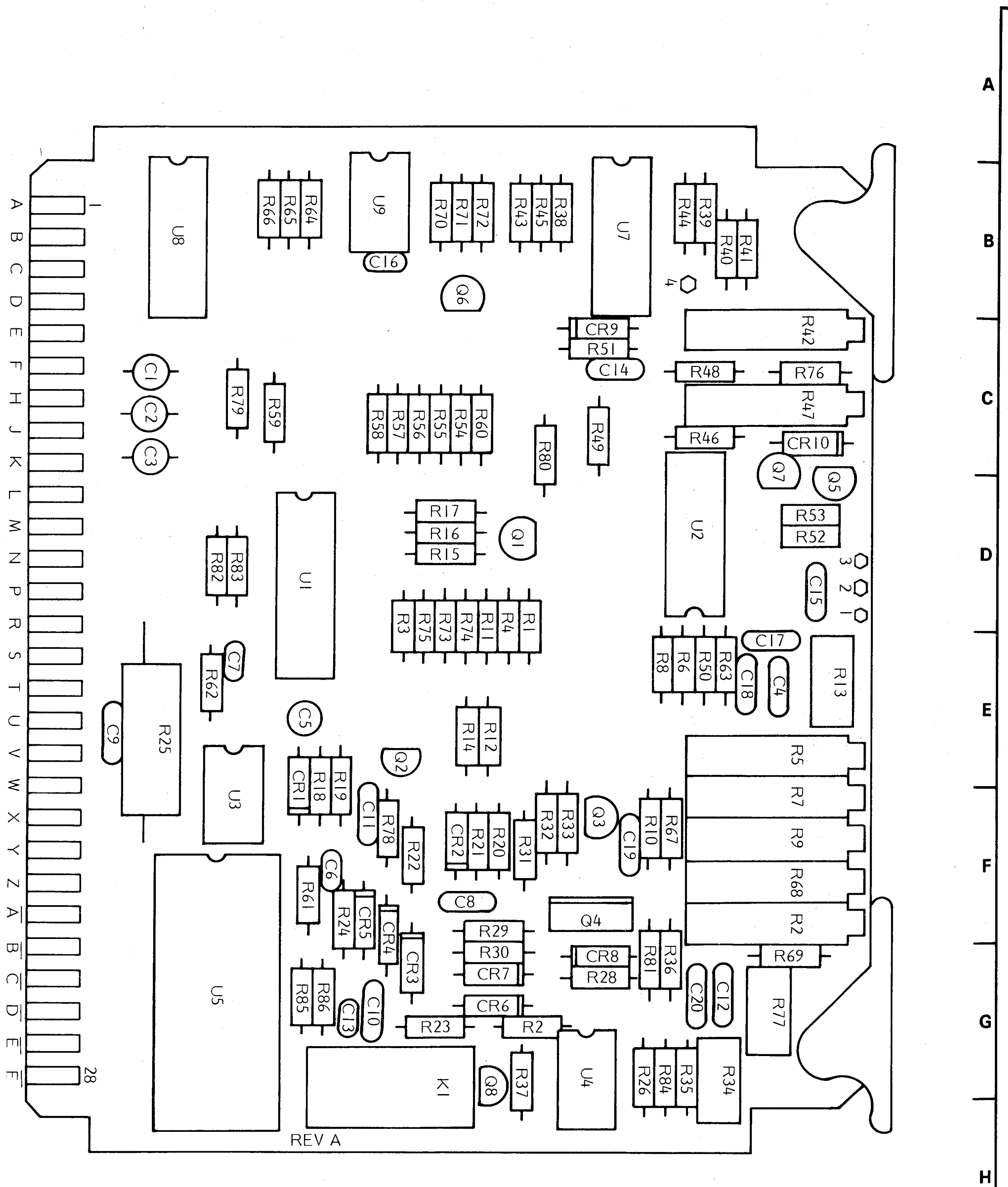
Figure 7-79. A7 YIG Driver PCB, Assy 660-D-8009-9, -12, Schematic (Sheet 3 of 3)



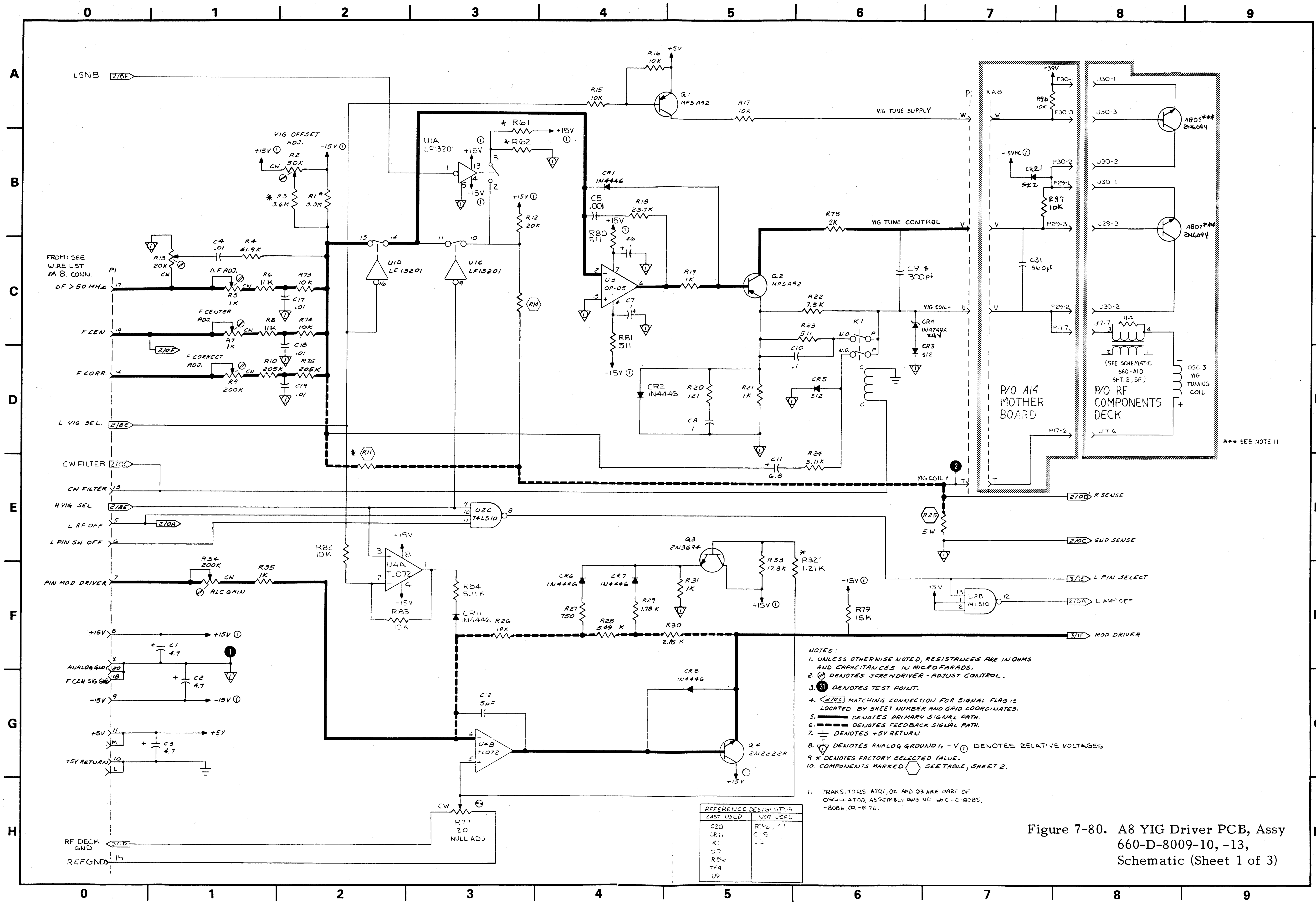


Osc 2 and Osc 3 YIG, PIN Driver, and PIN Modulator Parts Locator Diagram

Figure 7-79
(Sheet 3 of 3)



A7/A8 PCB Parts Locator Diagram



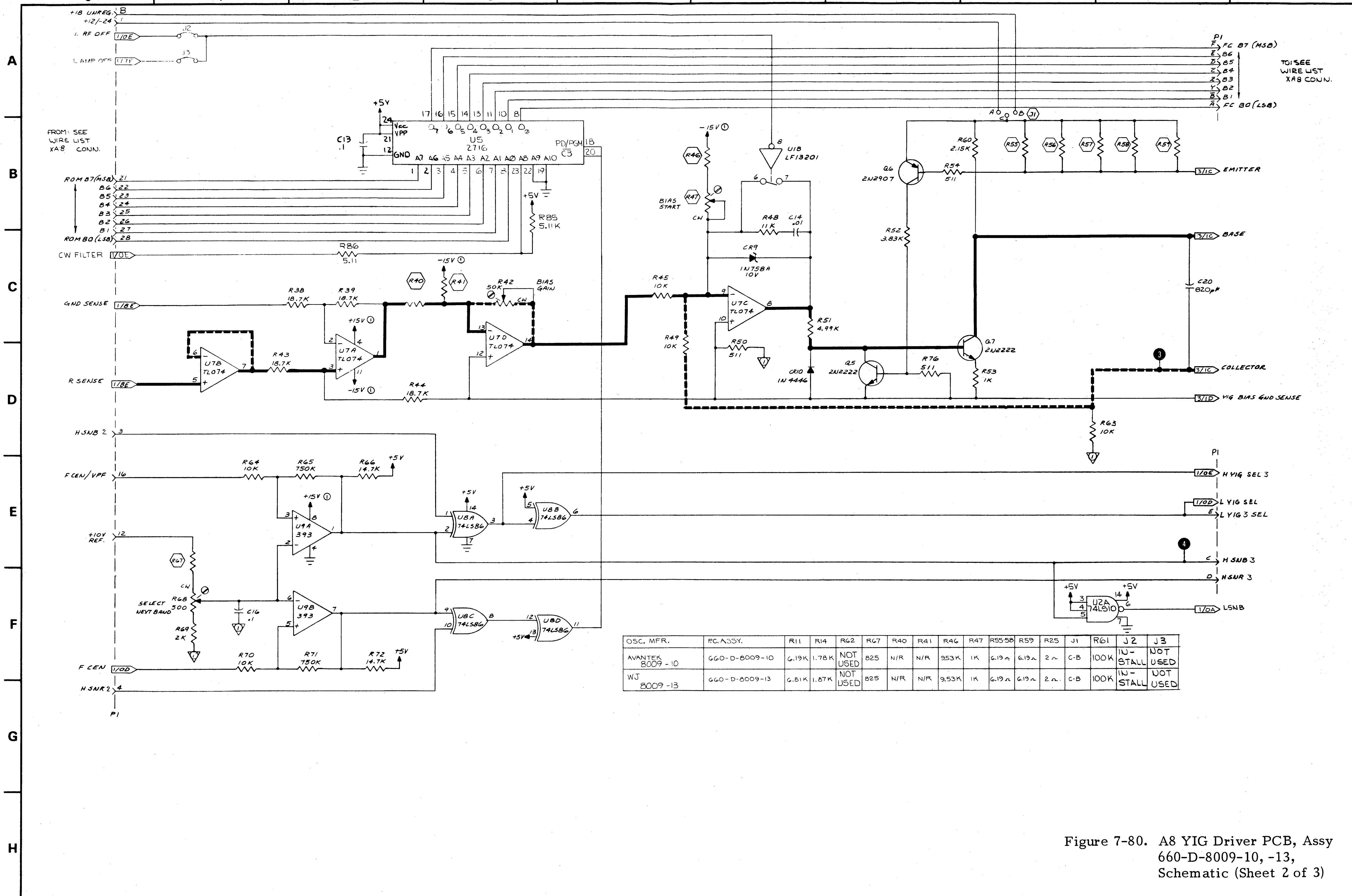
NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. ⊘ DENOTES SCREWDRIVER-ADJUST CONTROL.
3. (31) DENOTES TEST POINT.
4. <2/0C] MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ▬▬ DENOTES PRIMARY SIGNAL PATH.
6. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.
7. ⏚ DENOTES +5V RETURN
8. ▽(1) DENOTES ANALOG GROUND 1, −V(1) DENOTES RELATIVE VOLTAGES
9. * DENOTES FACTORY SELECTED VALUE.
10. COMPONENTS MARKED ⬡ SEE TABLE, SHEET 2.
11. TRANSISTORS A7Q1, Q2, AND Q3 ARE PART OF OSCILLATOR ASSEMBLY DWG NO 660-C-8085, -8086, OR -8176.

REFERENCE DESIGNATOR	
LAST USED	NOT USED
C20	R36, 21
CR11	C15
K1	[illegible]
Q7	
R86	
TP4	
U9	

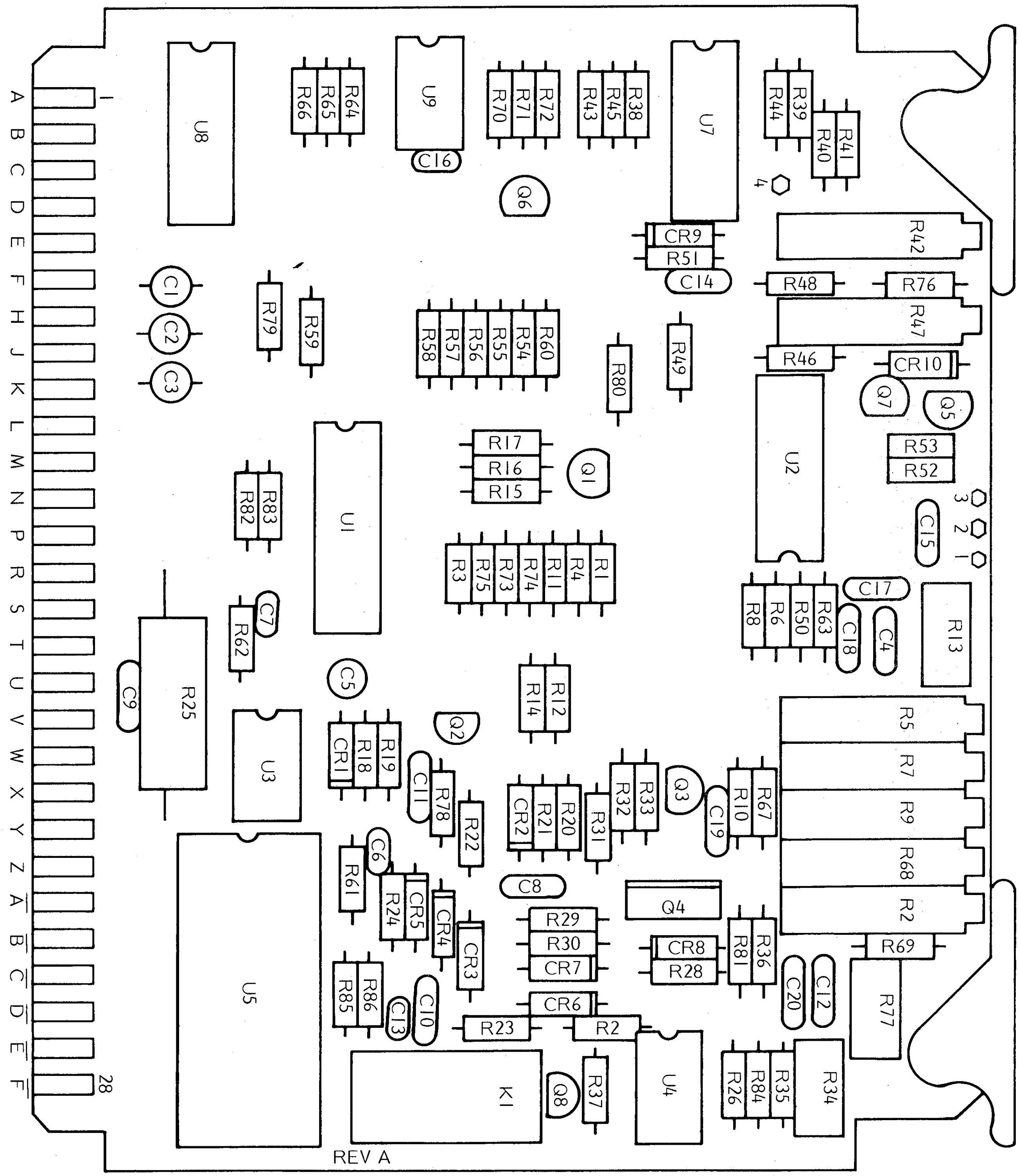
Figure 7-80. A8 YIG Driver PCB, Assy 660-D-8009-10, -13, Schematic (Sheet 1 of 3)

parts locator



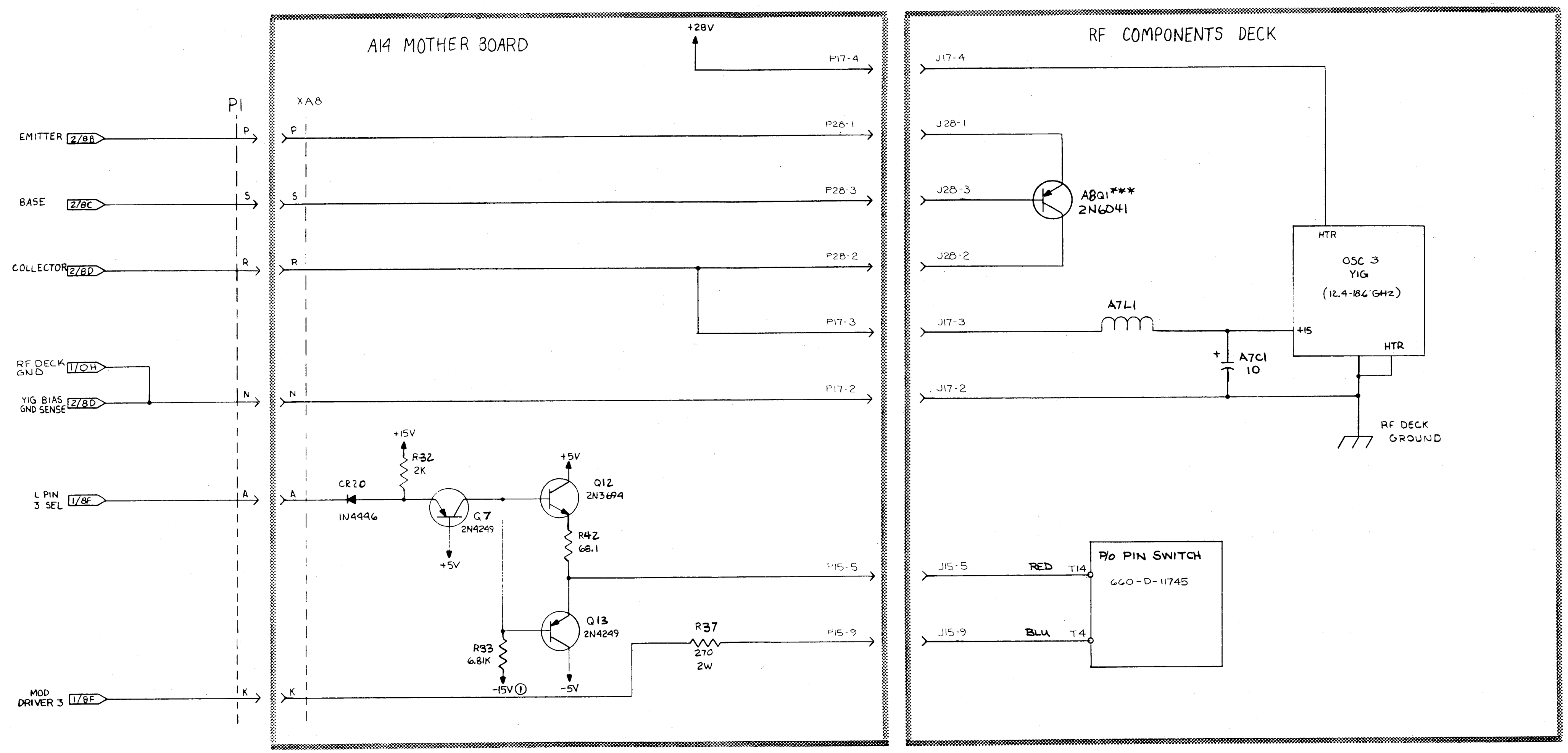
OSC. MFR.	P.C. ASSY.	R11	R14	R62	R67	R40	R41	R46	R47	R55-58	R59	R25	J1	R61	J2	J3
AVANTEK 8009 - 10	660-D-8009-10	6.19K	1.78K	NOT USED	825	N/R	N/R	9.53K	1K	6.19Ω	6.19Ω	2Ω	C-B	100K	IN-STALL	NOT USED
WJ 8009 -13	660-D-8009-13	6.81K	1.87K	NOT USED	825	N/R	N/R	9.53K	1K	6.19Ω	6.19Ω	2Ω	C-B	100K	IN-STALL	NOT USED

Figure 7-80. A8 YIG Driver PCB, Assy 660-D-8009-10, -13, Schematic (Sheet 2 of 3)



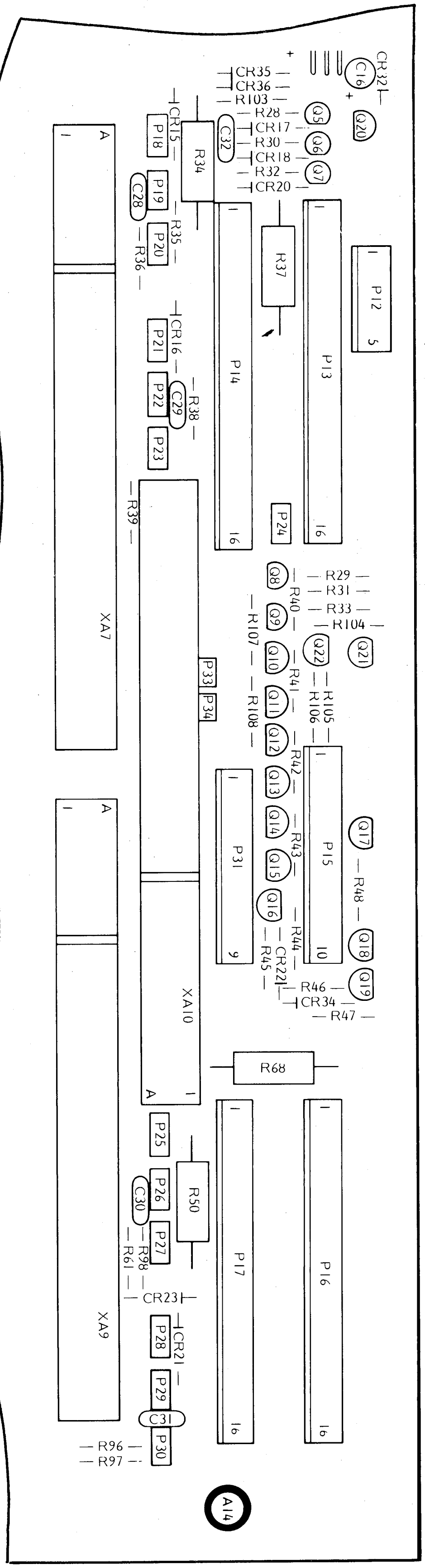
A7/A8 PCB Parts Locator Diagram

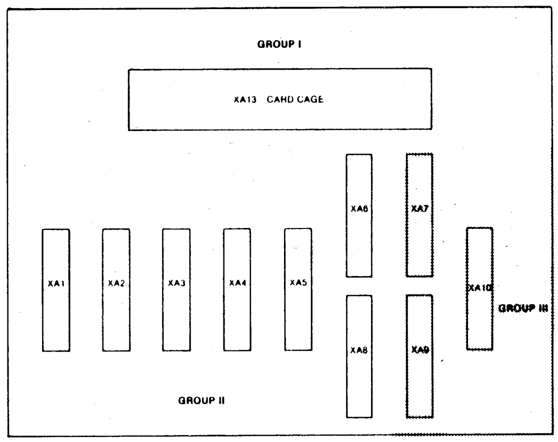
Figure 7-80
(Sheet 2 of 3)



REV.	C.O. NO.	DR. BY DATE:	APPD. BY: DATE:
SEE SHEET 1			

Figure 7-80. A8 YIG Driver PCB, Assy 660-D-8009-10, -13, Schematic (Sheet 3 of 3)





Osc 2 and Osc 3 YIG, PIN Drive, and PIN Modulator Parts Locator Diagram

Figure 7-80 (Sheet 3 of 3)

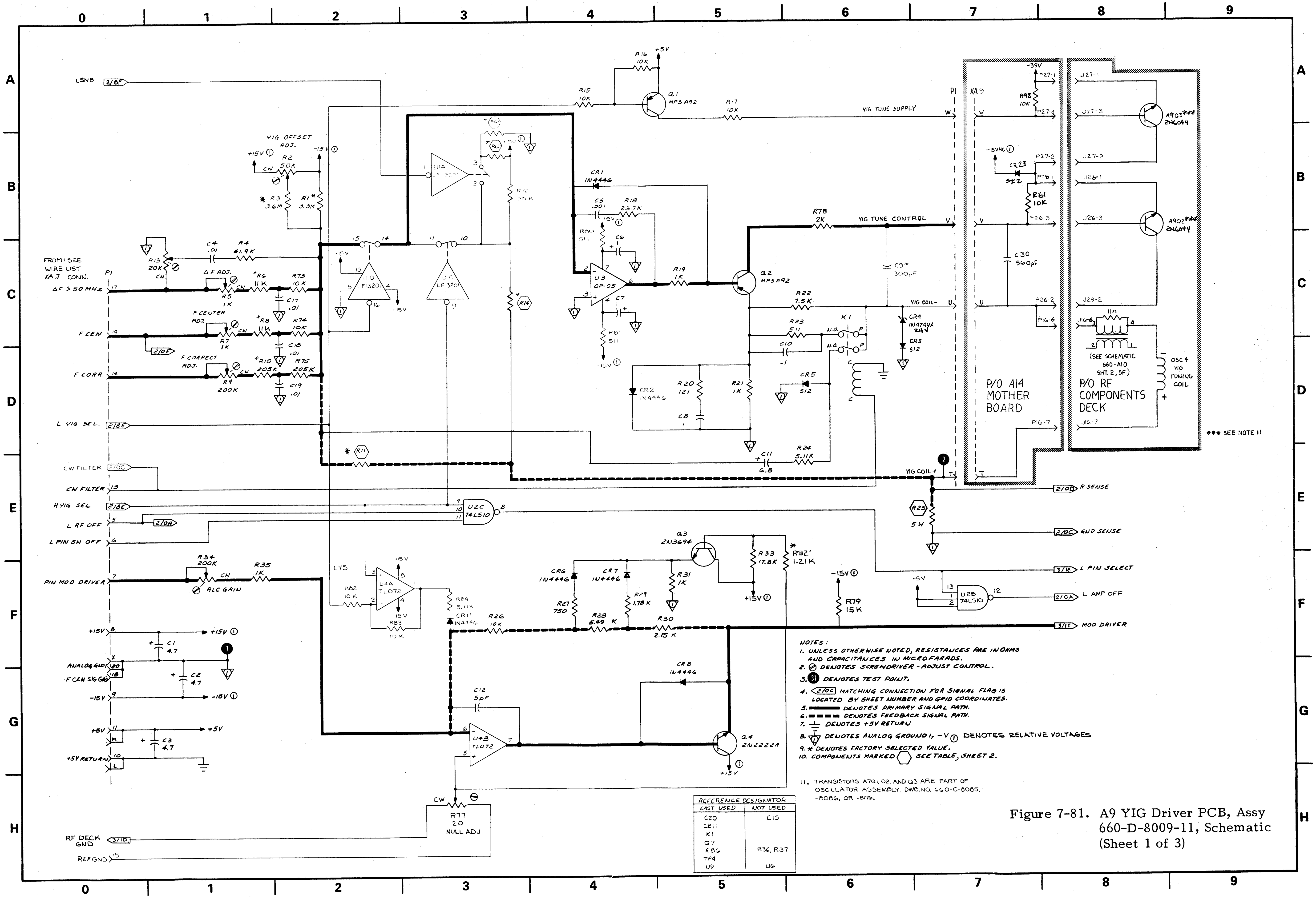
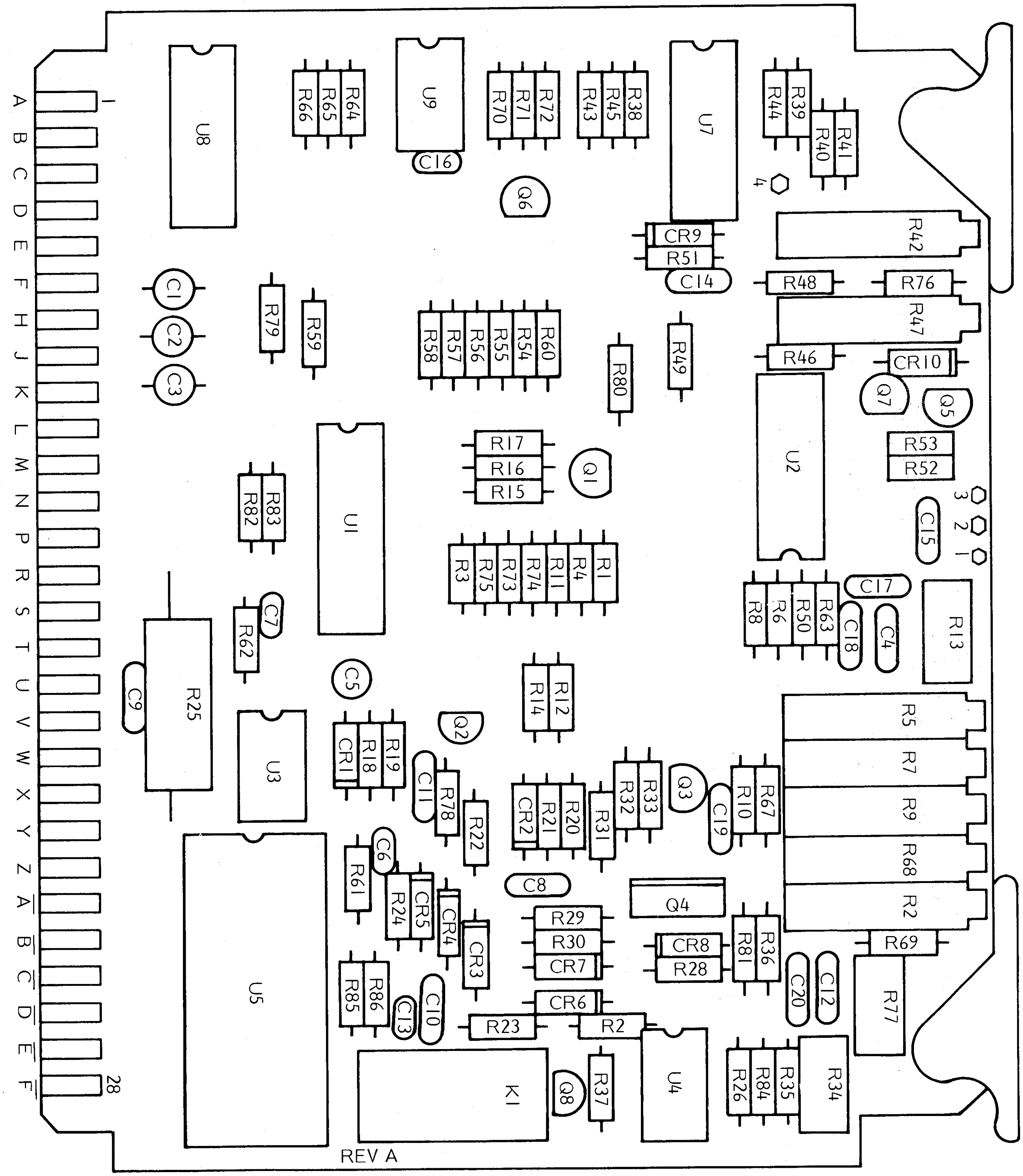
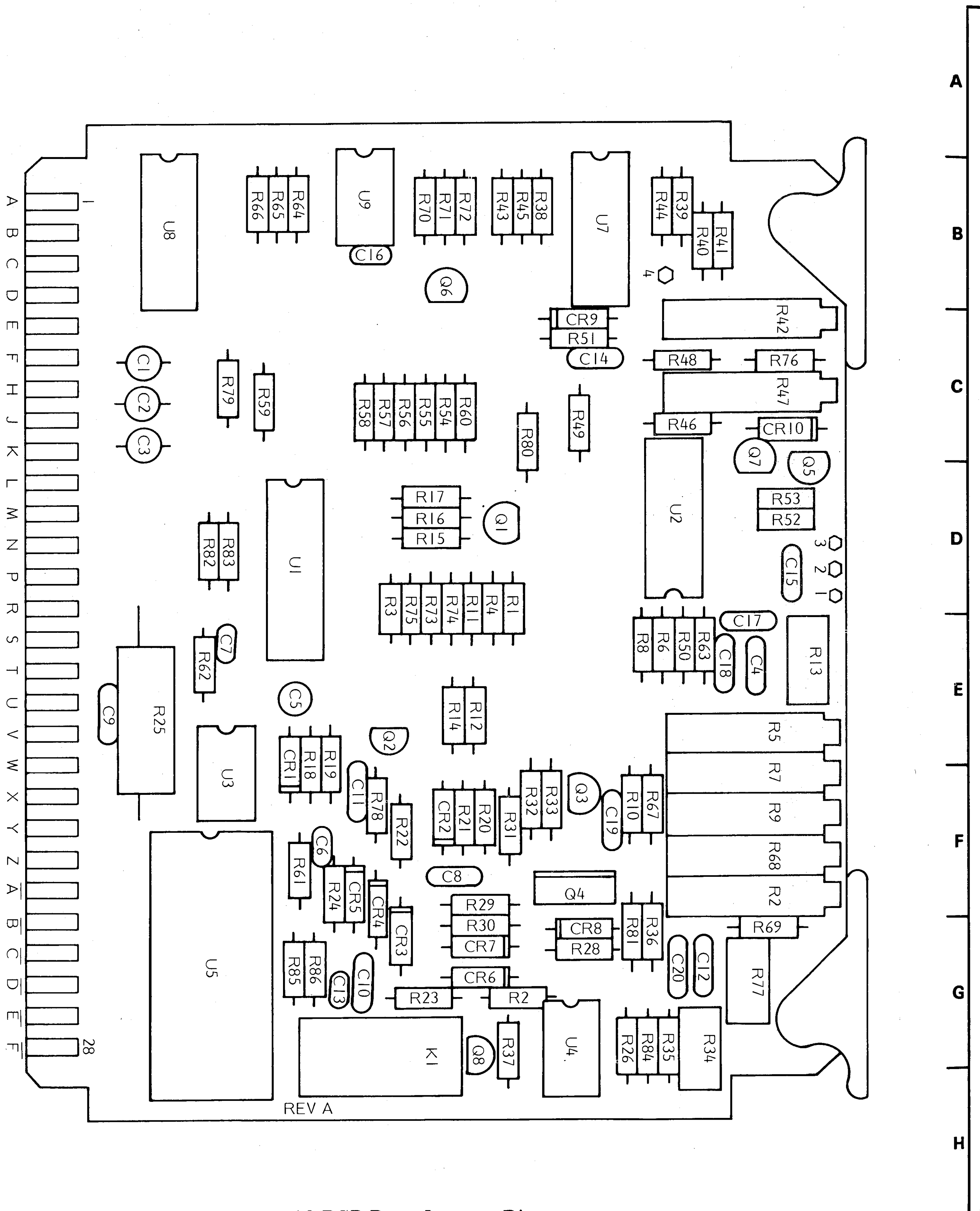


Figure 7-81. A9 YIG Driver PCB, Assy 660-D-8009-11, Schematic (Sheet 1 of 3)

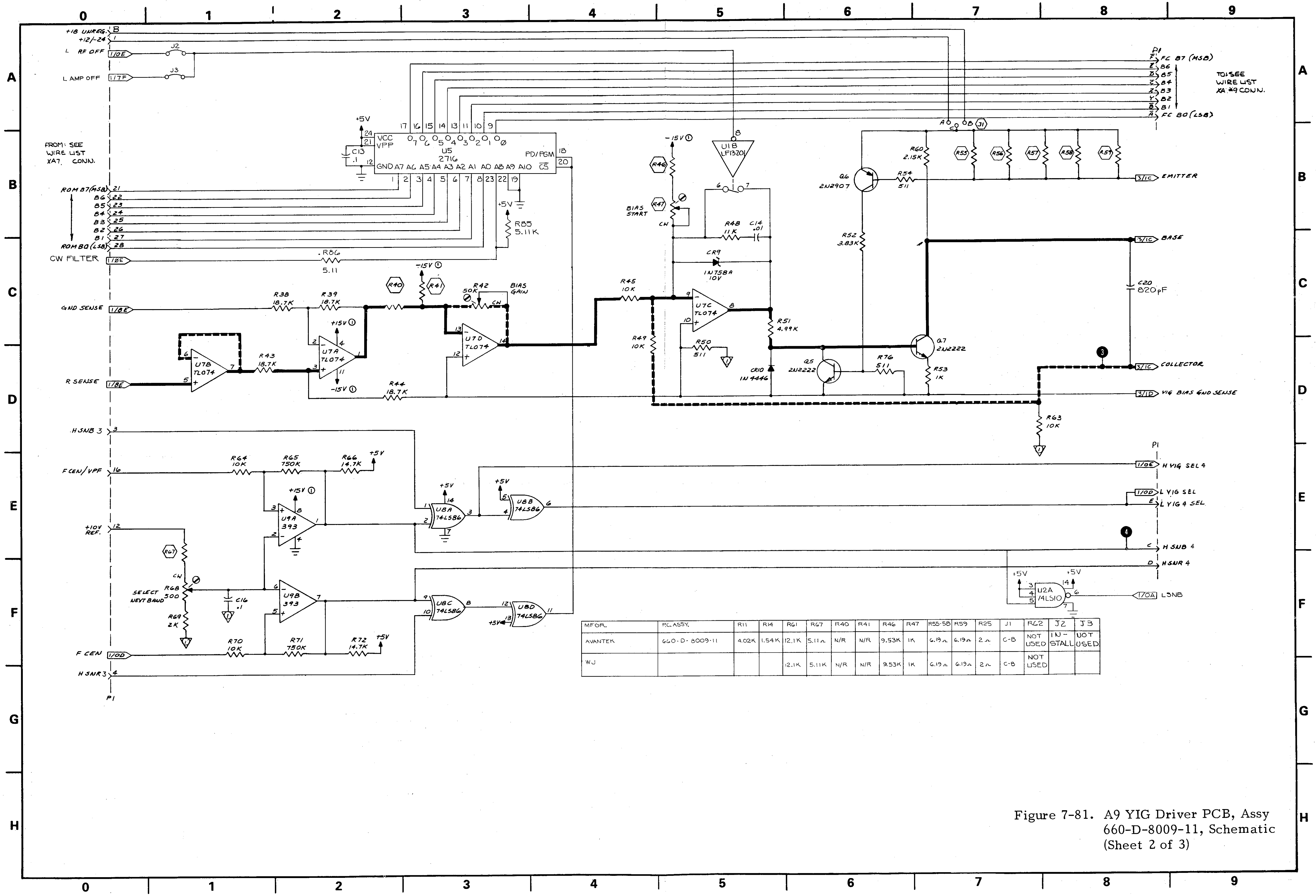


A9 PCB Parts Locator Diagram

Figure 7-81
(Sheet 1 of 3)



A9 PCB Parts Locator Diagram



MFGR.	P.C. ASSY.	R11	R14	R61	R67	R40	R41	R46	R47	R55-58	R59	R25	J1	R62	J2	J3
AVANTEK	660-D-8009-11	4.02K	1.54K	12.1K	5.11Ω	N/R	N/R	9.53K	1K	6.19Ω	6.19Ω	2Ω	C-B	NOT USED	IN-STALL	NOT USED
WJ				12.1K	5.11K	N/R	N/R	9.53K	1K	6.19Ω	6.19Ω	2Ω	C-B	NOT USED		

Figure 7-81. A9 YIG Driver PCB, Assy 660-D-8009-11, Schematic (Sheet 2 of 3)

parts locator

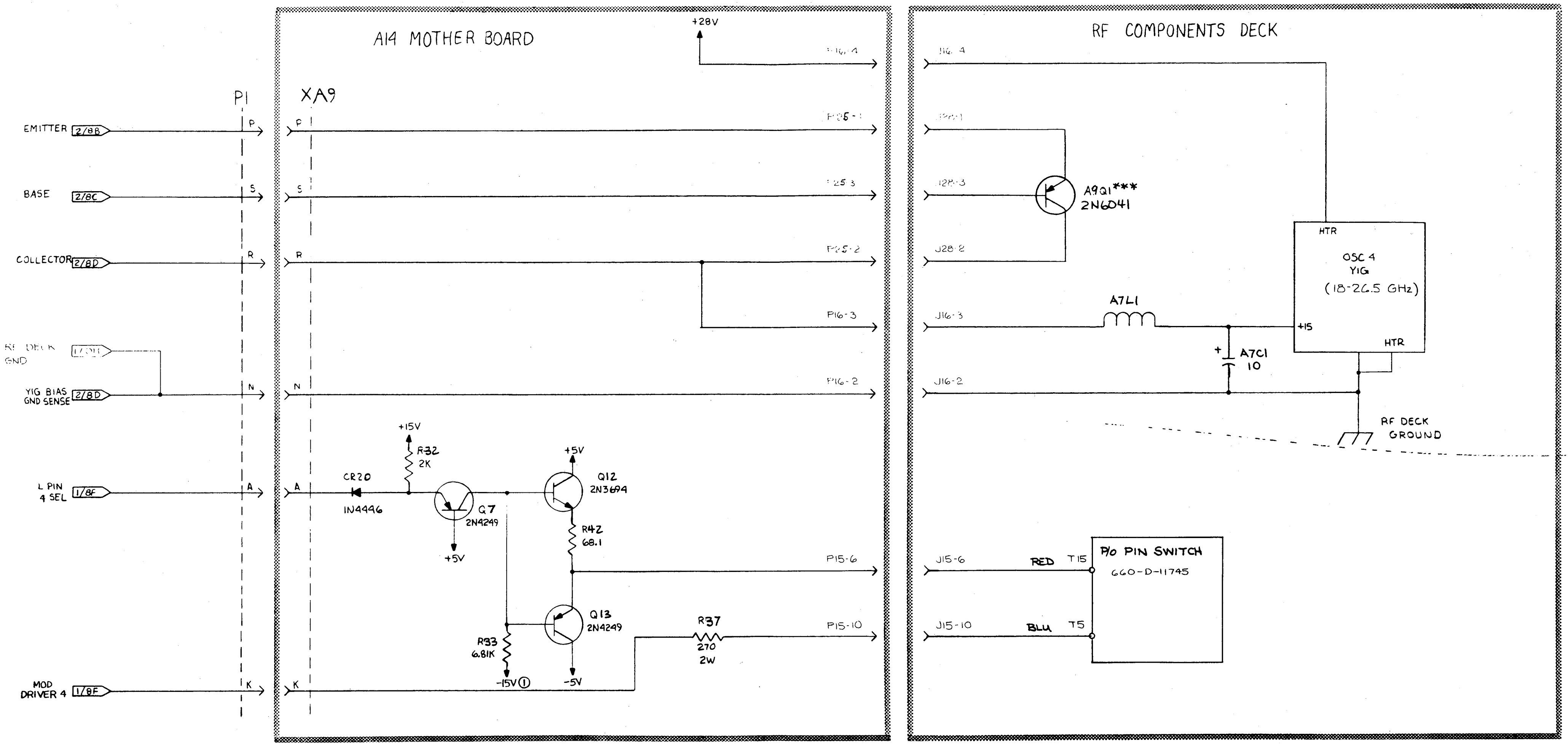
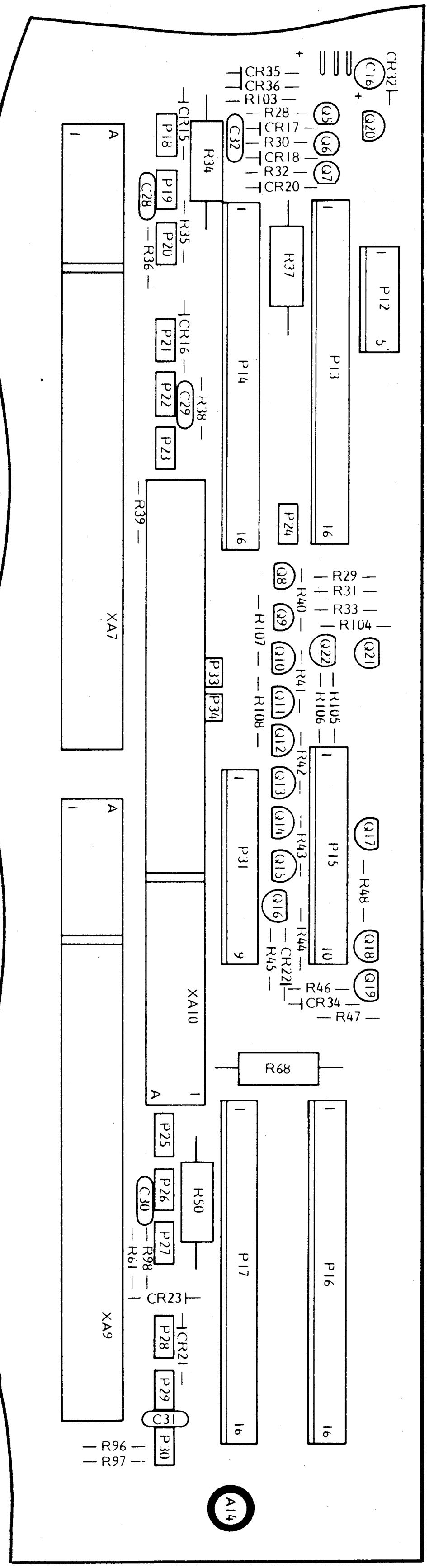


Figure 7-81. A9 YIG Driver PCB, Assy 660-D-8009-11, Schematic (Sheet 3 of 3)



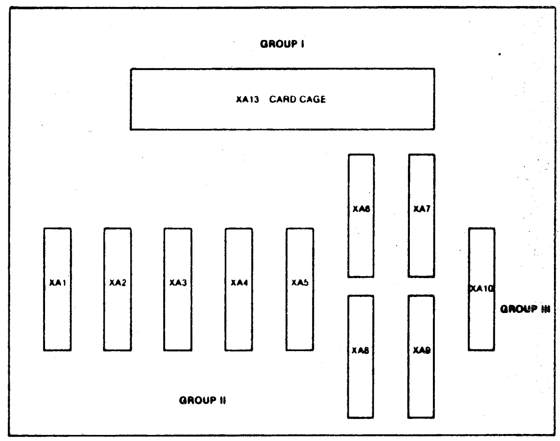
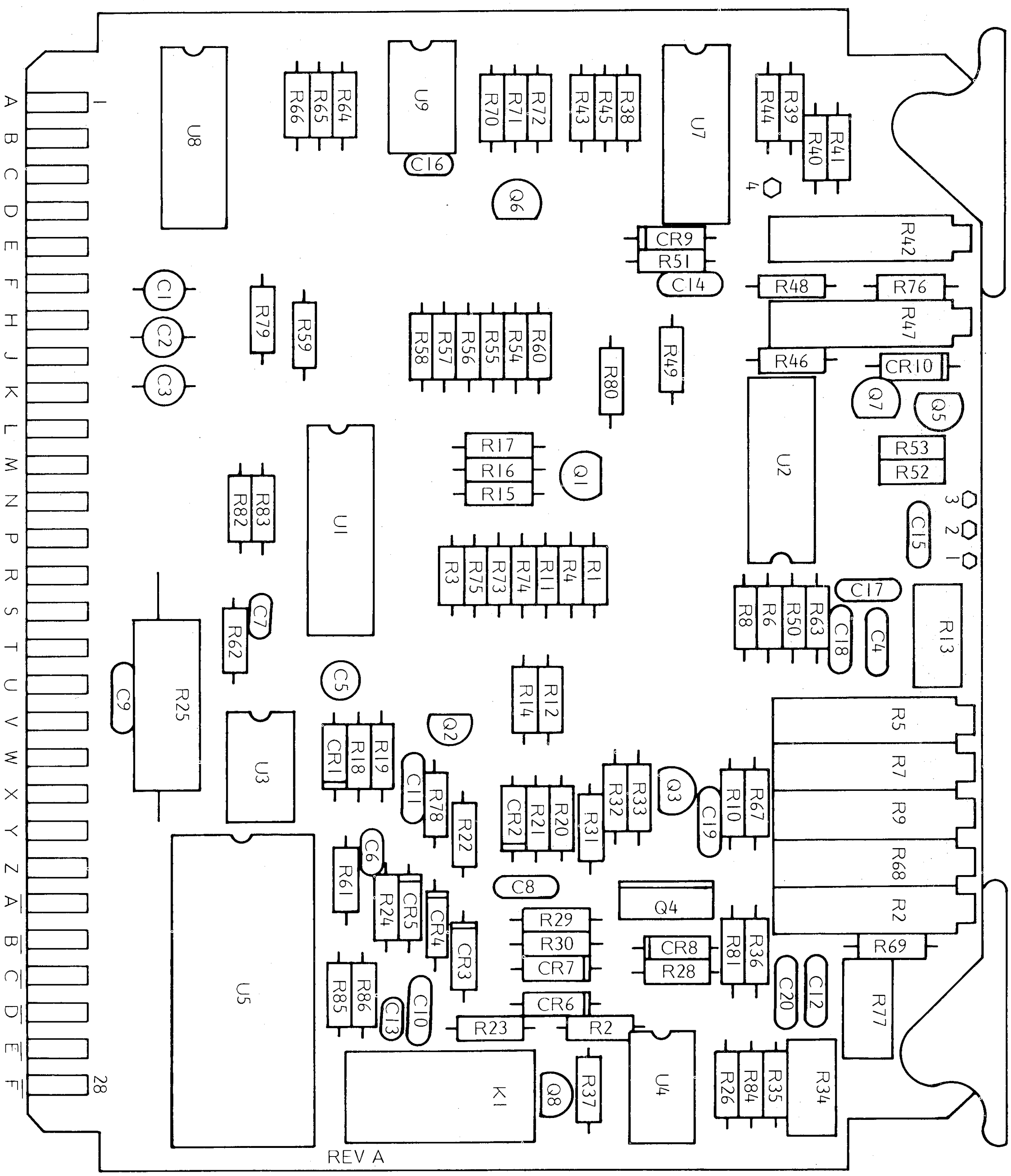
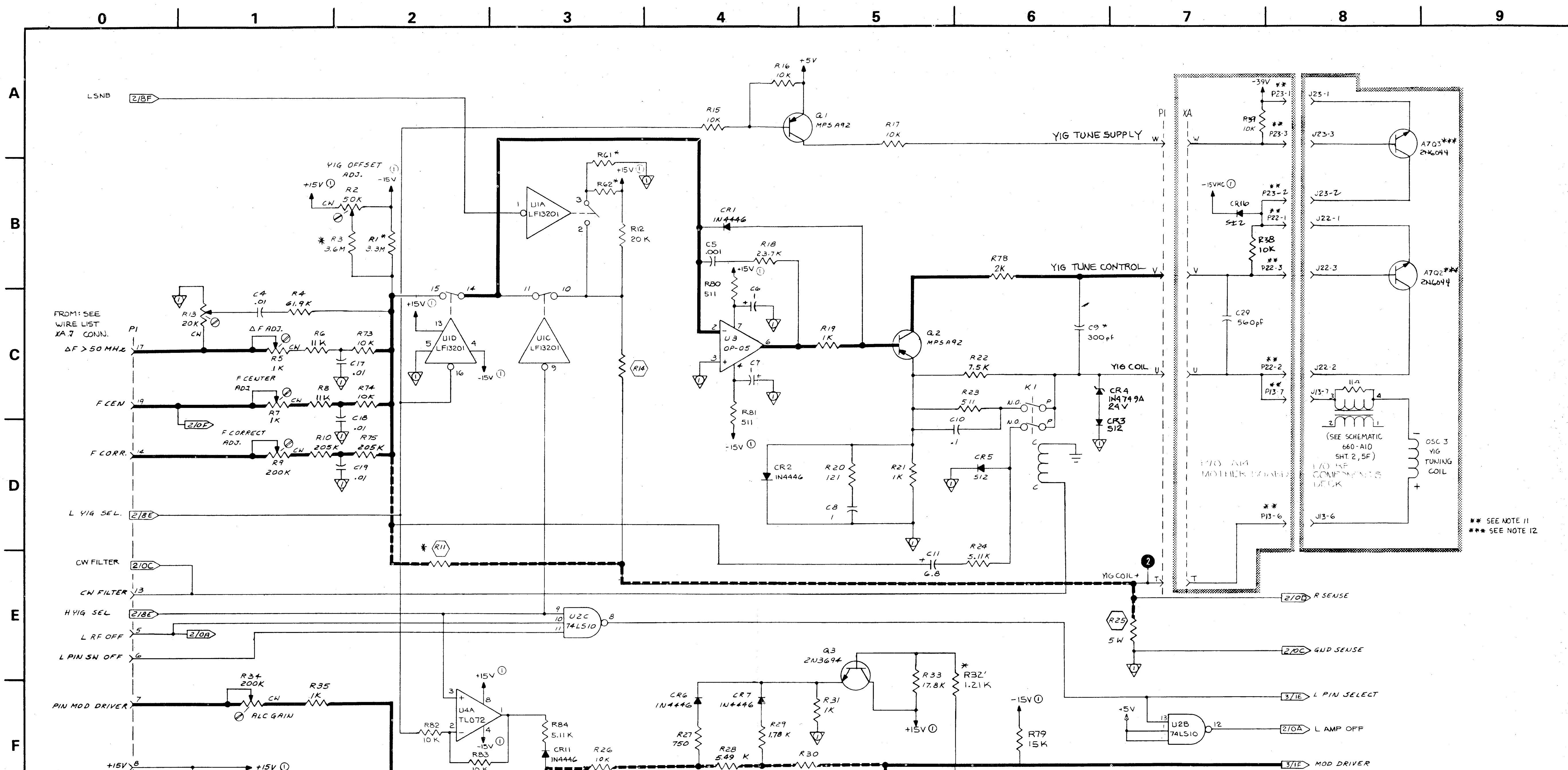


Figure 7-81
(Sheet 3 of 3)



A7/A8 PCB Parts Locator Diagram



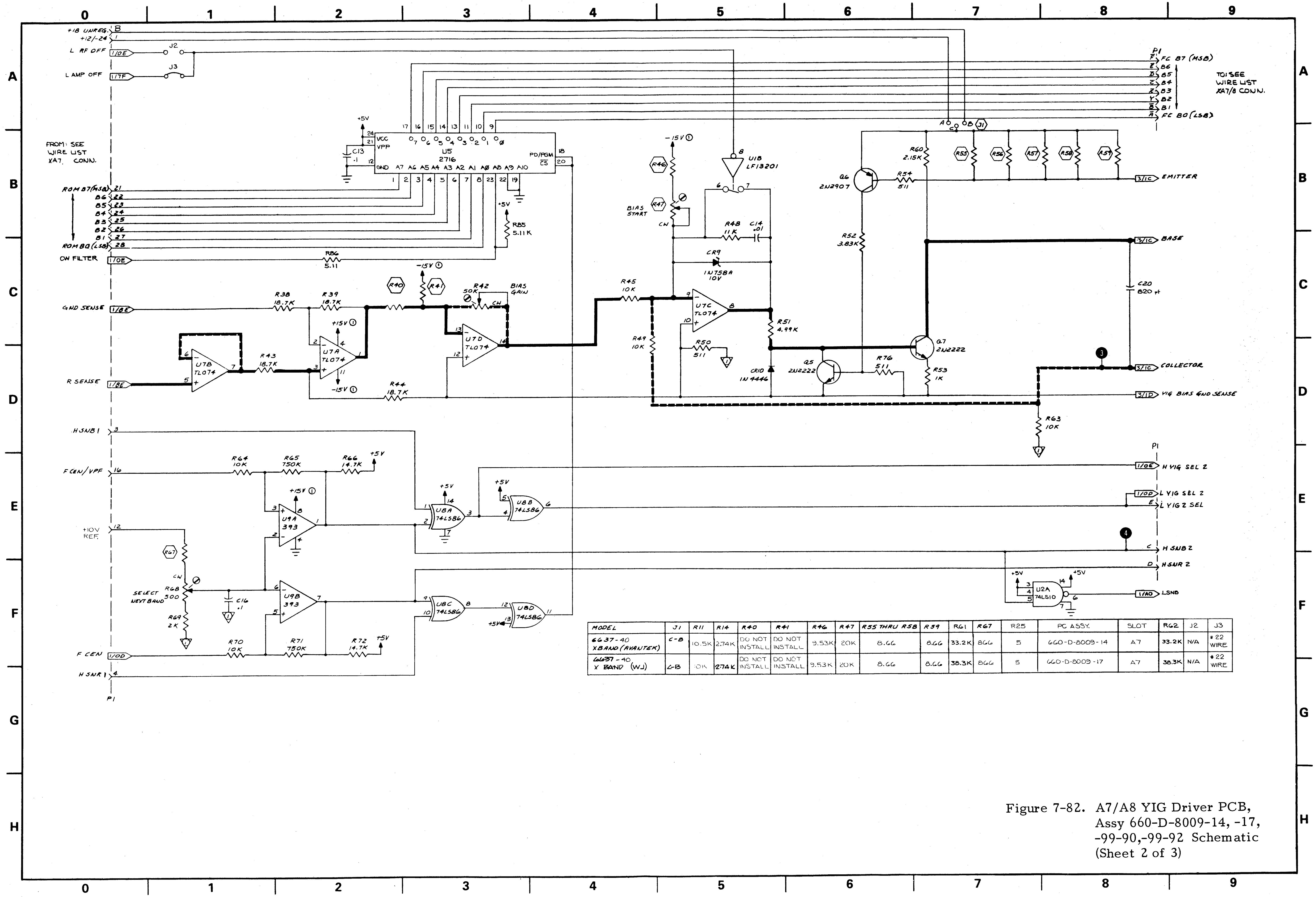
NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. ⊘ DENOTES SCREWDRIVER-ADJUST CONTROL.
3. ❸❶ DENOTES TEST POINT.
4. <2/0C] MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ▬▬▬ DENOTES PRIMARY SIGNAL PATH.
6. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.
7. ⏚ DENOTES +5V RETURN
8. ▽ DENOTES ANALOG GROUND 1, −V ① DENOTES RELATIVE VOLTAGES
9. * DENOTES FACTORY SELECTED VALUE.
10. COMPONENTS MARKED ⬡ SEE TABLE, SHEET 2.
11. ASSUMES PCB IS INSTALLED IN A7 SLOT.
12. TRANSISTORS A7Q1, Q2, AND Q3 ARE PART OF OSCILLATOR ASSEMBLY, DWG NO 660-C-8085, -8086, OR -8176.
13. USED ONLY ON WILTRON PART NUMBER 60-16.
14. /// DENOTES RF DECK GROUND

REFERENCE DESIGNATOR	
LAST USED	NOT USED
C20	C15
CR11	U6
K1	
Q7	
R86	
TP4	
U9	

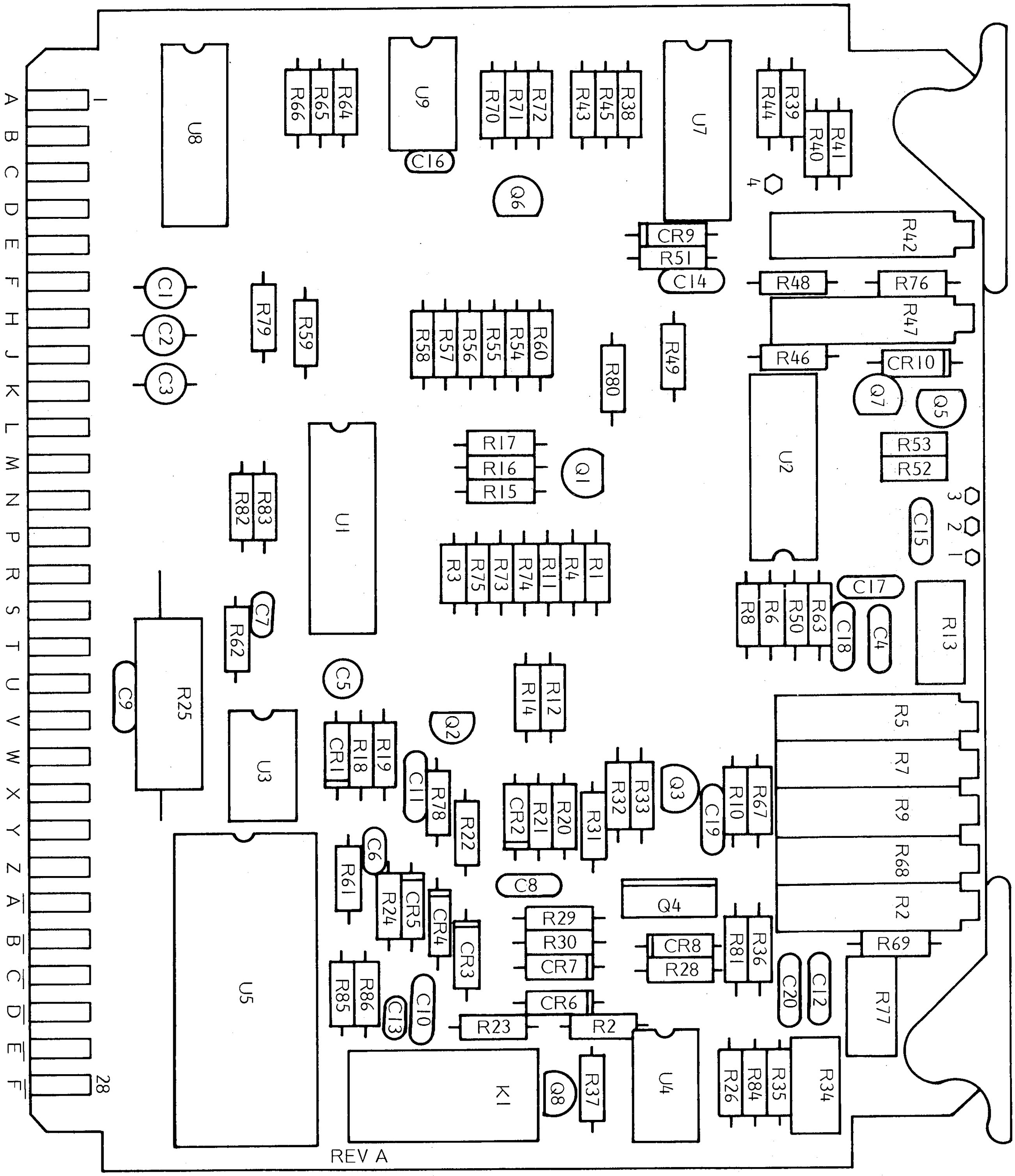
Figure 7-82. A7/A8 YIG Driver PCB, Assy 660-D-8009-14, -17, -99-90, -99-92 Schematic (Sheet 1 of 3)

parts locator



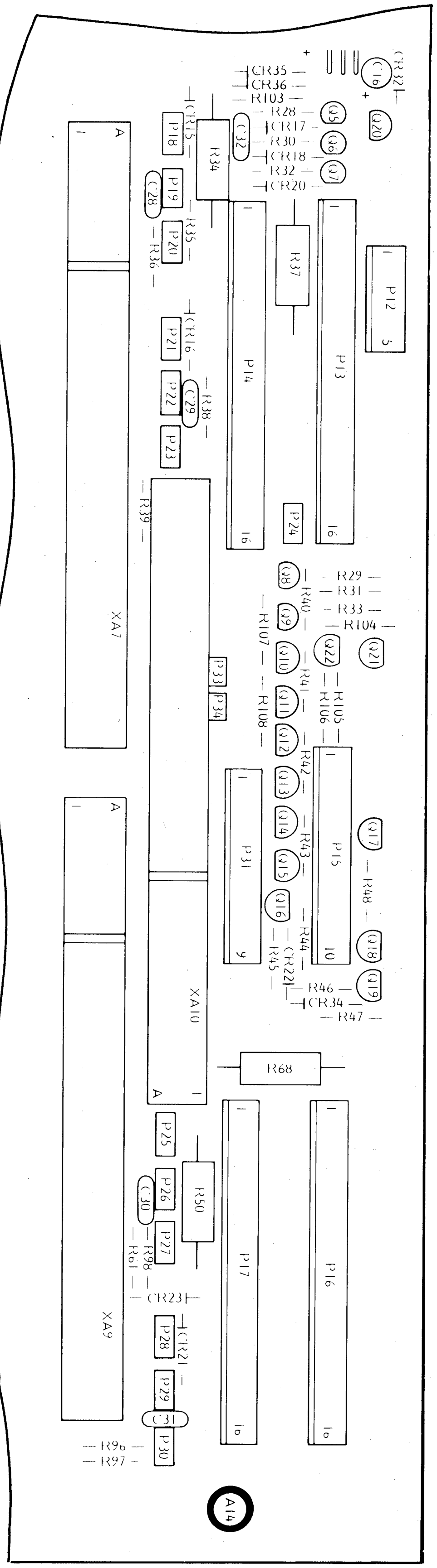
MODEL	J1	R11	R14	R40	R41	R46	R47	R55 THRU R58	R59	R61	R67	R25	PC ASSY.	SLOT	R62	J2	J3
6637-40 XBAND (AVANTEK)	C-B	10.5K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	20K	8.66	8.66	33.2K	866	5	660-D-8009-14	A7	33.2K	N/A	#22 WIRE
6637-40 X BAND (WJ)	C-B	10K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	20K	8.66	8.66	38.3K	866	5	660-D-8009-17	A7	38.3K	N/A	#22 WIRE

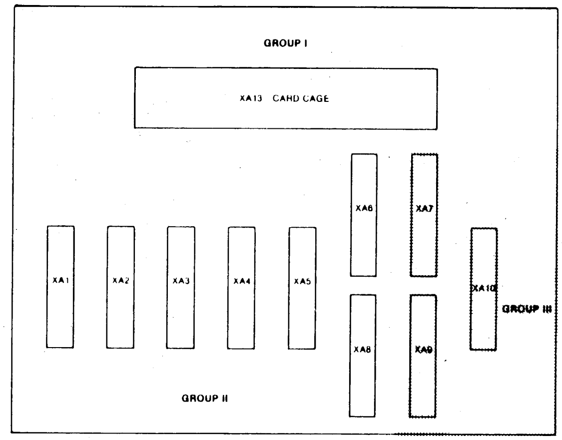
Figure 7-82. A7/A8 YIG Driver PCB, Assy 660-D-8009-14, -17, -99-90,-99-92 Schematic (Sheet 2 of 3)



A7/A8 PCB Parts Locator Diagram

Figure 7-82
(Sheet 2 of 3)





Osc 2 and Osc 3 YIG, PIN Driver, and PIN Modulator Parts Locator Diagram

A
B
C
D
E
F
G
H

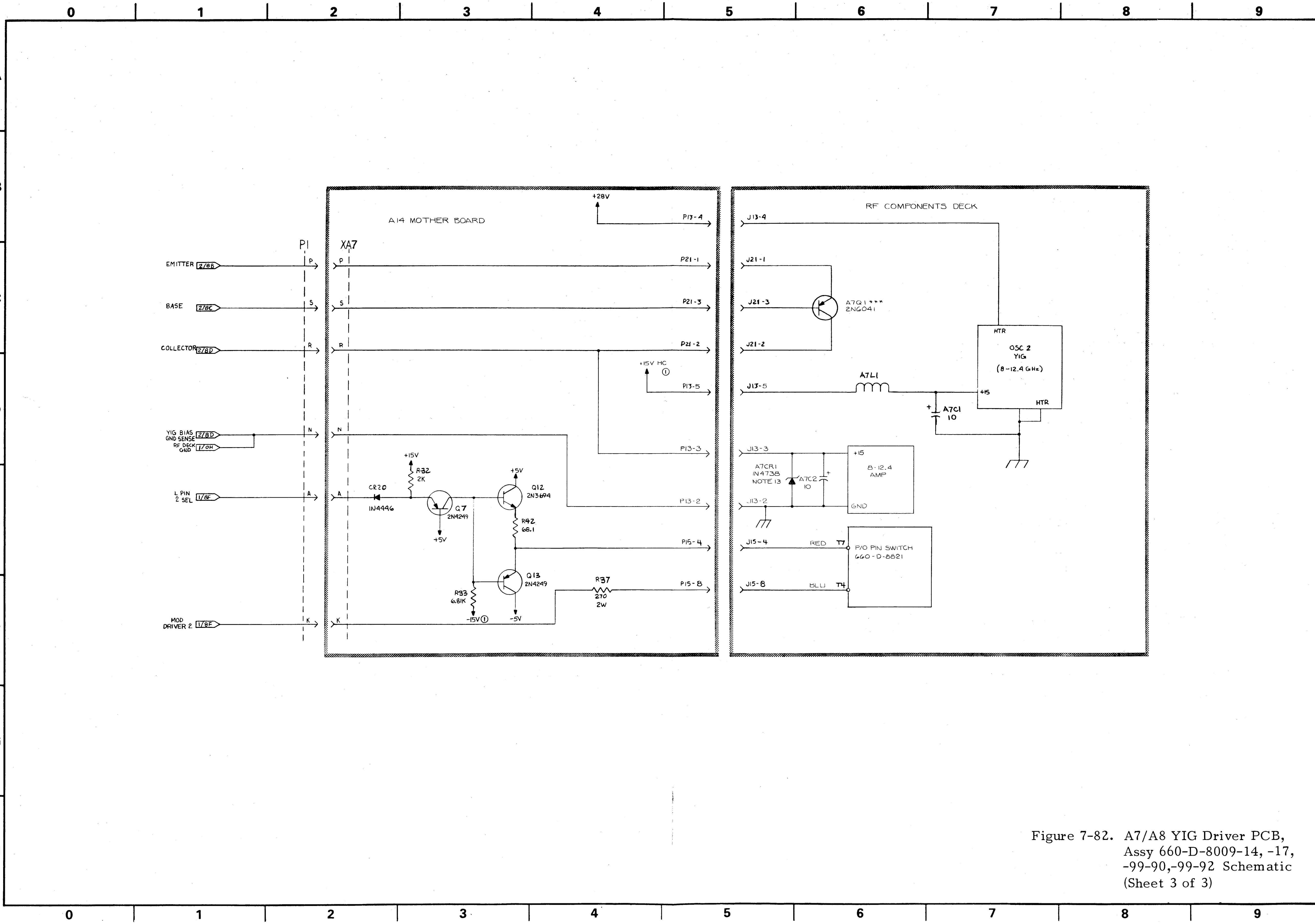


Figure 7-82. A7/A8 YIG Driver PCB, Assy 660-D-8009-14, -17, -99-90,-99-92 Schematic (Sheet 3 of 3)

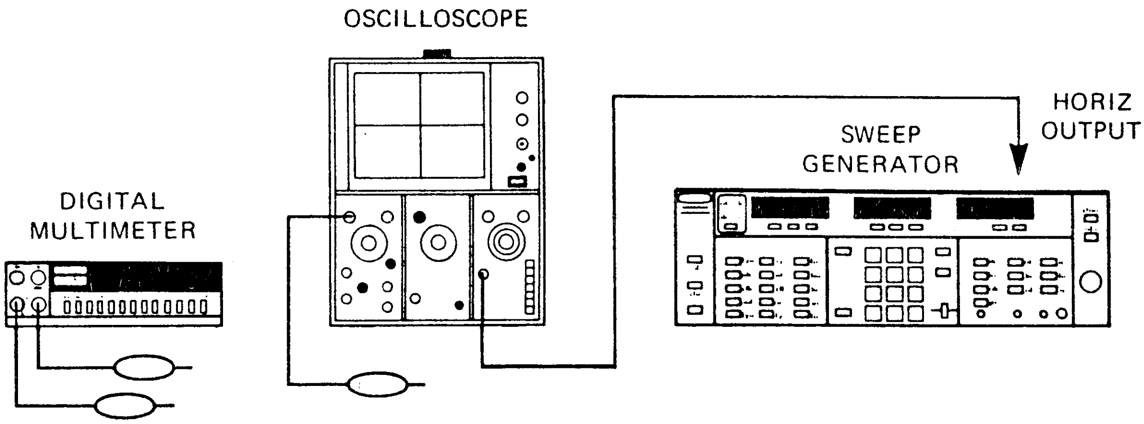
7-12.8 A5 Frequency Instruction and A6-A9 YIG Driver PCBs, Troubleshooting Information and Data

Except in the 6609A, error codes 09 thru 14 report on the A5 Frequency Instruction and A6-A9 YIG Driver PCBs. The microprocessor routines associated with these error codes test the A5-A9 PCBs using three methods. In the first method (Error Code 09), the A5 F Center DAC is made to output mid-band frequency data in the .01 to 2 GHz HET band to the A6 PCB. The routine then monitors the **L HET YIG SEL** line for activity. If the line fails to go HIGH, indicating the completion of the Heterodyne Down Converter sweep, "Error 09" is displayed.

In the second method (Error Codes 10 through 13), the F Center DAC (U7) is made to output mid-band frequency data in each of the Osc 1 thru Osc 4 YIG bands, sequentially. At the end of each YIG-band's error-code test, a bit pattern formed by the four **YIG SEL** and **SNR** lines is applied to latch buffer A14U7 (Figure 7-84). This bit pattern is compared with test data stored in A12 PCB read-only memory (ROM). If the bit-pattern and ROM test data do not compare favorably, the appropriate error code is displayed.

In the third method (Error Code 14), both the Sweep Width (ΔF) DAC (U24) and the Step Freq DAC (U19) are tested. In this method, (1) the F Center DAC is set to mid-band; (2) the Sweep Width (ΔF) DAC is set to provide a full-band sweep; and (3) the Step Freq DAC is set to 0, then 10 volts. This Step Freq DAC operation simulates a full-band sweep. At the 10V point on this simulated sweep, the **YIG SEL/SNR** bit pattern is compared with the ROM test data. If the comparison is unfavorable, "Error 14" is displayed.

The test equipment setup for troubleshooting Error Codes 09-14 is provided in Figure 7-83; the troubleshooting flowcharts are provided in Figures 7-85 through 7-88.



SWEEP GENERATOR CONTROL SETTINGS

FREQUENCY RANGE: CW F0 (Error Codes 09 thru 13)

FULL (Error Code 14)

TRIGGER: AUTO
MARKERS: All Off
LEVELING: INTERNAL
LEVEL: 10 dB below Max. Leveled Power
SWEEP TIME: 10 ms
RETRACE RF: Off

RF ON: On
RF SLOPE: Off
F0: Applicable midband or midrange frequency

Figure 7-83. Test Equipment Setup for Troubleshooting Error Codes 09 thru 14

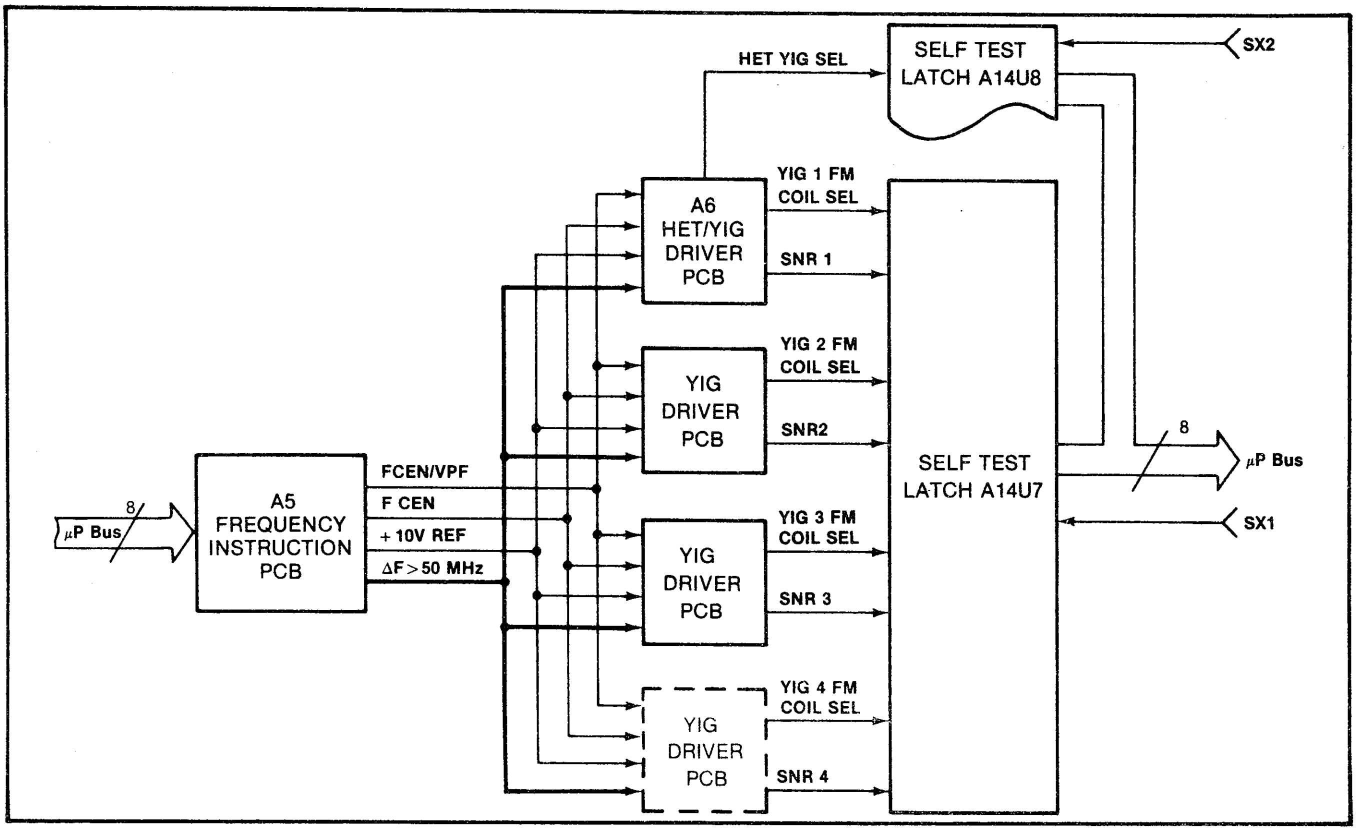
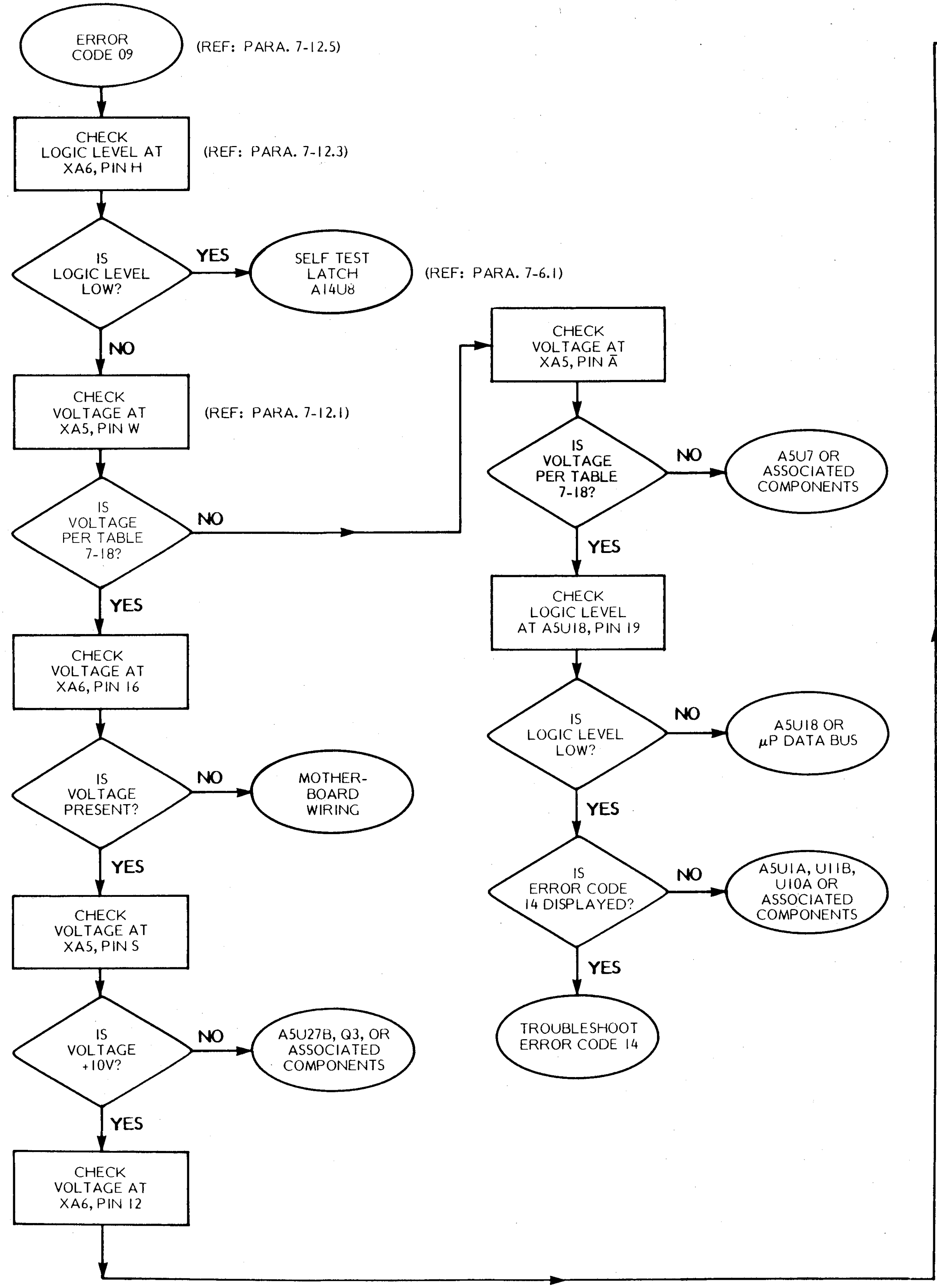
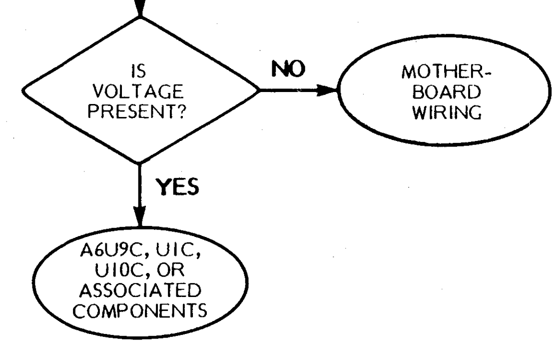


Figure 7-84. Error Codes 9 thru 14, Diagnostic (Self Test) Circuit

Table 7-18. F Center DAC Voltages (Formula: VDAC = $(10/F_{High\ End}) \times (F_{Desired})$

MODEL	1 GHz	5 GHz	10 GHz	15 GHz	22 GHz	33 GHz
6609A	5.000V					
6617A	1.250V	6.250V				
6621A/6621A-40		4.032V	8.065V			
6629A/6629A-40			5.376V	8.065V		
6637A/6637A-40		2.688V	5.376V	8.065V		
6638A		2.500V	5.000V	7.500V		
6642A					5.500V	8.250V
6647A	0.538V	2.688V	5.376V	8.065V		
6648A	0.500V	2.500V	5.000V	7.500V		
6653A		1.887V	3.774V	5.660V	8.302V	
6659A	0.377V	1.887V	3.774V	5.660V	8.302V	





GENERAL INSTRUCTIONS FOR FIGURE 7-85 THRU 7-88 FLOWCHARTS

1. Before starting any of the flowcharts, check the following dc voltages at applicable PCB edge connector P1.

   a. +15V, pins 8 (+) and 20 (-).

   b. -15V, pins 9 (-) and 20 (+).

   C. +10V, pins 12 (+) and 20 (-).

   d. +5V, pins 11 (+) and 10 (-).

2. Logic levels are TTL.

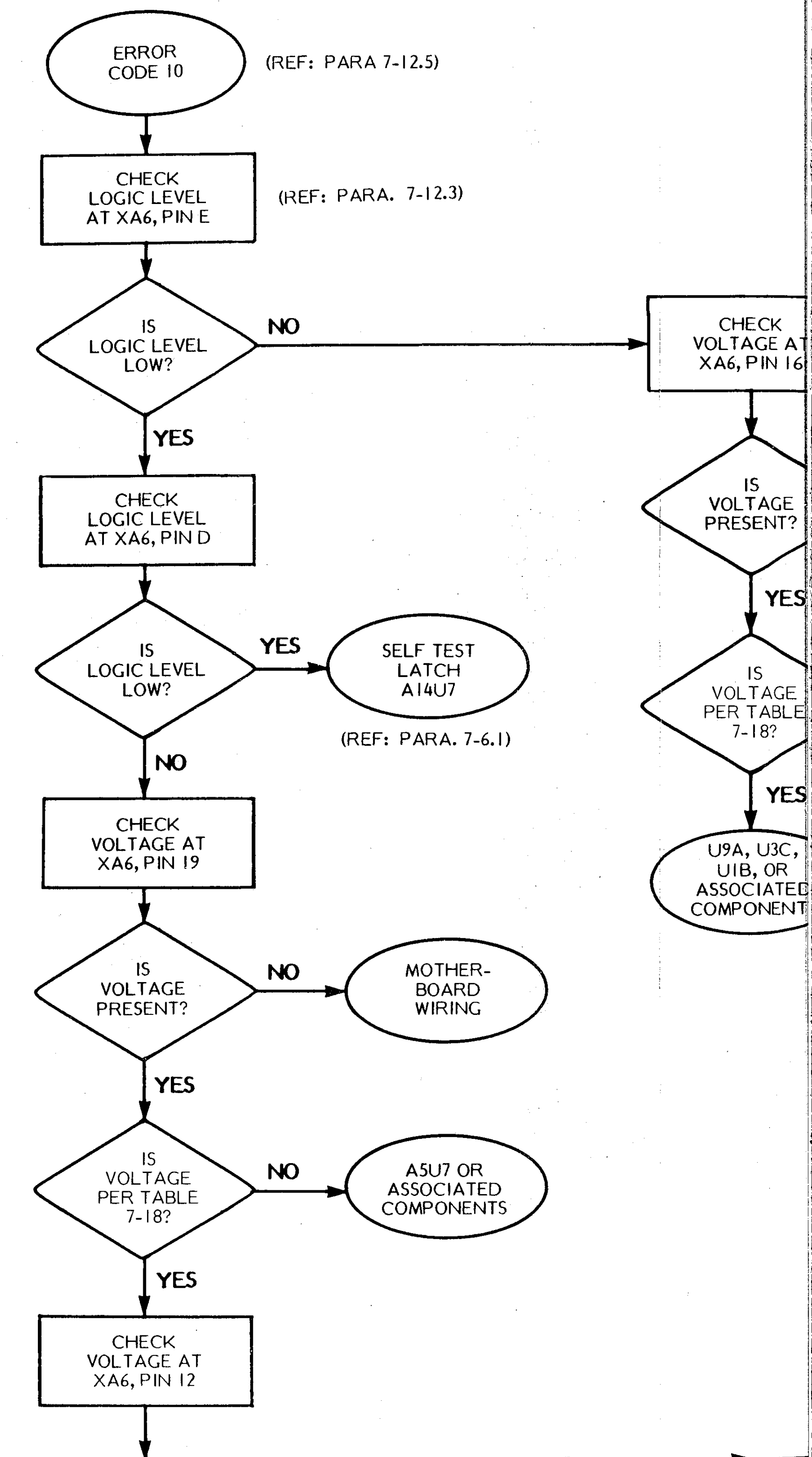
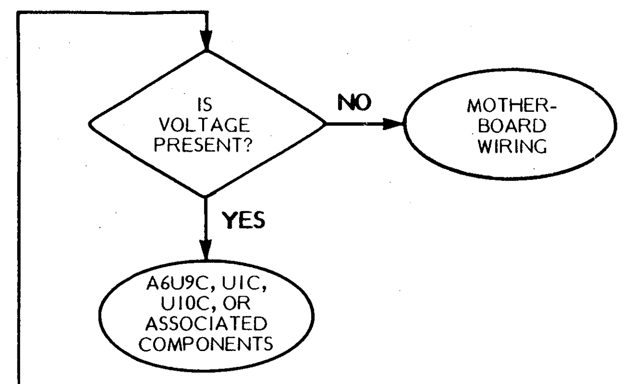


Figure 7-85. Error Code 09 Troubleshooting Flowchart



GENERAL INSTRUCTIONS FOR FIGURE 7-85 THRU 7-88 FLOWCHARTS

1. Before starting any of the flowcharts, check the following dc voltages at applicable PCB edge connector P1.
   a. +15V, pins 8 (+) and 20 (-).
   b. -15V, pins 9 (-) and 20 (+).
   C. +10V, pins 12 (+) and 20 (-).
   d. +5V, pins 11 (+) and 10 (-).
2. Logic levels are TTL.

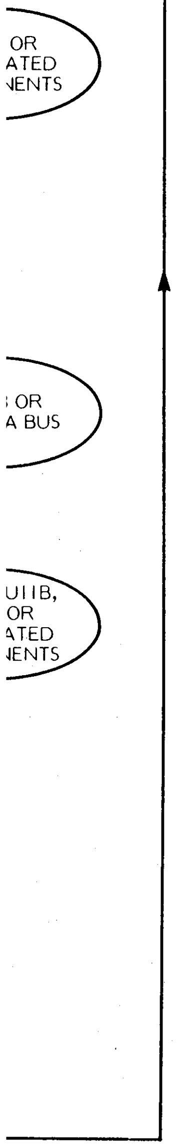


Figure 7-85. Error Code 09 Troubleshooting Flowchart

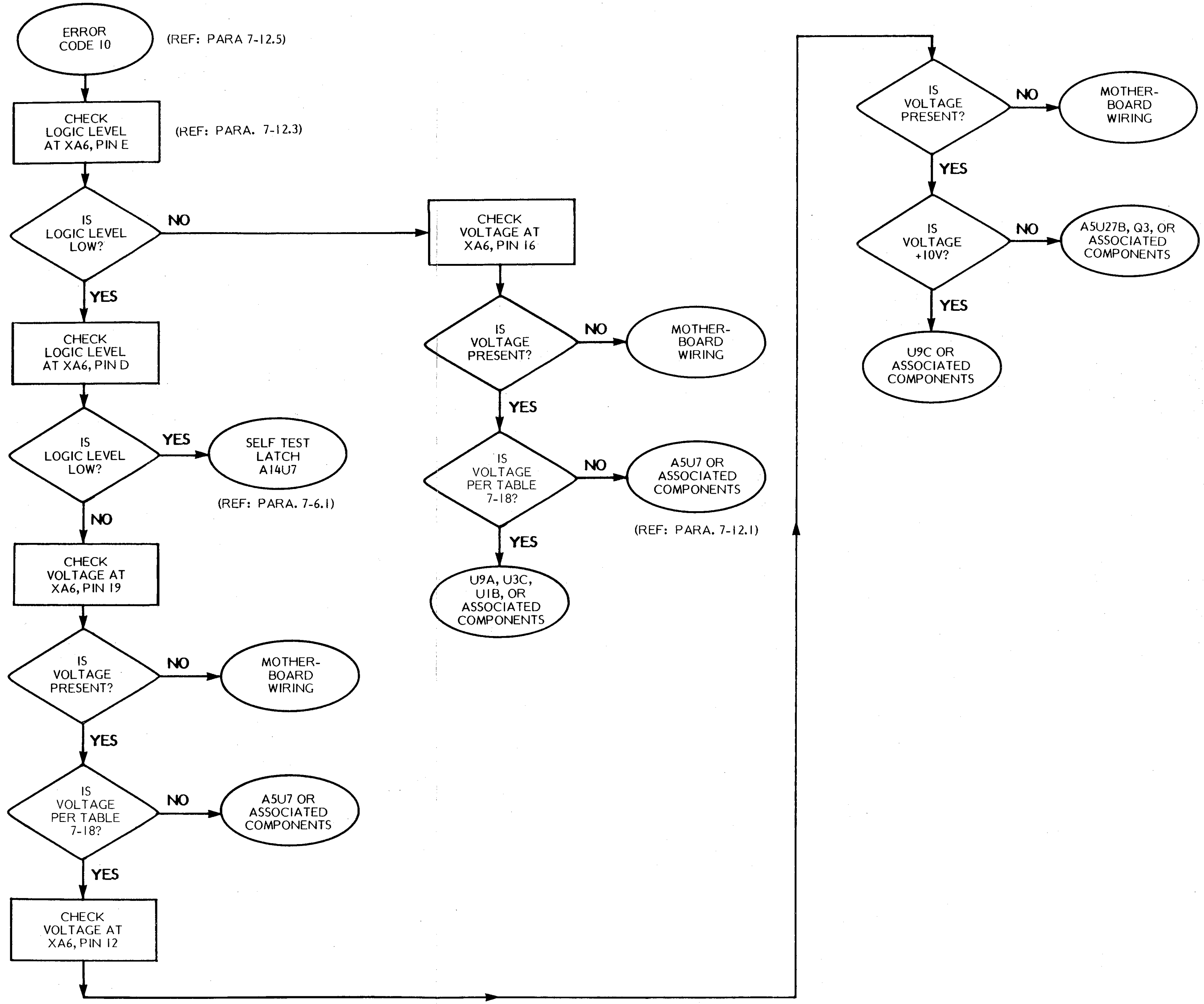


Figure 7-86. Error Code 10 Troubleshooting Flowchart

Figure 7-85

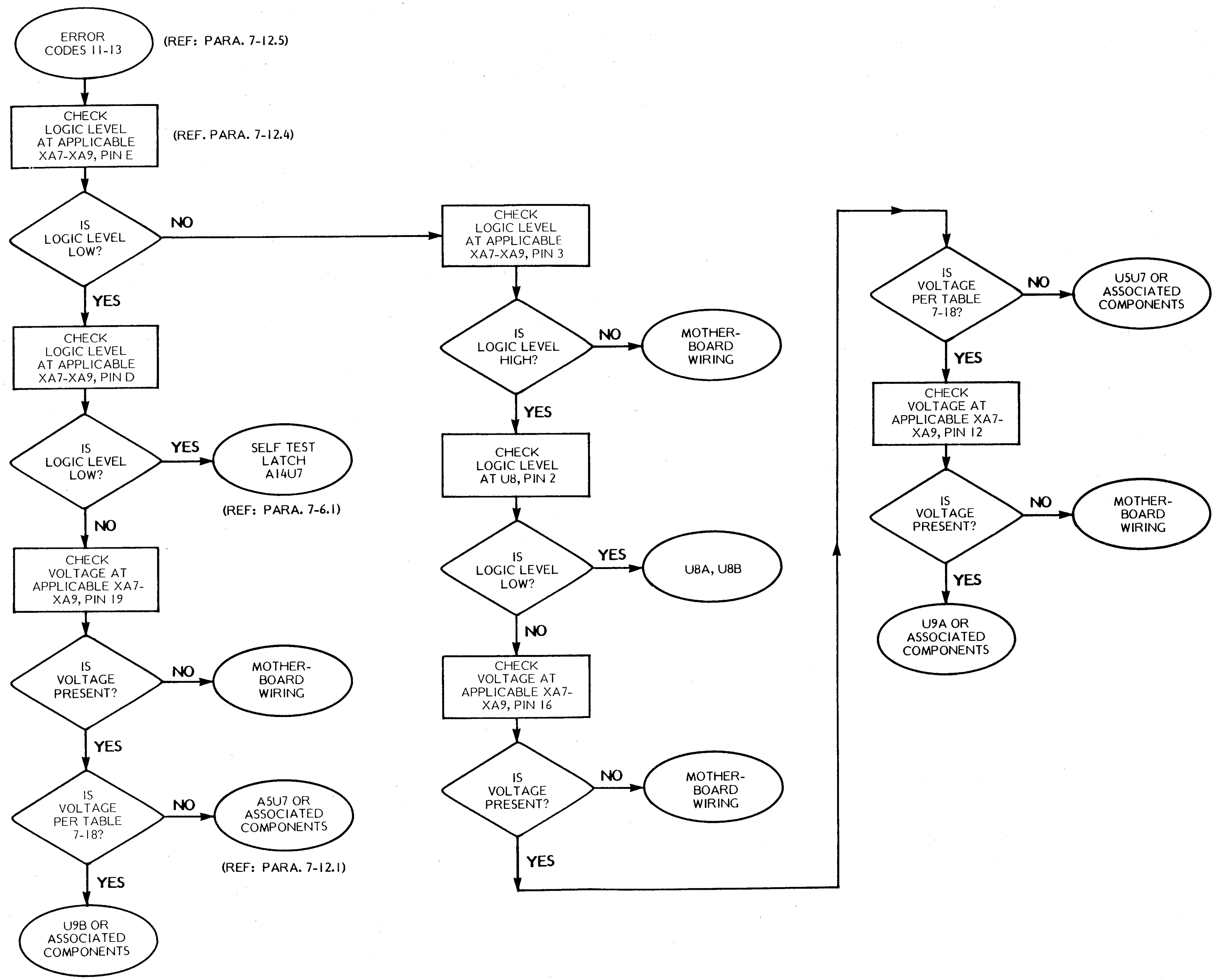


Figure 7-87. Error Code 11 Troubleshooting Flowchart

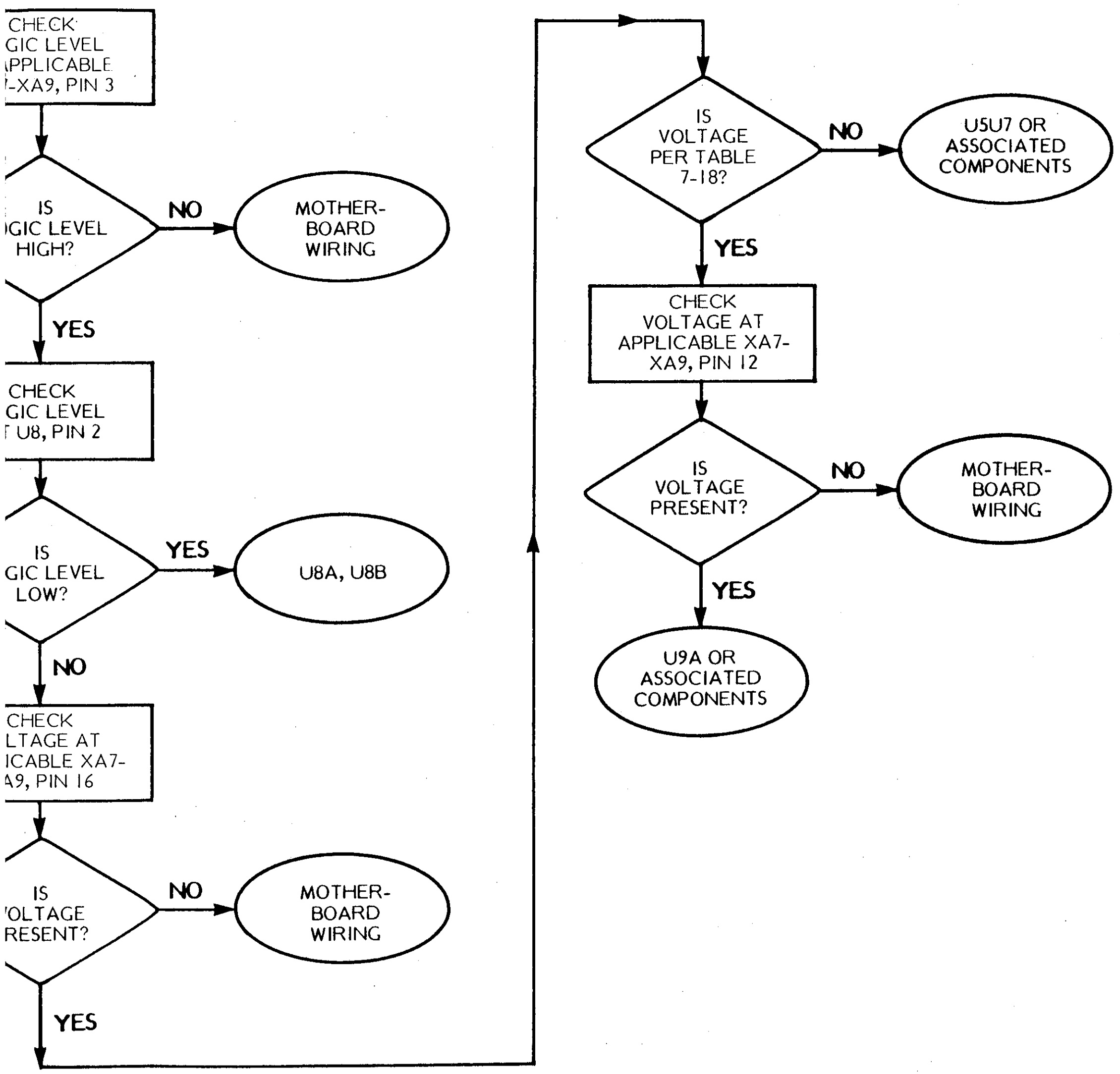
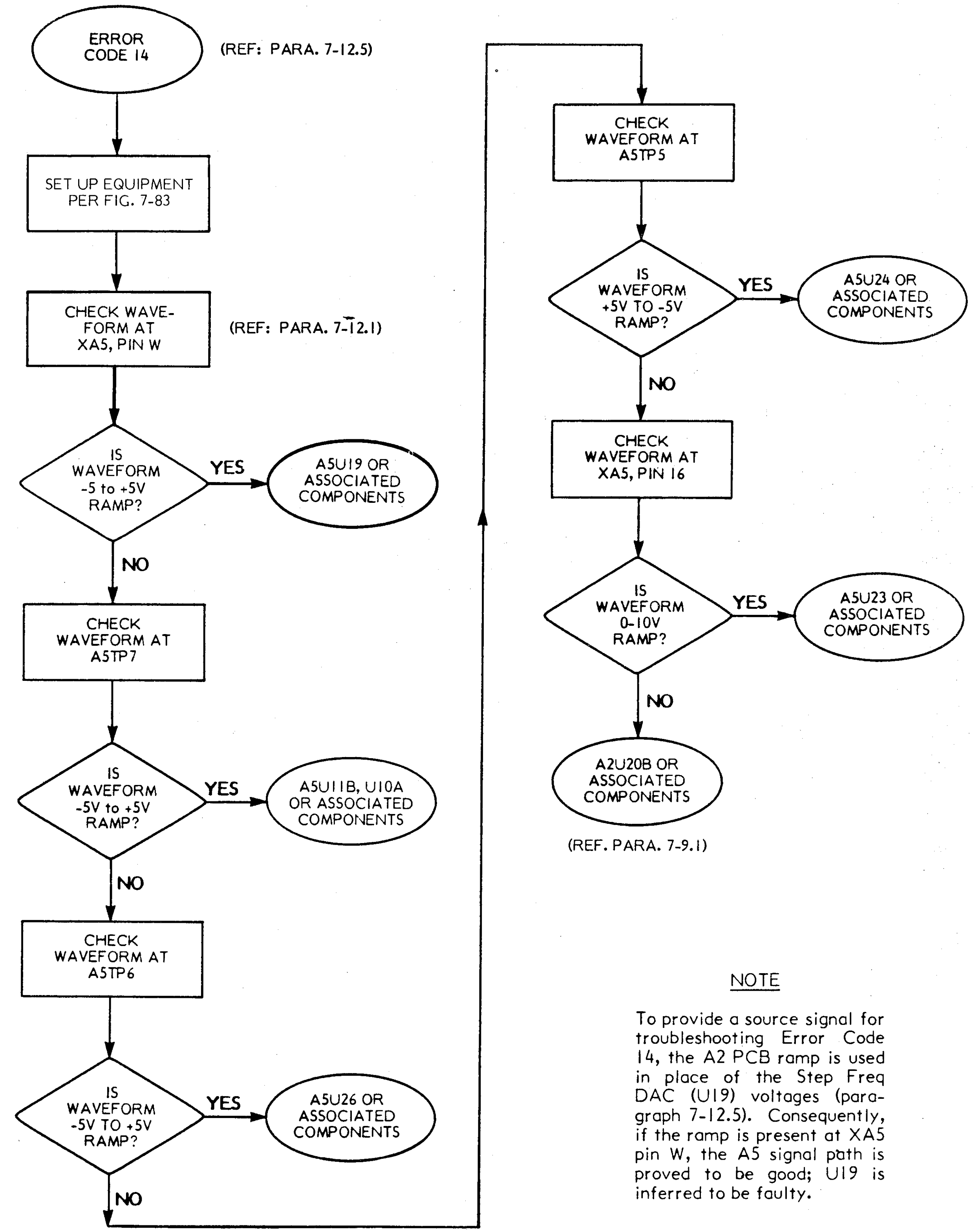


Figure 7-87. Error Code 11 Troubleshooting Flowchart



NOTE

To provide a source signal for troubleshooting Error Code 14, the A2 PCB ramp is used in place of the Step Freq DAC (U19) voltages (paragraph 7-12.5). Consequently, if the ramp is present at XA5 pin W, the A5 signal path is proved to be good; U19 is inferred to be faulty.

Figure 7-88. Error Code 14 Troubleshooting Flowchart

Figure 7-87

7-13 A10 FM/ATTENUATOR PCB

7-13.1 A10 FM/Attenuator PCB, Circuit Description

The A10 FM/Attenuator PCB has two primary functions. The PCB generates currents that control (1) FM modulation for the YIG oscillators, (2) drive for the 2 to 8 GHz YIG tracking filter, and (3) operation of the optional 70 dB Step Attenuator. In addition, this PCB generates the End of Band (EOB) signal that is used on the A2 PCB (paragraph 7-9.1). A functional block diagram of the A10 circuitry is shown in Figure 7-89; the schematic diagram (2 sheets) is shown in Figure 7-90.

The FM input enters this PCB on either the **EXT FM INPUT** signal line, the **ΔF≤50 MHz** signal line, or on both concurrently (Figure 7-89). The **ΔF≤50 MHz** signal line is from the A5 Frequency Instruction PCB. If a delta-frequency sweep mode (ΔF F0, ΔF F1) has been selected and the sweep width (ΔF) is 50 MHz or less, this input is a voltage ramp. As described in paragraph 7-12.1, the amplitude of this ramp depends on the sweep width. For a sweep width of 50 MHz, the amplitude of the ramp is 10 volts (from -5V to +5V). For sweep widths less than 50 MHz, the amplitude of the ramp is proportionally less than 10 volts.

The **EXT FM INPUT** signal line is from the rear panel EXT FM Ø LOCK INPUT connector, which is an isolated-shield-(or floating ground-) type connector. The connector's center conductor and shield leads provide the inputs for the noise-cancelling Diff Input circuit (U4). The output of the U4 circuit is the difference between the two input signals. This output is applied to the EXT FM ENABLE switch (U5). This switch is controlled by the **H EXT FM ENABLE** control line from the mi-croprocessor, via a latch on the A2 PCB. If the front panel FM AND PHASELOCK push-button is engaged, this control line is TRUE. When TRUE, the line causes the EXT FM ENABLE switch to close, allowing the EXT FM INPUT signal to supply an input to the Variable Gain/Inverter stage.

The Variable Gain/Inverter stage (U7) provides a voltage gain for the FM input signal. The amount of gain this stage provides depends on which one of the available YIG oscillators is supplying the output frequency. A LOW logic state on one of the four **YIG FM COIL SEL** lines is used to select the U7 feedback resistor (Figure 7-83), thereby setting circuit gain. At any given time, only one **YIG SEL** line is LOW, signifying that the associated YIG oscillator is presently providing the sweep generator output frequency. For example, in a 6647A full-band frequency sweep, the sequence in which these lines go from HIGH to LOW is as follows:

a. At the start of the sweep (10 MHz), the **YIG 1** line is low and the **YIG 2**, **3**, and **4** lines are all HIGH.

b. When the sweep reaches 8 GHz, the **YIG 1** line goes HIGH and the **YIG 2** line goes low.

c. When the sweep reaches 12.4 GHz, the **YIG 2** line goes HIGH and the **YIG 3** line goes low.

d. When the top of the band (18.6 GHz) is reached, the sweep retraces and starts the cycle over again. During the **YIG SEL** line cycle, the **YIG 4** line stays HIGH.

The output of the Variable Gain/Inverter stage is applied, in parallel, to the WJ (Watkins-Johnson) and Avantek FM coil driver circuits.

To generate its output frequency, the sweep generator uses YIG oscillators manufactured by Watkins-Johnson and Avantek. To accommodate design differences, the A10 PCB has a separate FM coil-current drive circuit for each YIG type. As shown in the schematic (Figure 7-90), these two drive circuits are similar in design; their main differences lie in circuit-component values. Since the two YIG current drivers are similar, only the Avantek circuit is described.

The output from the Variable Gain/Inverter stage is applied to the Avantek circuit Voltage Amplifier (U9). The output of this amplifier drives the Current Amplifier circuit (Q3, Q4). The output of the Q3/Q4 circuit supplies current to all of the series-connected Avantek YIG oscillator FM coils.

This coil current returns to ground via the Current Sense resistor on the A10 PCB. The Current Sense resistor (actually four resistors: R51-R54) is effectively in series with the FM coils. The voltage drop across the Current Sense resistor is proportional to the current through the FM coils.

To reiterate, all three YIG oscillators receive their drive and FM coil currents in series. Only one oscillator band at a time, however, has its output switched to the sweep generator RF output circuit. This RF output switching is a function of the PIN switch, described in paragraph 7-14.

In addition to supplying the input for the FM coil-current driver circuits, the Variable Gain/Inverter stage also supplies the input for the Tracking Filter current-driver circuit. The operation of this circuit is similar to that described for the Avantek FM coil-driver circuit above.

Presently, a tracking filter is used only with the 2-8 GHz YIG oscillator (Oscillator Band 1). This filter is a high-Q YIG bandpass filter that is contained in the same module as the YIG oscillator. This filter YIG is placed in series with the oscillator YIG and tracks at the same frequency, thereby attenuating harmonic and spurious signals.

The fourth current driver circuit on this PCB is the High Current Drivers circuit (U12, U13, U14, U15) used for the Option 2, 70 dB Step Attenuator. These drivers provide the operating currents for the attenuator circuits. The step attenuator high-current drivers are in place on this PCB, even if the optional attenuator is not installed in the sweep generator.

The remaining circuit on the A10 PCB is the End of Band Pulse Generator (U1A-U1D, U2). This circuit generates a low-true pulse whenever a bandswitch point is reached. The inputs to this circuit are the L **HET YIG SEL** line, and the low-true **YIG 1**, **2**, **3**, and **4 SEL** lines previously described. The L **HET YIG SEL** line is LOW only when the sweep generator is in the 10 MHz to 2 GHz heterodyne band. (When in the heterodyne band, the **YIG 1** line is also LOW.) An example of EOB Circuit operation is given below. In this example, which is for a 6647A, the following sequence occurs for a full-band sweep:

e. When the sweep reaches 2 GHz, the L **HET** line goes HIGH (the **YIG 1 SEL** line stays LOW) and generates the L **EOB** pulse.

f. When 8 GHz is reached, the **YIG 1 SEL** line goes HIGH and the **YIG 2 SEL** line goes LOW and generates the L **EOB** pulse.

g. When 12.4 GHz is reached, the **YIG 2 SEL** line goes HIGH and the **YIG 3 SEL** line goes LOW. The L **EOB** pulse is generated when the **YIG 2 SEL** line goes HIGH.

h. When the top of the band (18.6 GHz) is reached, the above cycle repeats.

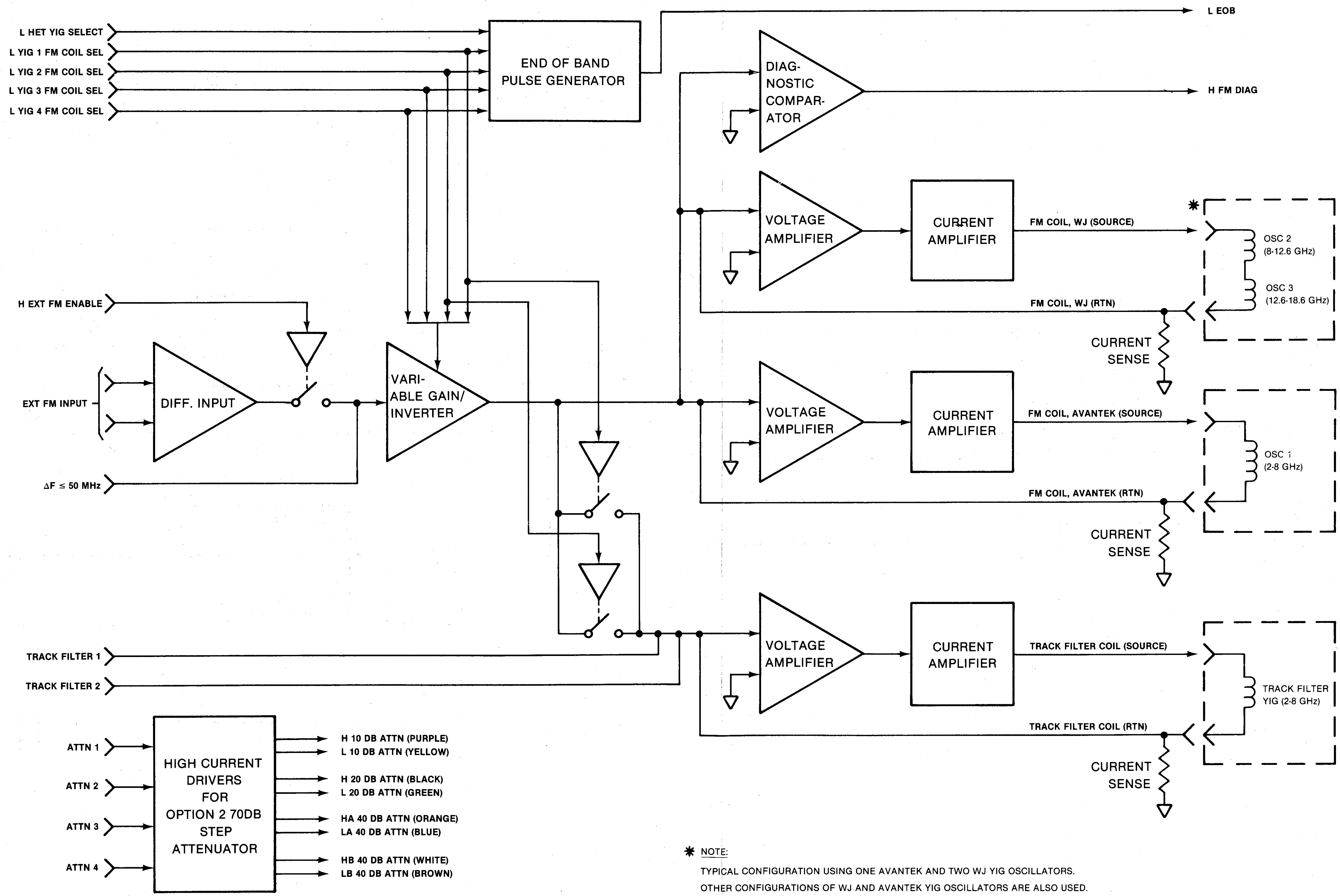
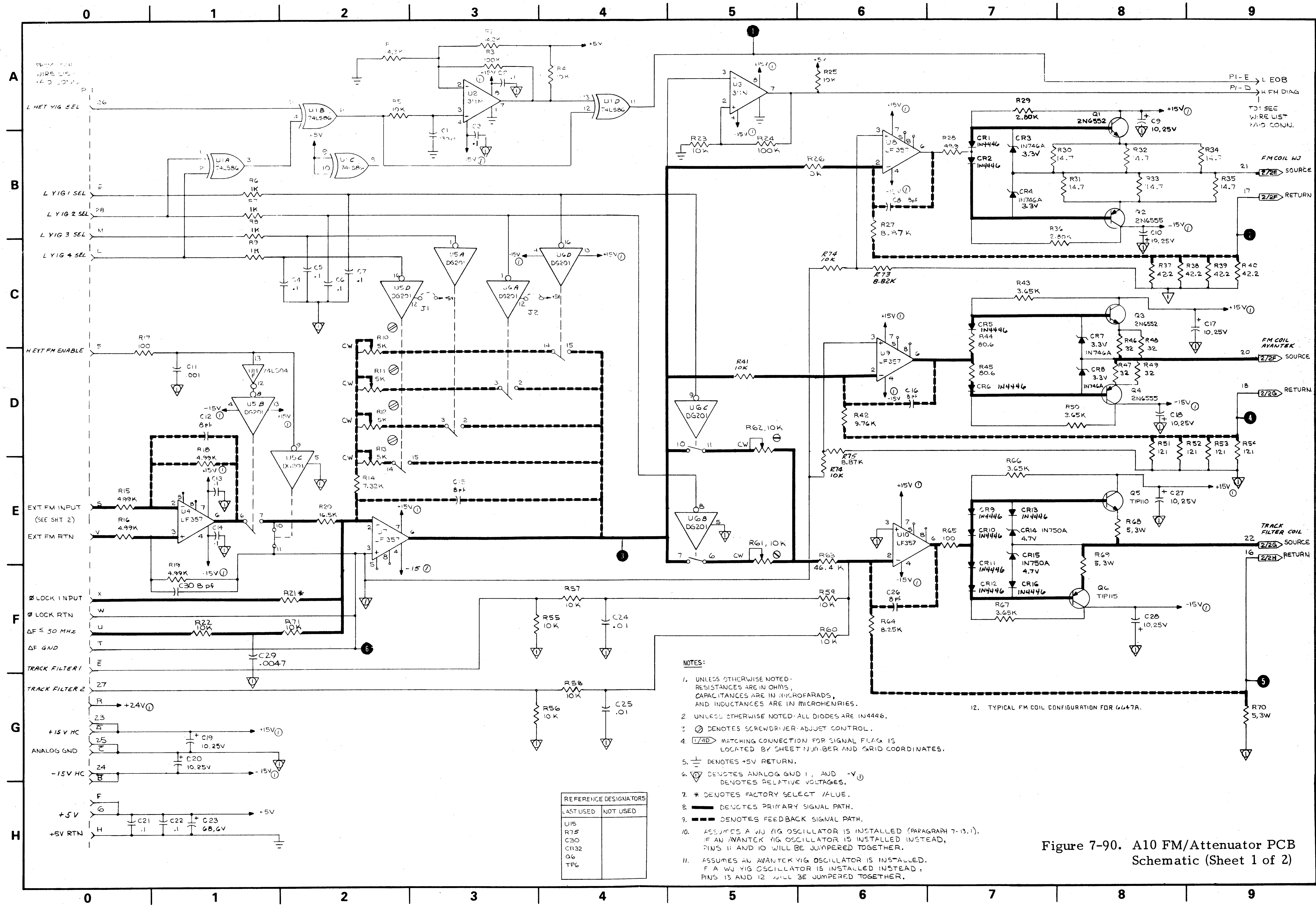


Figure 7-89. A10 FM/Attenuator PCB Functional Block Diagram

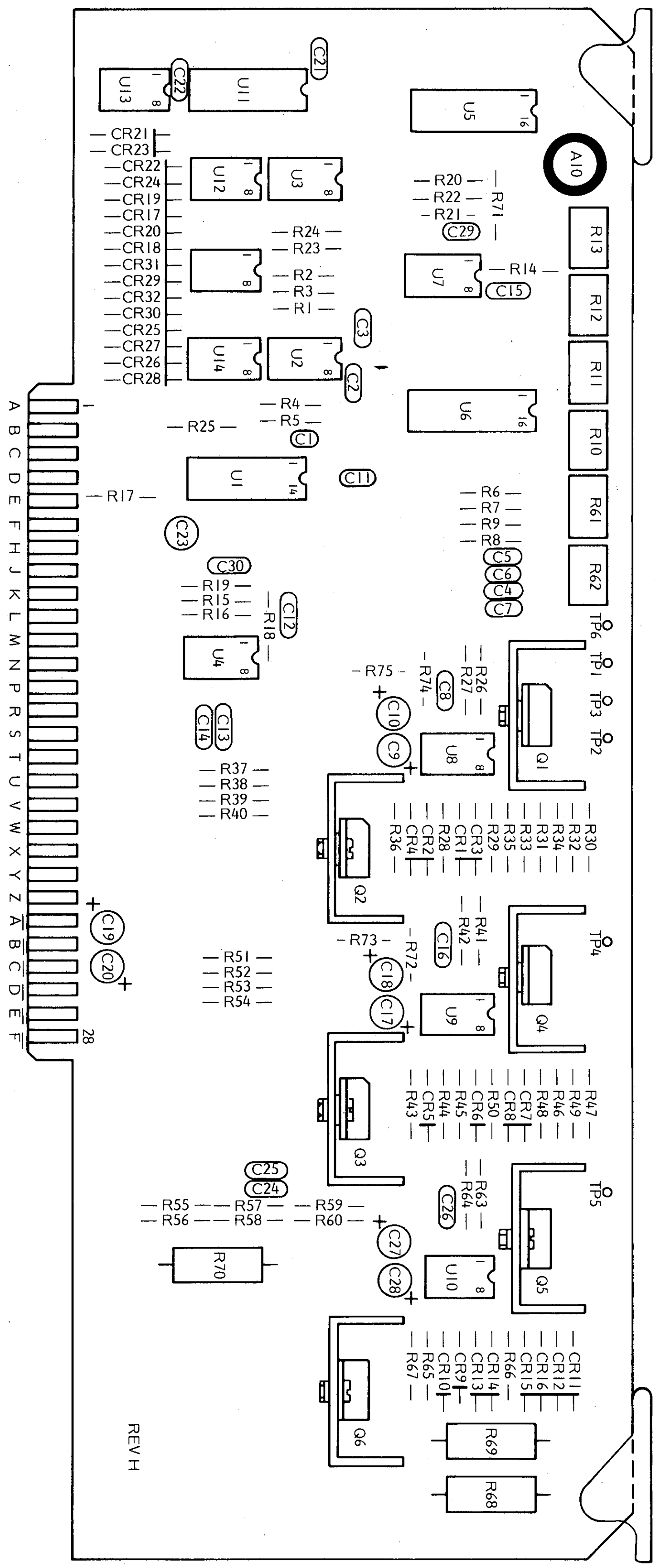


NOTES:

1. UNLESS OTHERWISE NOTED-
RESISTANCES ARE IN OHMS,
CAPACITANCES ARE IN MICROFARADS,
AND INDUCTANCES ARE IN MICROHENRIES.
2. UNLESS OTHERWISE NOTED-ALL DIODES ARE IN4446.
3. ⊘ DENOTES SCREWDRIVER-ADJUST CONTROL.
4. 1/4D> MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ⏚ DENOTES +5V RETURN.
6. ▽(1) DENOTES ANALOG GND 1, AND -V(1) DENOTES RELATIVE VOLTAGES.
7. * DENOTES FACTORY SELECT VALUE.
8. ▬▬ DENOTES PRIMARY SIGNAL PATH.
9. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH.
10. ASSUMES A WJ YIG OSCILLATOR IS INSTALLED (PARAGRAPH 7-13.1). IF AN AVANTEK YIG OSCILLATOR IS INSTALLED INSTEAD, PINS 11 AND 10 WILL BE JUMPERED TOGETHER.
11. ASSUMES AN AVANTEK YIG OSCILLATOR IS INSTALLED. IF A WJ YIG OSCILLATOR IS INSTALLED INSTEAD, PINS 13 AND 12 WILL BE JUMPERED TOGETHER.

REFERENCE DESIGNATORS	
LAST USED	NOT USED
U15 R75 C30 CR32 Q6 TP6	

Figure 7-90. A10 FM/Attenuator PCB Schematic (Sheet 1 of 2)



A10 PCB Parts Locator Diagram

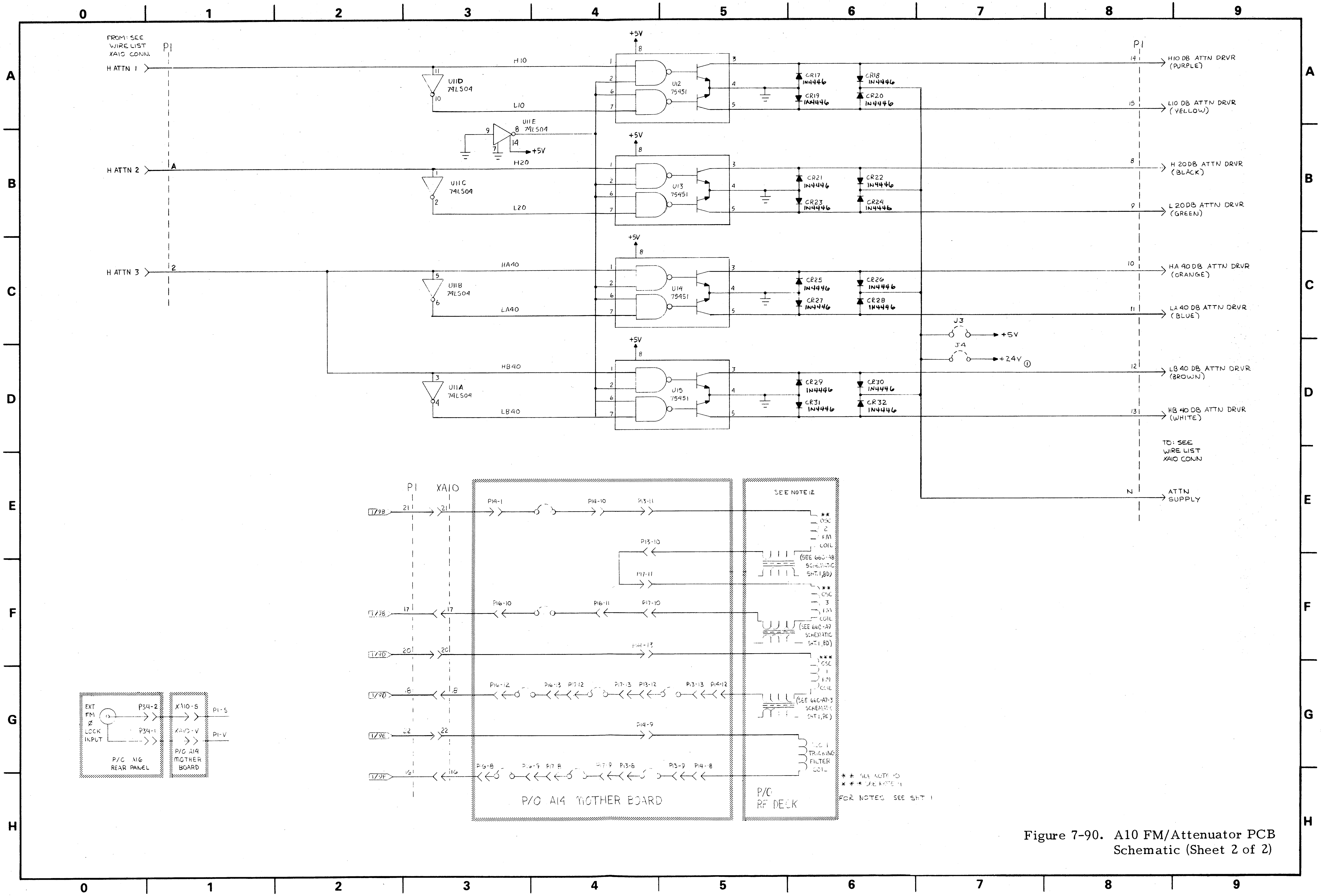
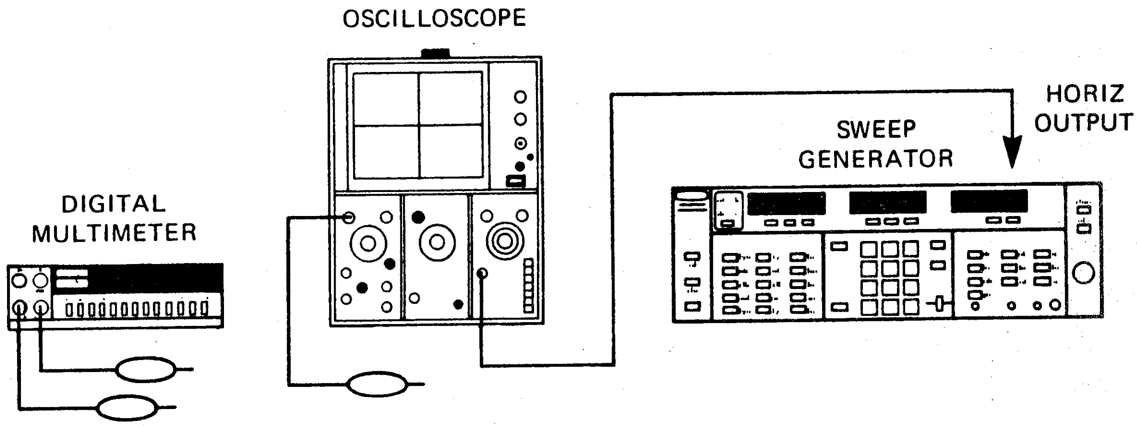


Figure 7-90. A10 FM/Attenuator PCB Schematic (Sheet 2 of 2)

7-13.2 A10 FM/Attenuator PCB, Troubleshooting Information and Data

Error Code 23 reports the status of the A10 FM/Attenuator PCB. The microprocessor routine associated with this error code tests the A10 PCB by simulating a ≤50 MHz sweep and then verifying that the H FM DIAG bit has toggled from LOW to HIGH.

A test equipment setup for troubleshooting Error Code 23 is provided in Figure 7-91, a troubleshooting flowchart is provided in Figure 7-92, and a troubleshooting block diagram is provided in Figure 7-93.



SWEEP GENERATOR CONTROL SETTINGS

FREQUENCY RANGE: ΔF F0
RF SLOPE: Off
FM AND PHASELOCK: Off
LEVEL: 0 dBm
TRIGGER: AUTO
SWEEP TIME: 10 ms
MARKERS: All Off
F0: Midband
LEVELING: INTERNAL
ΔF: 50 MHz
RETRACE RF: Off
RF ON: On

Figure 7-91. Test Equipment Setup for Troubleshooting Error Code 23

GENERAL INFORMATION

1. Before starting flowchart, check dc voltages at connector P1, as follows:

   a. +5V, pin F

   b. _15V, pin $\overline{A}$

   c. -15V, pin $\overline{B}$

2. Logic levels are TTL.

3. After completing the flowchart and extinguishing the "Error 23" display, verify the circuit meets the minimum performance criteria in paragraph 4-7.

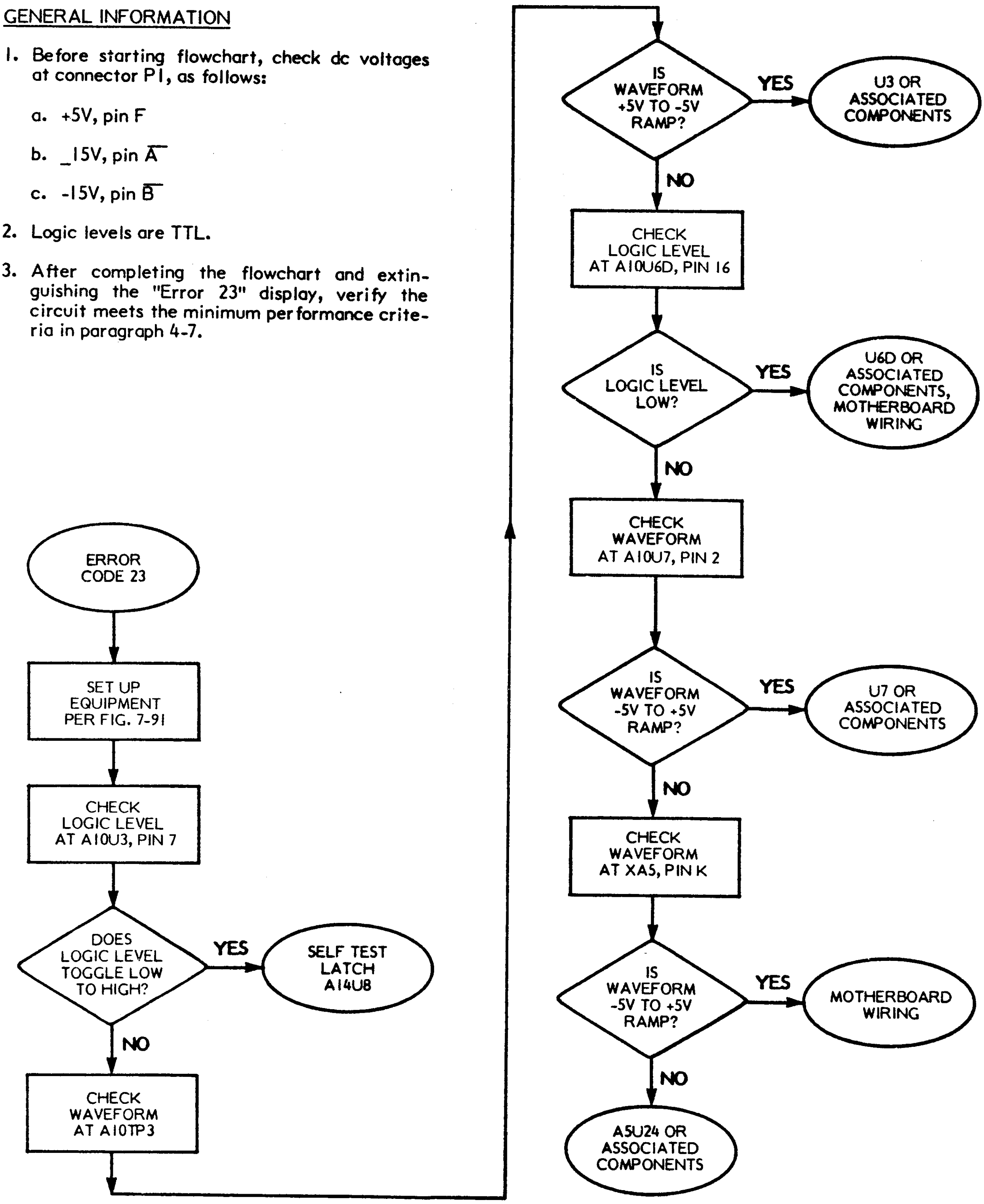


Figure 7-92. Error Code 23 Troubleshooting Flowchart

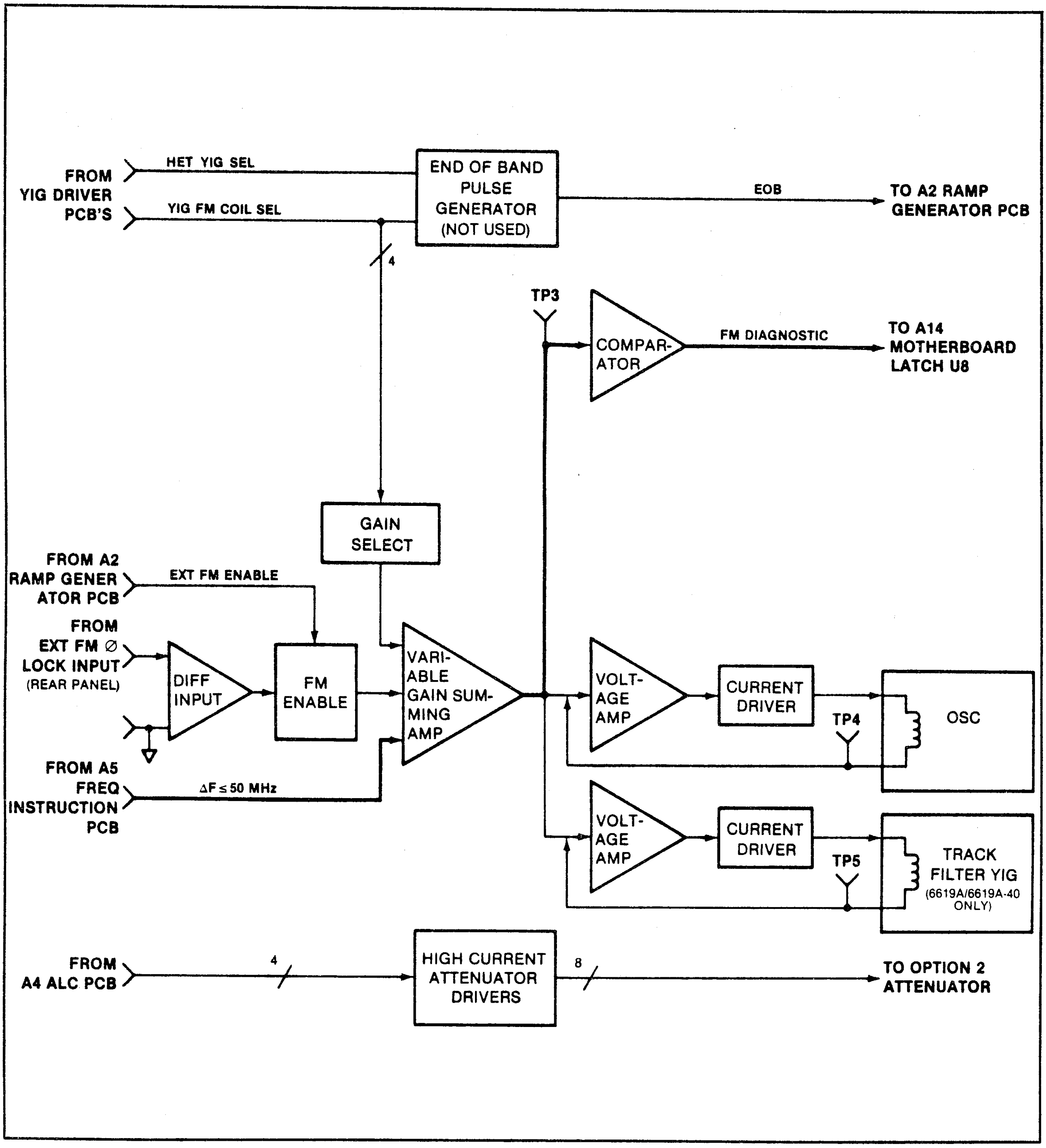


Figure 7-93. Error Code 23 Troubleshooting Block Diagram

7-14 RF DECK, CIRCUIT DESCRIPTION

The RF Deck components are used to generate sweep- and CW-frequency RF signals, and to route such signals to the front and rear (if applicable) panel RF OUTPUT connectors. Block diagrams showing RF component configurations are provided in Figures 7-94 thru 7-102. The RF components are described below:

a. Oscillators. The YIG-tuned oscillators are of two basic types – Gunn Diode and GaAs FET; they are supplied by two main vendors – Watkins-Johnson (WJ) and Avantek.

b. MOD (Modulator). The MOD unit is a current-controlled variable attenuator that provides amplitude modulation and power leveling for the Osc 1 output. It also provides impedance matching and isolation for the Osc 1 YIG.

c. Isolators. The Isolators prevent reflected RF energy from returning to the YIG and causing frequency pulling. They attenuate the forward-wave energy by ≈0.5 dB and the reverse-, or standing-wave, energy by ≥ 20 dB.

d. Filters. The filters provide bandpass filtering for the RF frequencies, to reduce harmonics.

e. PIN Switch. The PIN Switch is a current-controlled variable attenuator that switches between the available YIGs so that only one at a time is coupled to the RF OUTPUT circuit. The switch also provides the means for amplitude-modulating and power-leveling the RF output signal.

f. Heterodyne Down Converter. The Heterodyne Down Converter generates the .01 to 2 GHz sweep- and CW-frequency outputs. When a frequency between .01 and 2 GHz is selected from the front panel, the output of the Osc 1 YIG is modified to sweep between 4.61 and 6.6 GHz. Via the PIN Switch, this modified YIG output is mixed with the output from a 4.6 GHz local oscillator. The difference frequency is amplified and used to provide the .01 to 2 GHz output. When the .01-2 GHz band is selected, a portion of the down converter's Mixer is detected and used for internal leveling.

g. Coupler. The Coupler couples and detects a portion of the >2 GHz RF output for use in internal power leveling. The detected sample, along with a voltage representing the coupler's temperature, is routed to the A4 PCB.

h. Attenuator. The optional Attenuator provides up to 70 dB of attenuation for the RF output. The drive current for the attenuator is supplied by a cable from the A10 PCB.

i. Transformers (not shown on figure). Tranformers are used to improve linearity for sweeps ≤50 MHz. A transformer is provided for each of the available YIG oscillators. One transformer winding is in series with the YIG's main tuning coil, and the other winding is in series with the YIG's FM tickler coil.

j. Amplifiers. The amplifiers used with the 6600A-40 models amplify the applicable 2-8, 8-12.4, and 12.4-18.6 GHz YIG oscillators' frequency by approximately 6 dB. Minimum output is ≥ 20 dBm.

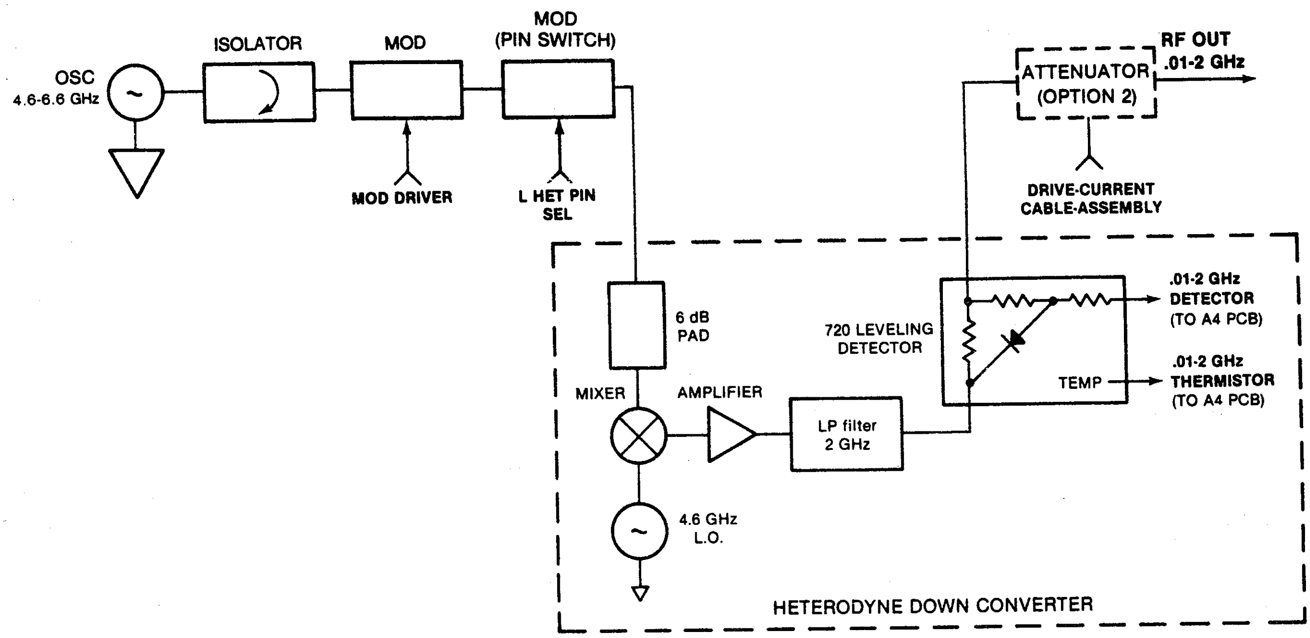


Figure 7-94. Model 6609A RF Components

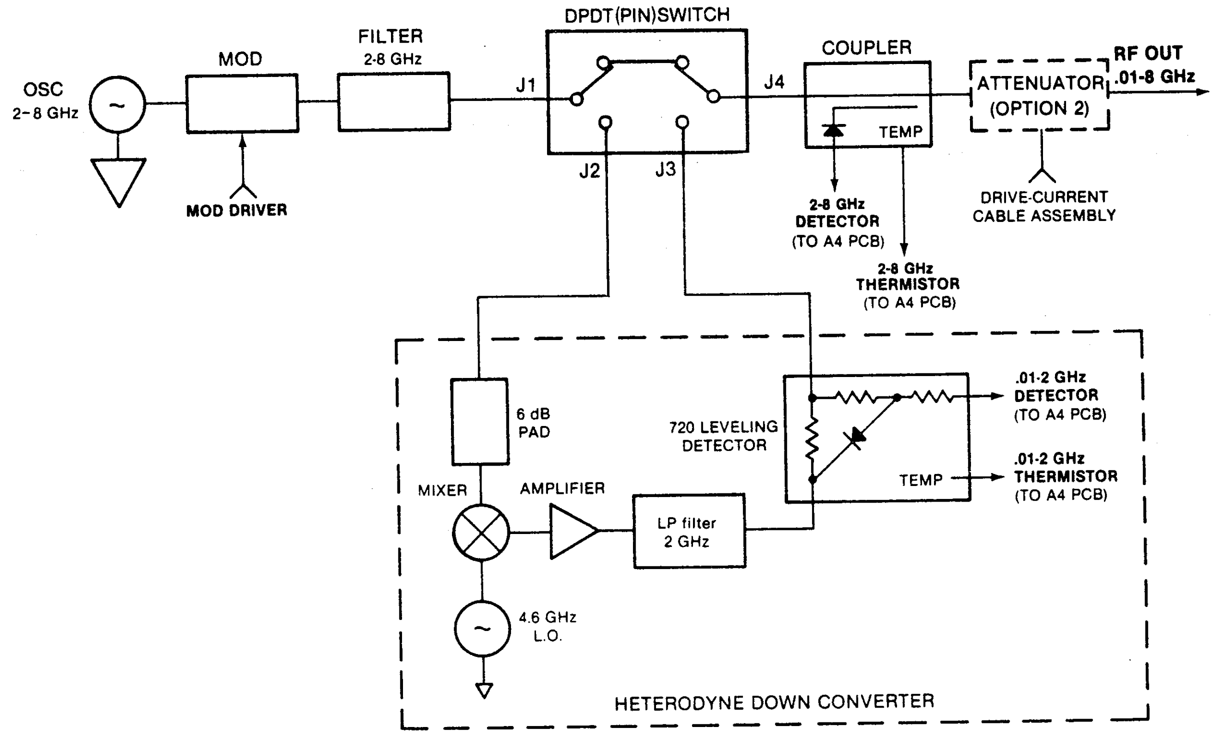


Figure 7-95. Model 6617A RF Components

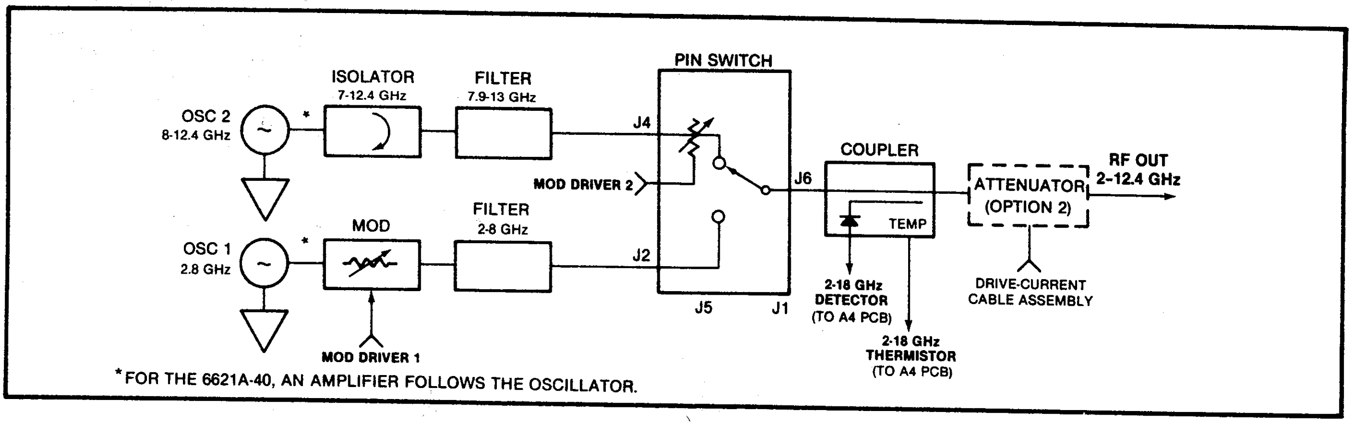


Figure 7-96. Model 6621A/6621A-40 RF Components

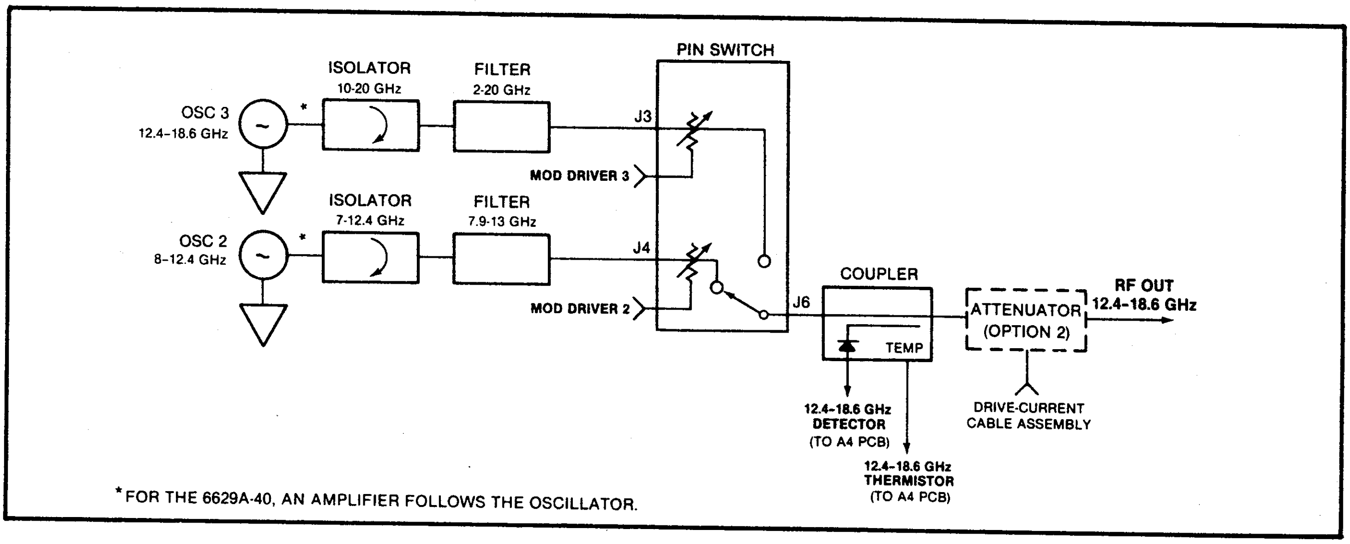


Figure 7-97. Model 6629A/6629A-40 RF Components

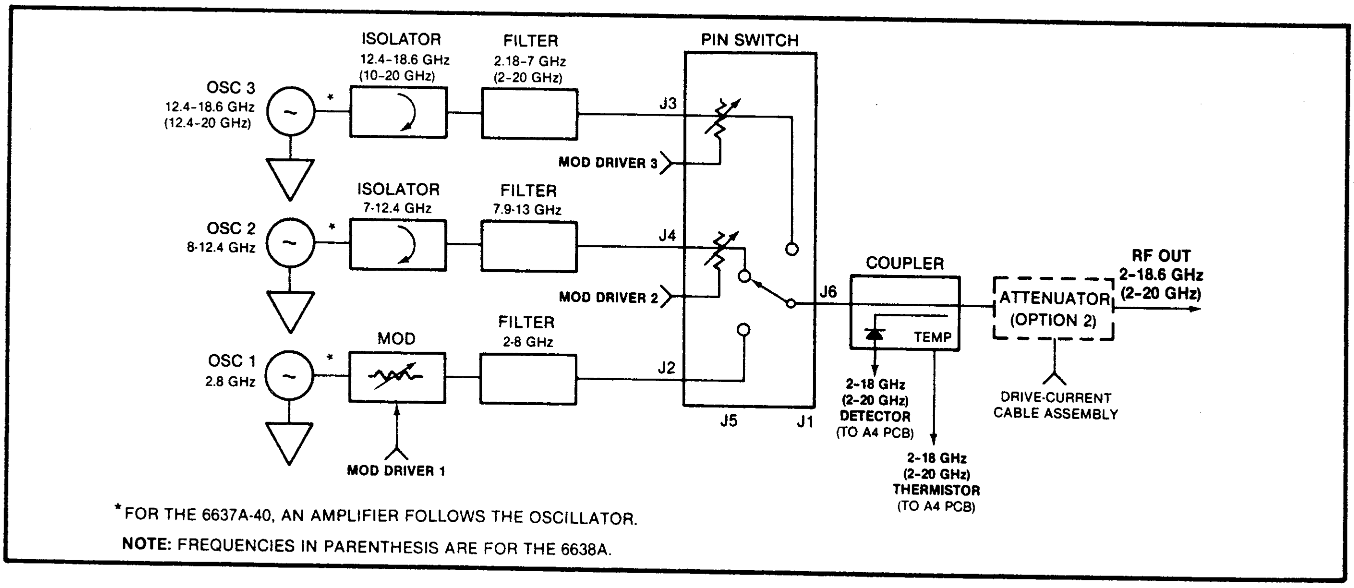


Figure 7-98. Model 6637A/6637A-40/6638A RF Components

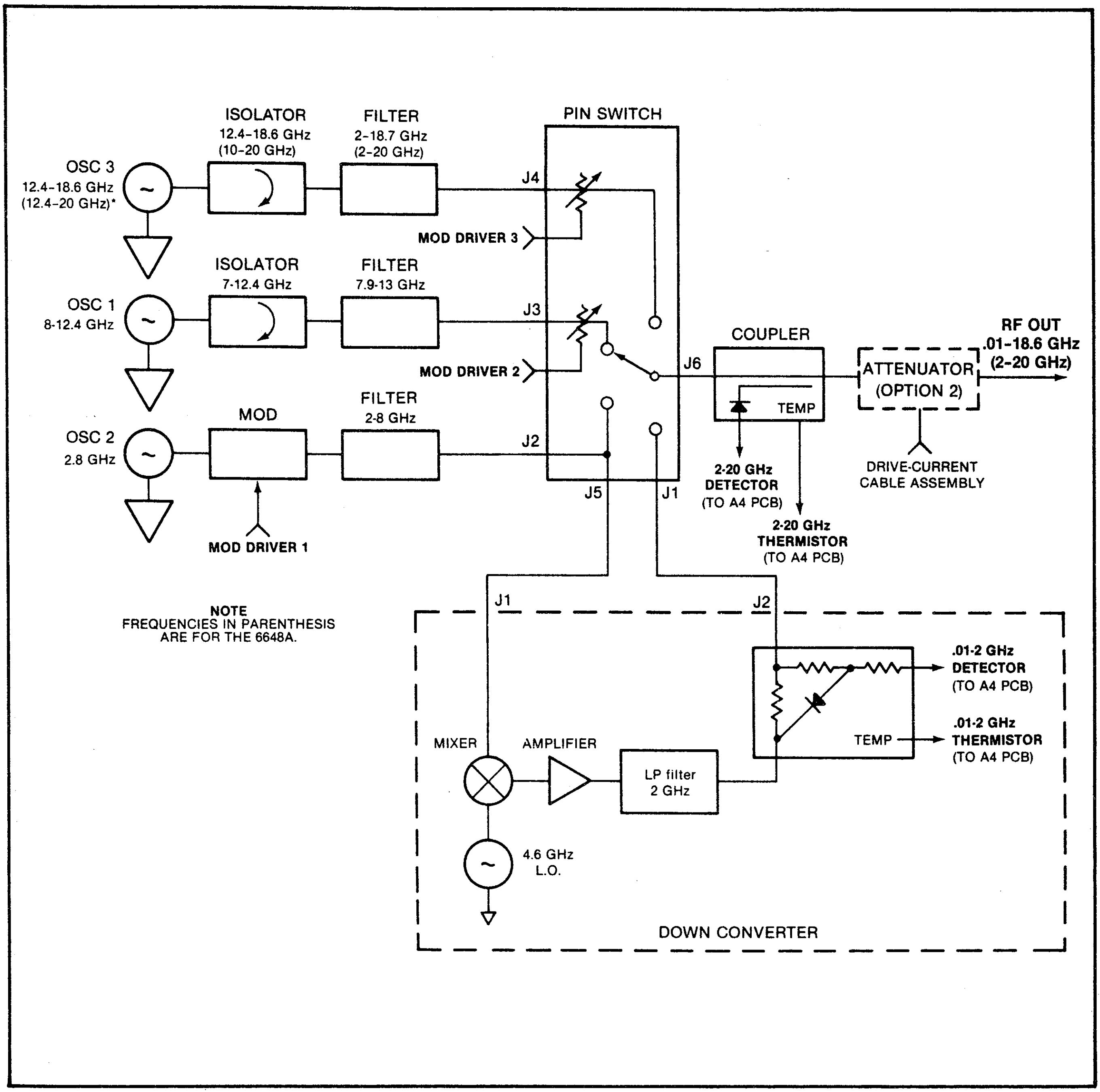


Figure 7-99. Model 6647A/6648A RF Components

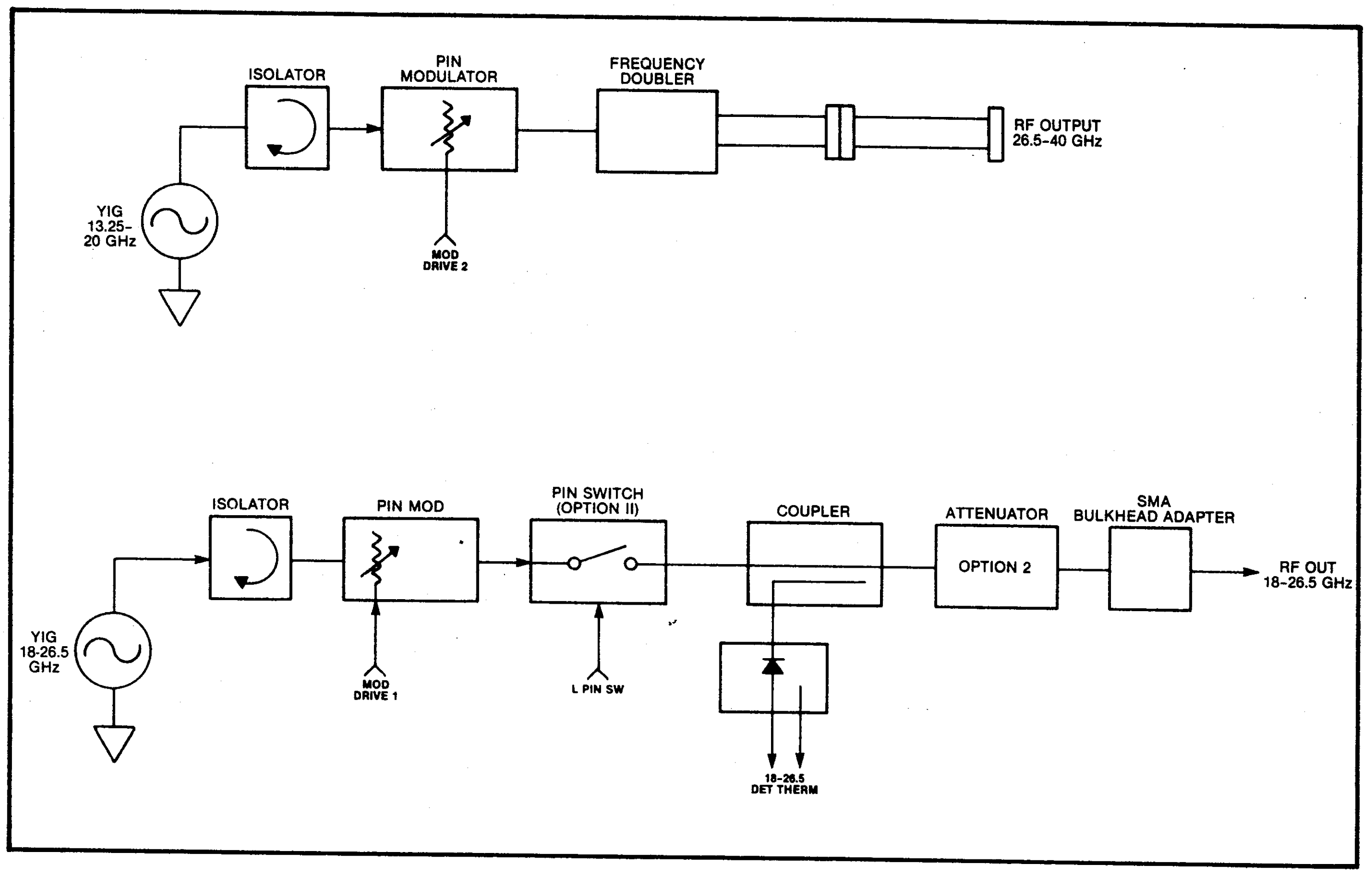


Figure 7-100. Model 6642A RF Components

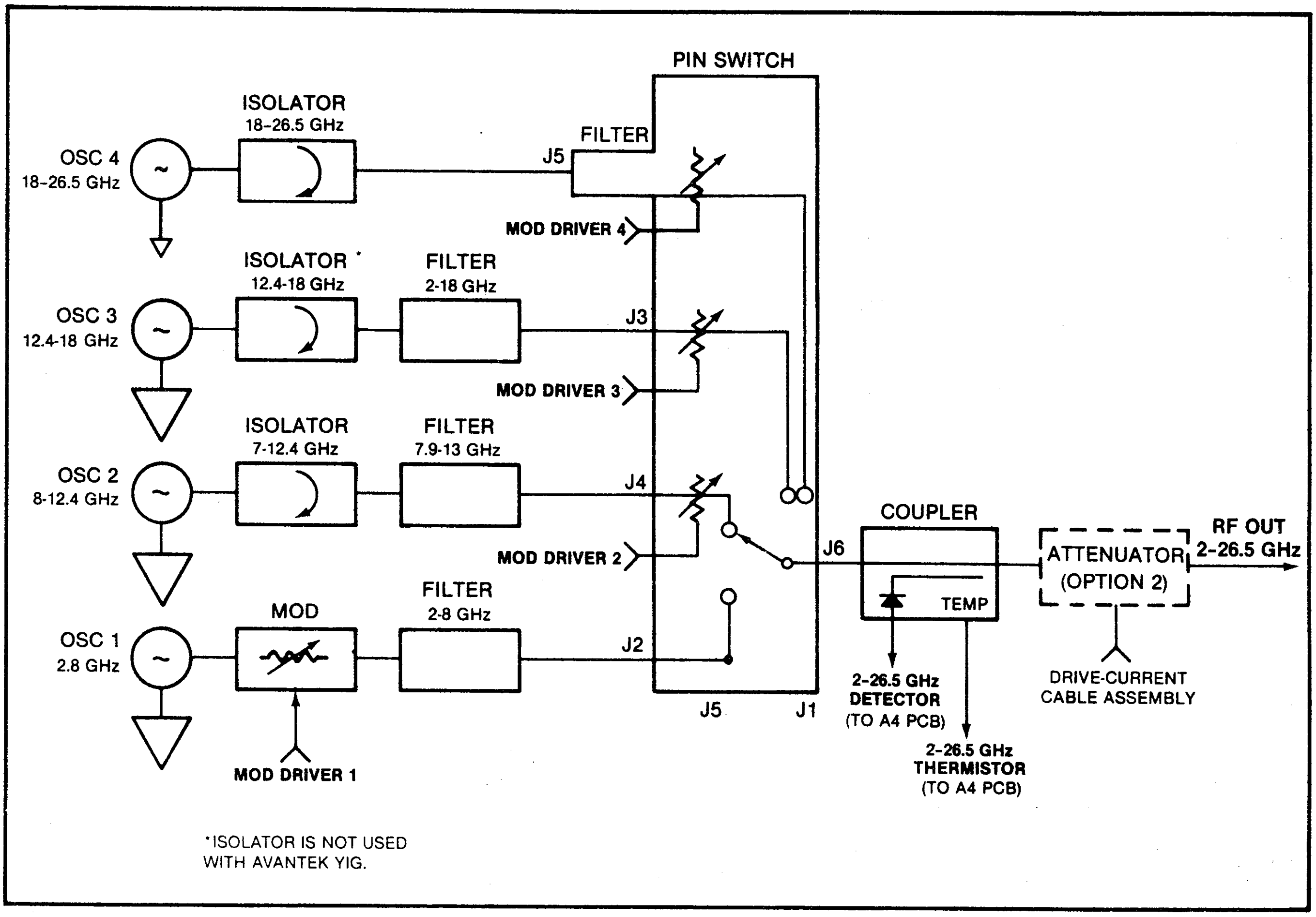


Figure 7-101. Model 6653A RF Components

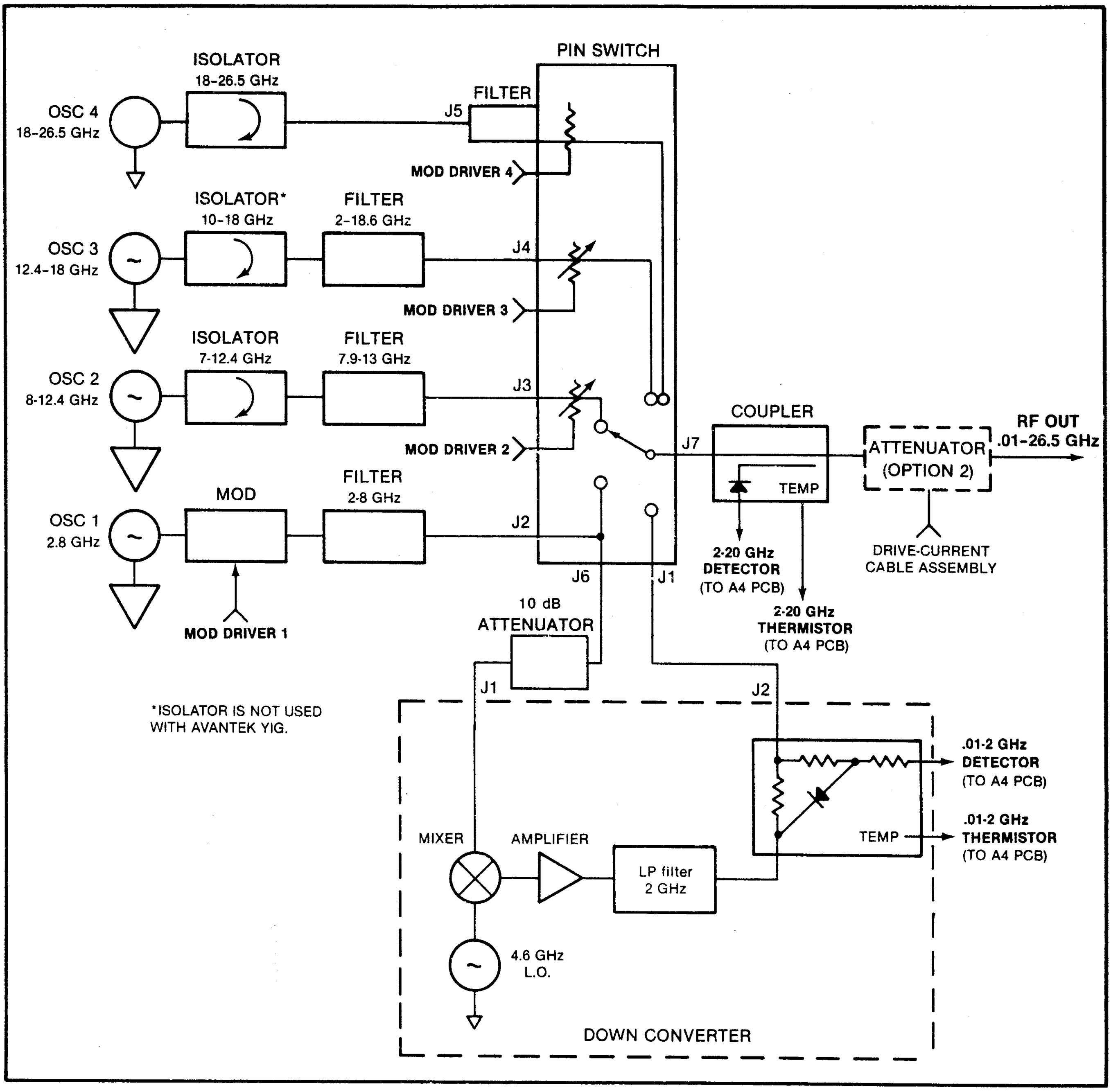


Figure 7-102. Model 6659A RF Components

7-15 A13/A14 SWITCHING POWER SUPPLY AND A14 MOTHERBOARD PCB'S

7-15.1 A13/A14 Switching Power Supply, Circuit Description

The A13/A14 Switching Power Supply is a half-bridge, quasi-square-wave, high-efficiency +5V converter that also contains the ±15V LC (low current), ±15V HC (high current), +12V, +24V, and -39V regulated voltage supplies, and the +18V, +12/-24V, and +28V unregulated voltage supplies. An overall block diagram of the switching power supply is shown in Figure 7-106. A parts locator diagram for the A13/A14 circuit is shown in Figure 7-107. And the A13/A14 schematics (4 sheets) are shown in Figure 7-108.

WARNING

> Voltages hazardous to life are present throughout the Switching Power Supply. When performing any maintenance, use extreme care to avoid electrical shock.

As shown in Figure 7-106, the switching power supply circuits and components are dispersed over the following PCBs and assemblies:

a. A16 Rear Panel Assembly: Line Voltage Selector Module, Fan, Fan Transformer, and Power Switch;

b. A14 Motherboard PCB: Off-Line Rectifier, Over-Current Sense, Over-Voltage Sense, Out of Reg Sense, Line Sense, -39V and +24V Regulator circuits;

c. A13 Switching Power Supply PCB: Control Amplifier, Soft-Start Control, Shut-Down Timer, Pulse-Width Modulator, and Switching Transistors circuits; and

d. A0 Basic Frame Assembly: +/-15V Regulator integrated circuits and -39V Regulator pass transistor.

The ac line power entering the sweep generator is input to the Off-Line Rectifier circuit (A14CR12). This circuit is a full-wave voltage doubler (120V line) or a full-wave bridge rectifier (220V line). The circuit's voltage output for either input-line voltage is 330 Vdc (±165 Vdc). The circuit's output current is sensed by A14R16 and if greater than 2 amperes, activates the optically-coupled Overcurrent Sense circuit (A14U1). When activated, A14U1 causes the Shut Down Timer circuit to turn off the switching transistor drive voltage. The ±165 Vdc output from the Off-Line Rectifier circuit is applied to the dc-isolated Switching Transistors on the A13 PCB.

CAUTION

> Use an isolation transformer between the sweep generator and the ac line whenever maintenance is being performed on the switching power supply. Because portions of this power supply are referenced to the peak-negative or -positive line voltage, an isolation transformer is necessary to protect test instruments.

The Switching Transistors (A13Q5, A13Q6) alternately switch between **+165 Vdc** and **-165 Vdc** at a 50 kHz rate. These transistors are driven by the Pulse-Width Modulator (PWM) circuit (A13U4, A13Q3, A13Q4). This circuit (Figure 7-105) is used to develop a train of pulses. The duty cycle of this pulse train varies between 25 and 40% (approximately), depending on the amplitude of control voltage "Vc." This Vc-voltage amplitude is determined by either the Control Amplifier (A13U2), the Soft-Start Control circuit (A13Q1), or the Shut-Down Timer circuit (A13U3).

The input to the Control Amplifier is the **+5V SENSE** line from the motherboard. This line senses the voltage across the +5V load. The output of A13U2 forces the PWM to adjust the duty cycle to whatever is necessary to maintain +5V at the sense line.

The input to the Soft-Start Control circuit is +12V from the +12V Regulator (A13U1). At the instant the POWER switch is pressed,

+12V is applied to A13Q1 and, via C6, to the "Vc" pin on A13U4. With the Vc pin at +12V, the duty cycle of the A13U4 output pulse-train is minimum, thus causing the output of the +5V supply to be minimum. As C6 charges, the voltage at the A13U4 "Vc" pin decreases, the duty cycle of the A13U4 output pulse train increases, and the +5V supply output voltage increases. When the Control Amplifier senses that 5 volts has been reached (≈20 ms), regulation occurs. If a malfunction were to occur, such as A13U2 failing, the Over-Voltage circuit (A14Q4) would trigger the Shut-Down Timer circuit at approximately 5.7 volts.

The input to the Shut-Down Timer circuit (A13U3) is a trigger pulse caused by the **OVER-VOLTAGE/CURRENT** line going LOW. When triggered, A13U3 generates a 1-second pulse (approximately) that causes the A13U4 "Vc" voltage to go to +12V and the A13U4 "INH" (inhibit) voltage to go LOW. When the "INH" voltage is LOW, A13U4 is turned off; this shuts down the Switching Transistors. After A13U3 times out, the INH input goes HIGH and the power supply soft-starts. However, if the condition causing the A13U3 trigger is still present, A13U3 generates another pulse and shuts the supply down again. This A13U3 pulsing operation continues until either the over-voltage/current condition is corrected or the POWER switch is pressed OFF.

The outputs from the PWM circuit are coupled across dc isolation transformers T1 and T2, and used to drive FETs Q5 and Q6. These FETs require a bias of ≥5V to be switched on. The outputs from Q5 and Q6 form a composite waveform (Figure 7-103). The peak-to-peak value of this waveform is directly proportional to the peak value of the 120V line (or directly proportional to the peak-to-peak value of the 220V line). This waveform is coupled to the five secondaries of A13T3. The reduced voltages appearing in these secondaries are also proportional to the line voltage. These reduced voltages are rectified and passed through an inductor, which is used as an integrator. The value of the voltage that is output from the inductor can be controlled entirely by T_1 (Figure 7-104) (the duty cycle of the PWM).

As shown in Figure 7-106, the five rectifier circuits – excepting the +5V and the +12/-24V circuits – supply their respective outputs to voltage regulators. The -39V Regulator (A14Q1, A14Q2, A14Q3, and A0Q1) is driven by the -43V supply. The +24V Regulator (A14U2) is driven by the +28V supply. The -15V LC (low current) and HC (high current) Regulators (A0U1, A0U2 respectively) are driven by the -18V supply. And the +15V LC and HC Regulators (A0U3 and A0U4 respectively) are driven by the +18V supply. The unregulated +18V also goes to the YIG driver bias supply on the A6-A9 PCBs and to the +15V Rectifier circuit. At the +15V Rectifier Circuit, the +18V both reverse-biases A14CR7/A14CR8 and provides the input for voltage regulator A13U1.

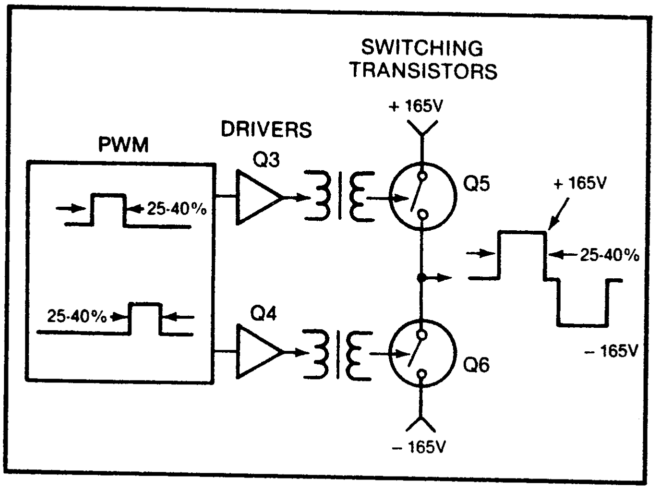


Figure 7-103. A13 Switching Transistors, Simplified Schematic

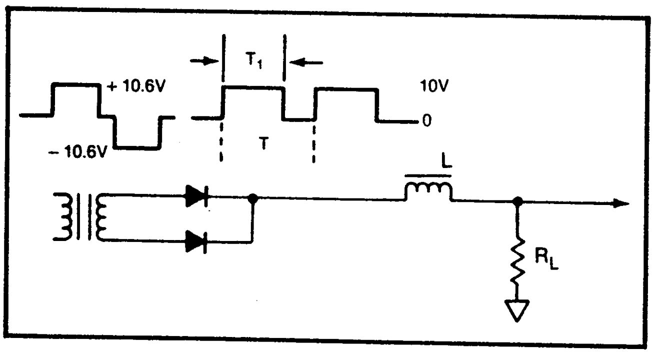


Figure 7-104. A13 Regulator, Simplified Schematic

The remaining two circuits in Figure 7-106 are the Out of Reg Sense (U4A, U4B, U5C, U5D) and the Line Voltage Sense (U5A, U5B) circuits. The Out of Reg Sense circuit detects when any of the regulated supplies goes out of tolerance. If such a condition exists, the **L OR** diagnostic line goes TRUE and the A14 OUT OF REG indicator LED lights. The Line Voltage Sense circuit detects when the ac line exceeds the +5% or -10% limits required for circuit operation. This circuit also detects if the Line Voltage Selector Module printed circuit card is correctly positioned for the available line voltage. If either the line voltage is incorrect or the PC card is improperly positioned, the appropriate **L HL** or **L LL** diagnostic line will go TRUE, and the LED indicator will light.

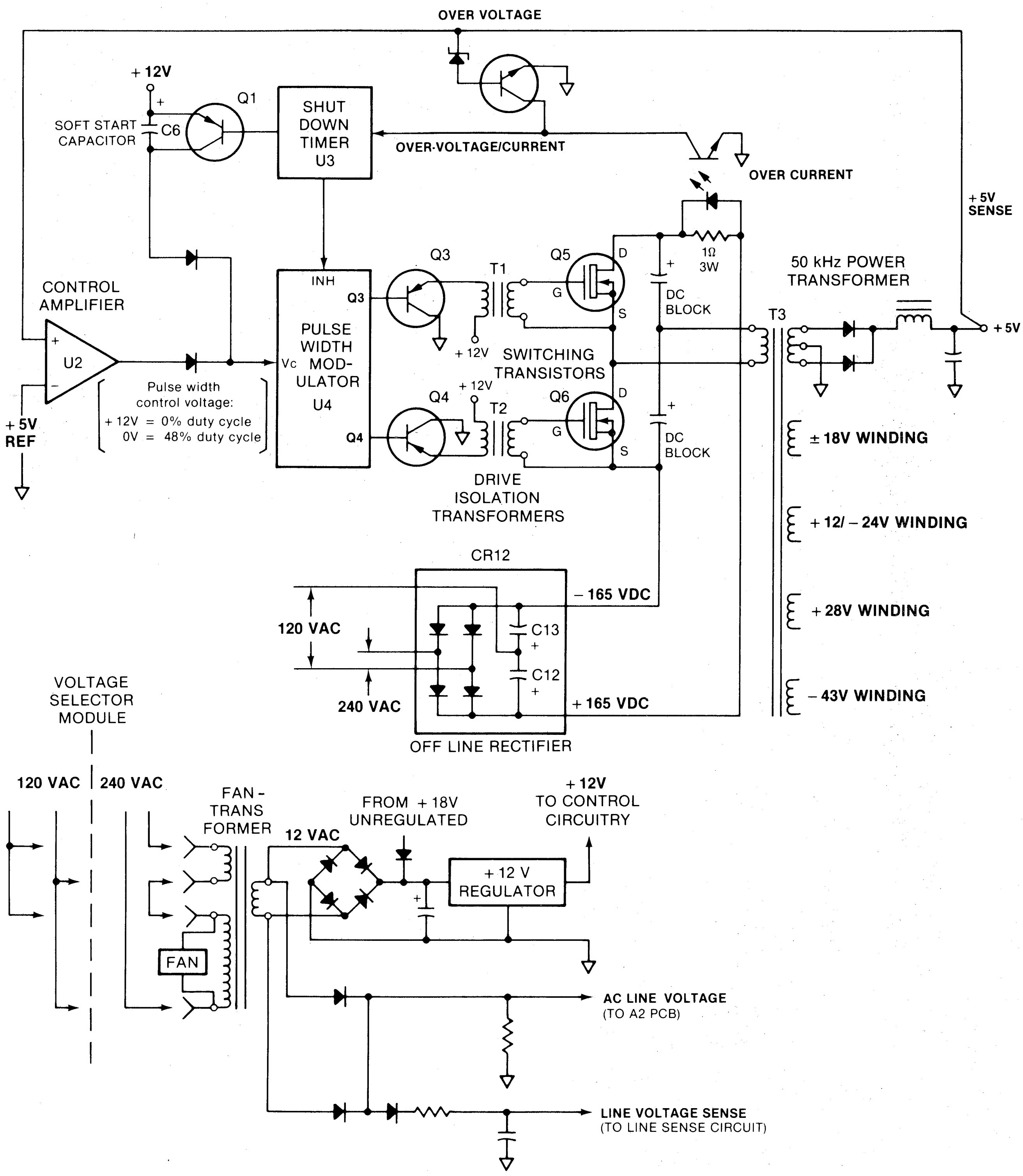
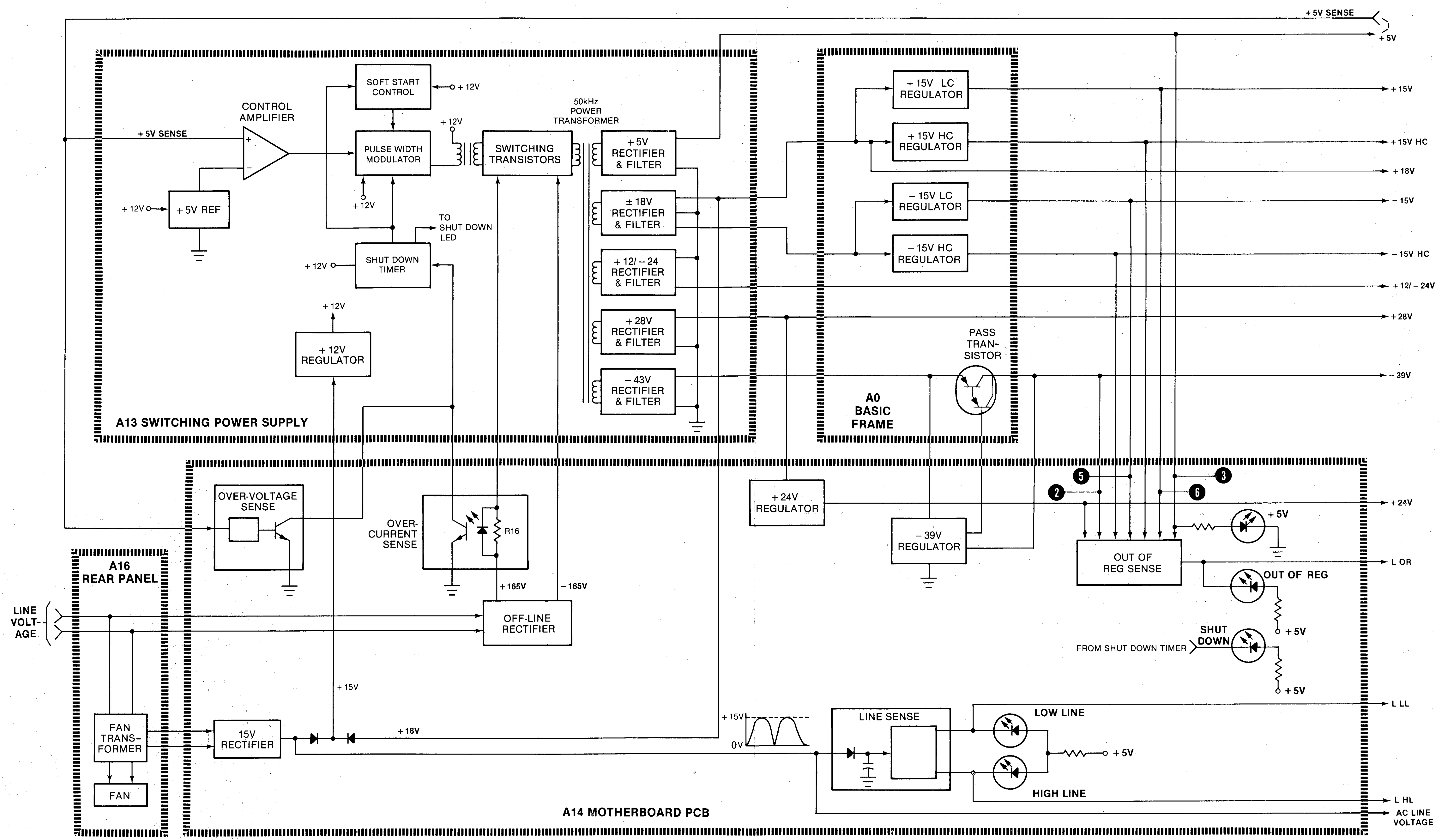


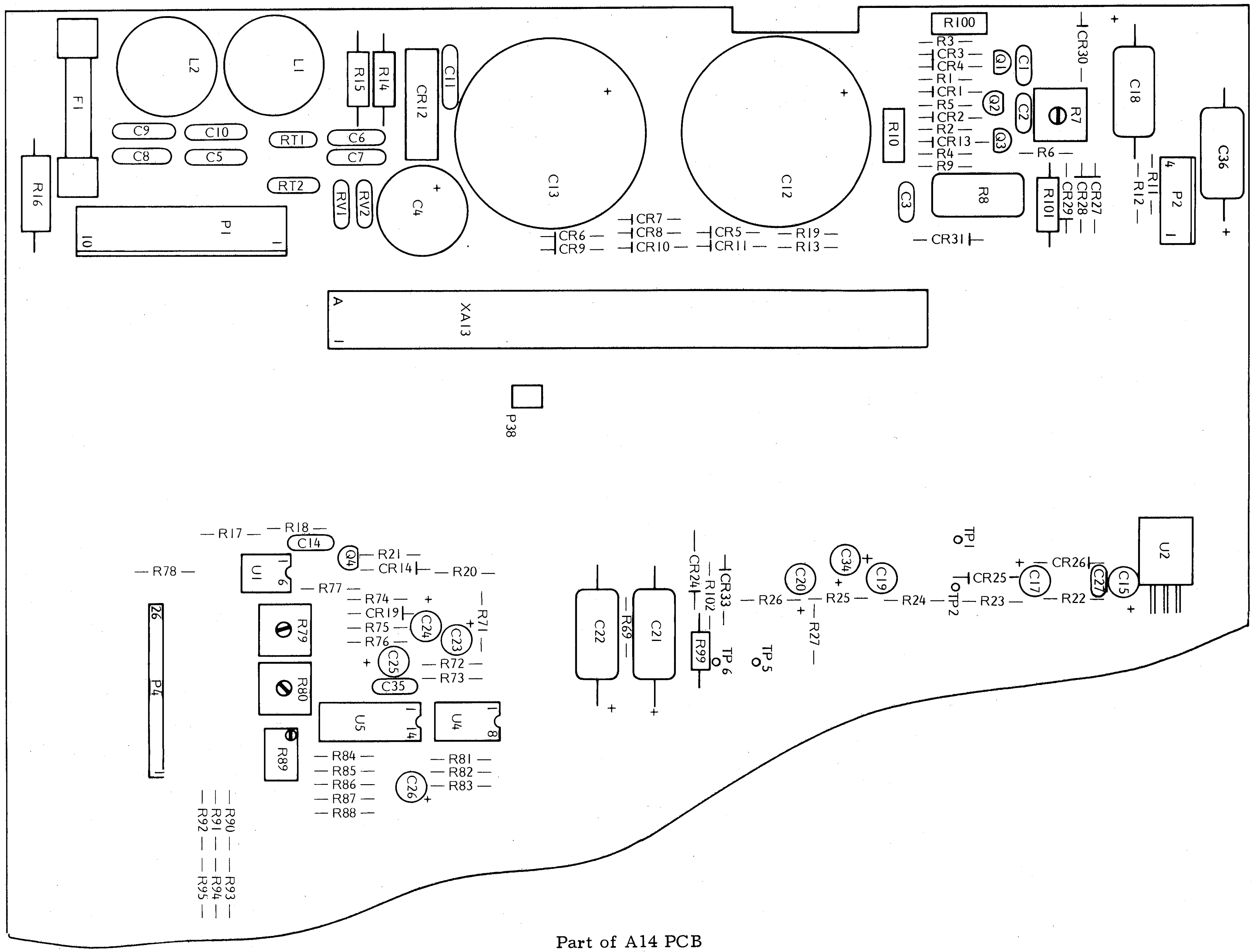
Figure 7-105. A13/A14 Switching Power Supply, Simplified Schematic



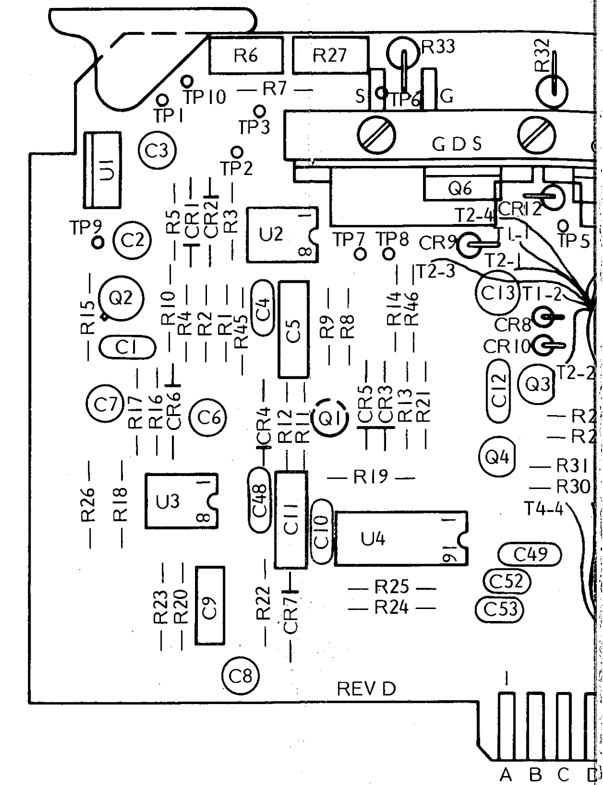
SEE FIGURE 7-79 FOR SIMPLIFIED SCHEMATIC OF A13/A14 SWITCHING POWER SUPPLY

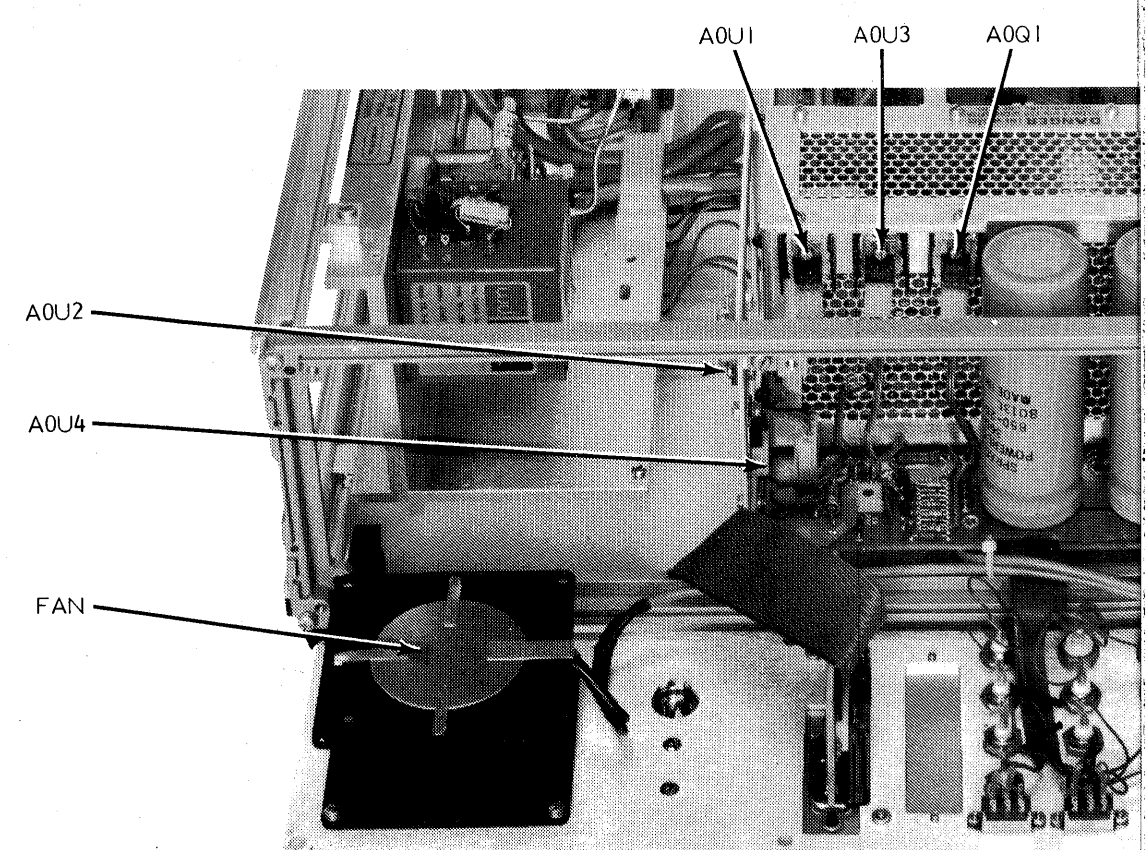
Figure 7-106. A13/A14 Switching Power Supply Overall Block Diagram

Figure 7-105

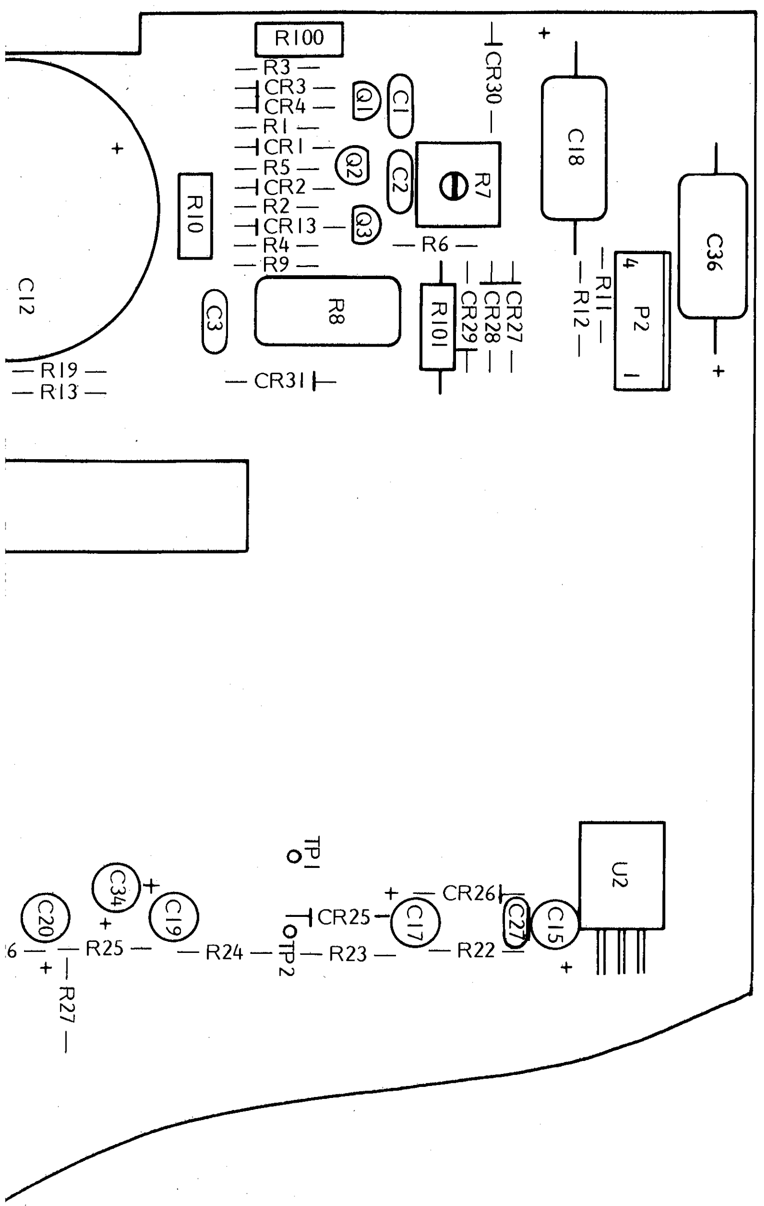


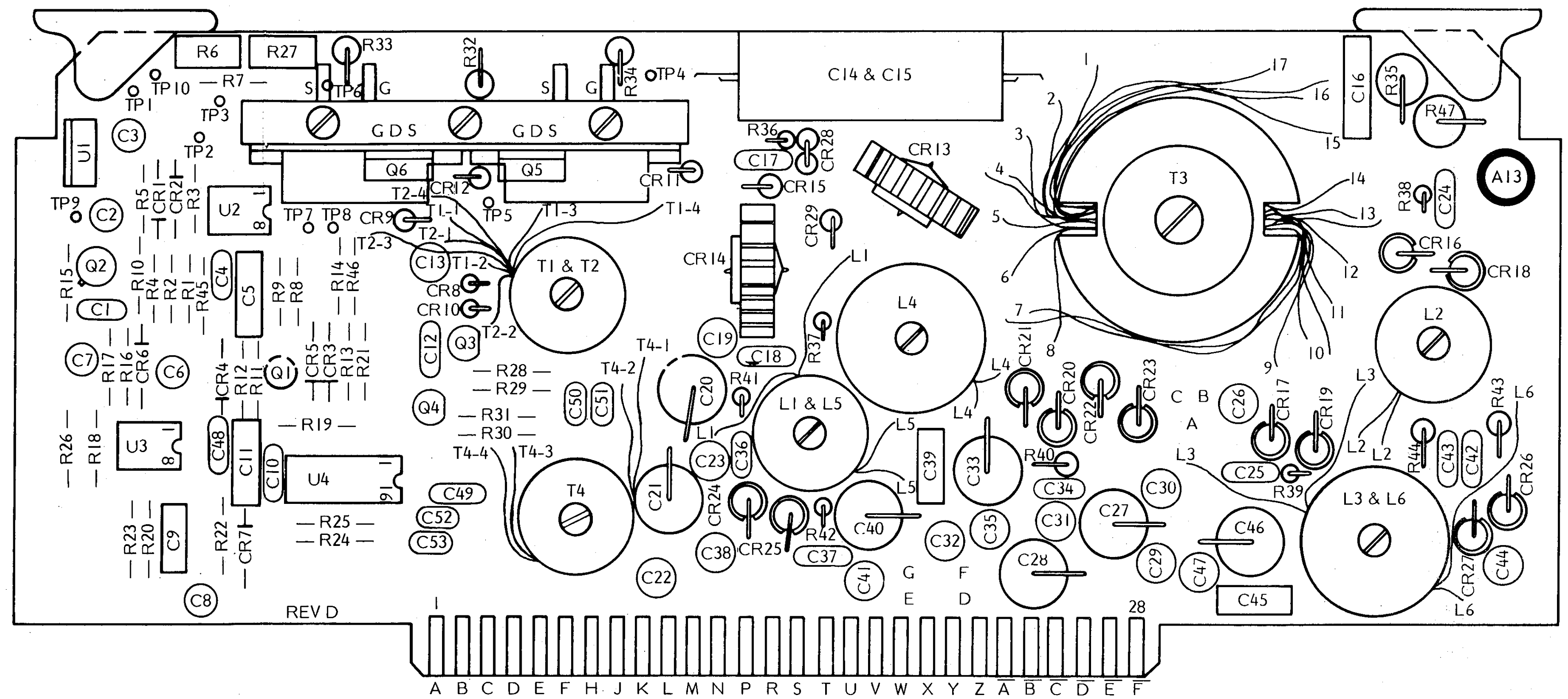
Part of A14 PCB



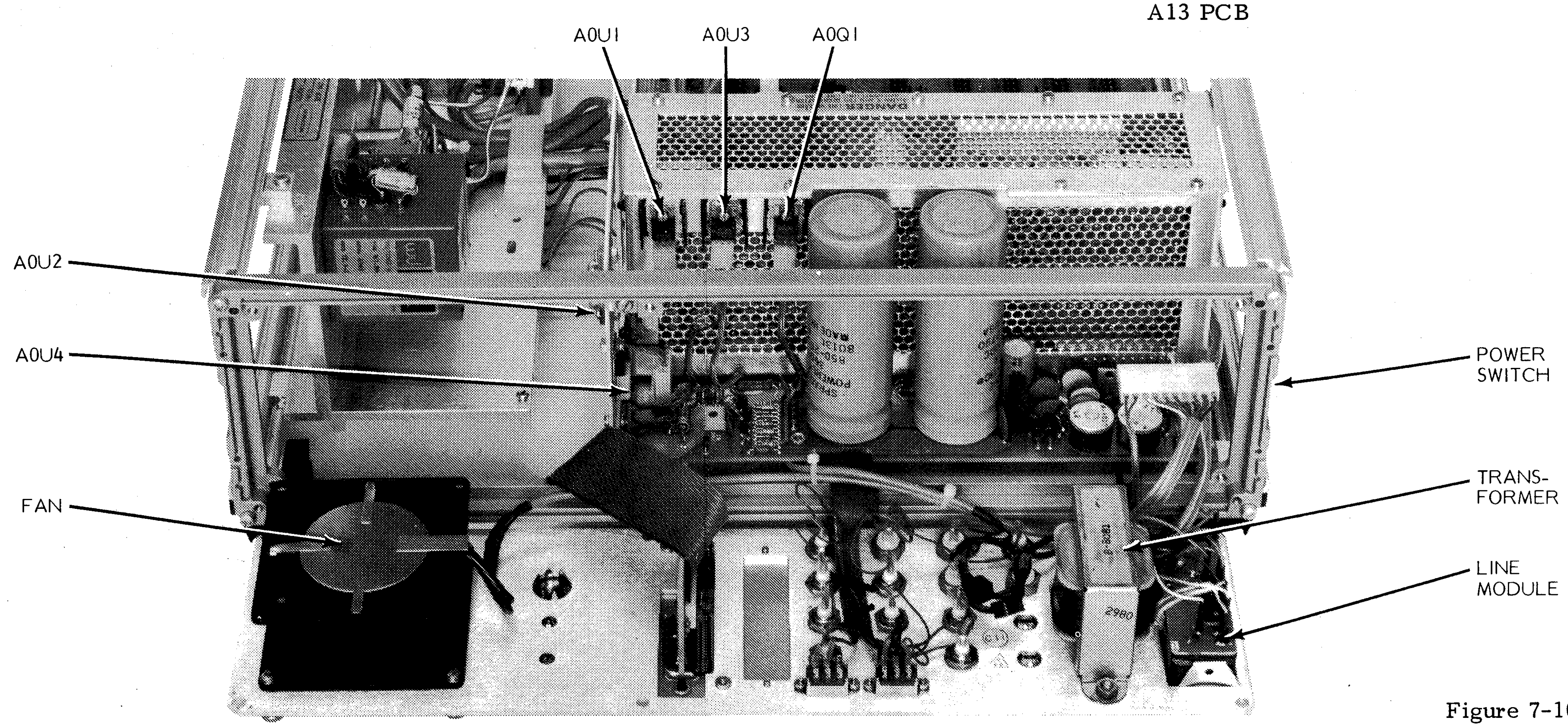


A16 Rear Panel



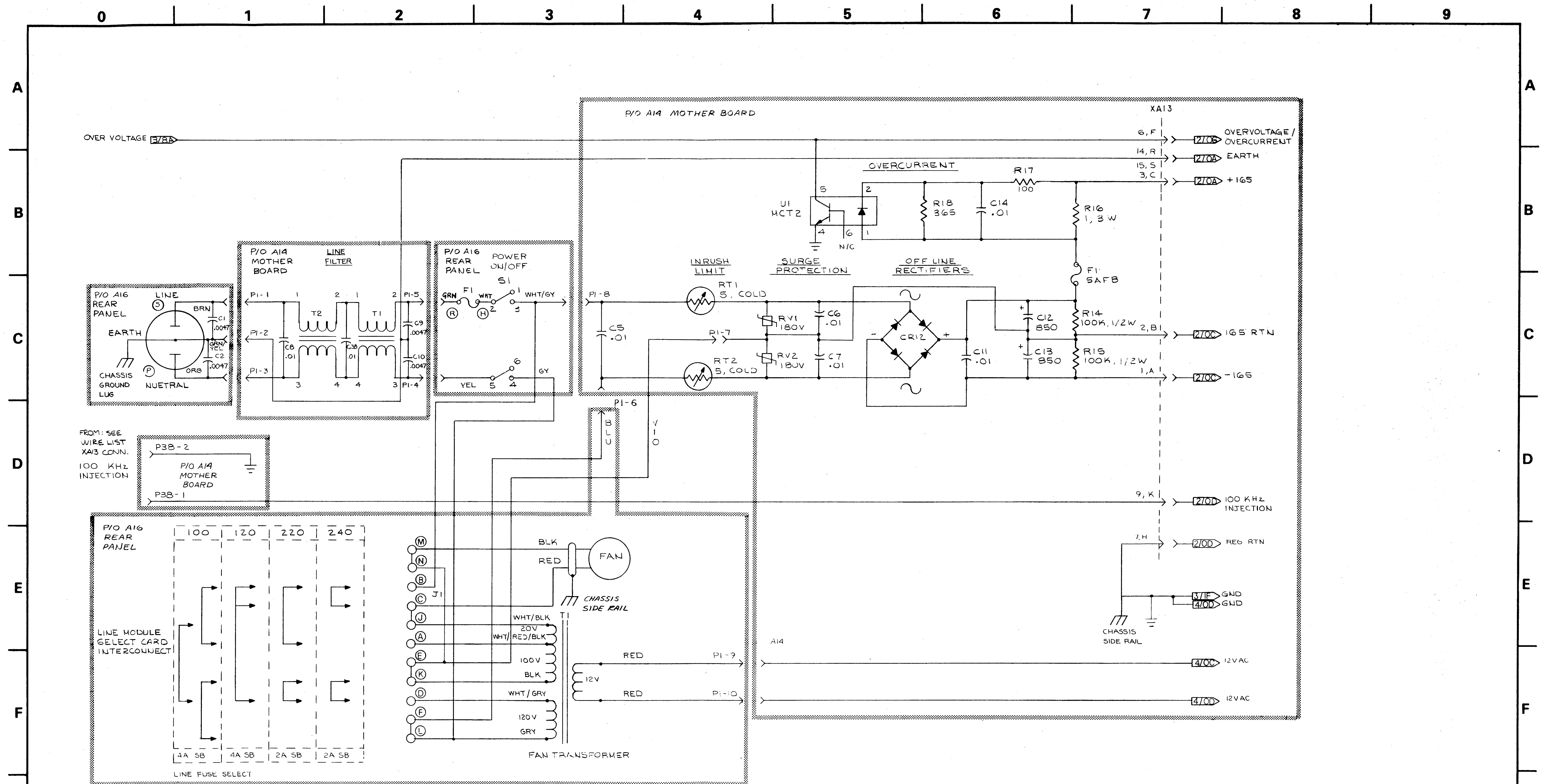


A13 PCB



A16 Rear Panel

Figure 7-107. A13/A14 Switching Power Supply, Parts Locator Diagram



NOTES

UNLESS OTHERWISE SPECIFIED, ALL CIRCUITRY SHOWN IS RESIDENT ON XA14

1. ① POLARITY SENSITIVE COMPONENTS. IF +12V IS REQUIRED THESE COMPONENTS WILL BE LOADED IN THE REVERSE DIRECTION.
2. Ⓐ DENOTES CONNECTIONS ON REAR PANEL LINE MODULE.
3. 3 DENOTES WIRE HOLE NUMBER FROM MOTHERBOARD XA14 TO VOLTAGE REGULATORS.
4. 2/3C> MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. DENOTES SCREWDRIVER ADJUST.
6. DENOTES GROUNDPLANE AREA.
7. ❼ DENOTES TEST POINTS
8. * REMOVE FOR TEST
9. DENOTES PRIMARY SIGNAL PATH.
10. DENOTES FEEDBACK SIGNAL PATH.
① DENOTES ISOLATED GND AND -V① DENOTES RELATIVE VOLTAGES.
11. /77 DENOTES CHASSIS GND.

Figure 7-108. A13/A14 Switching Power Supply Schematic (Sheet 1 of 4)

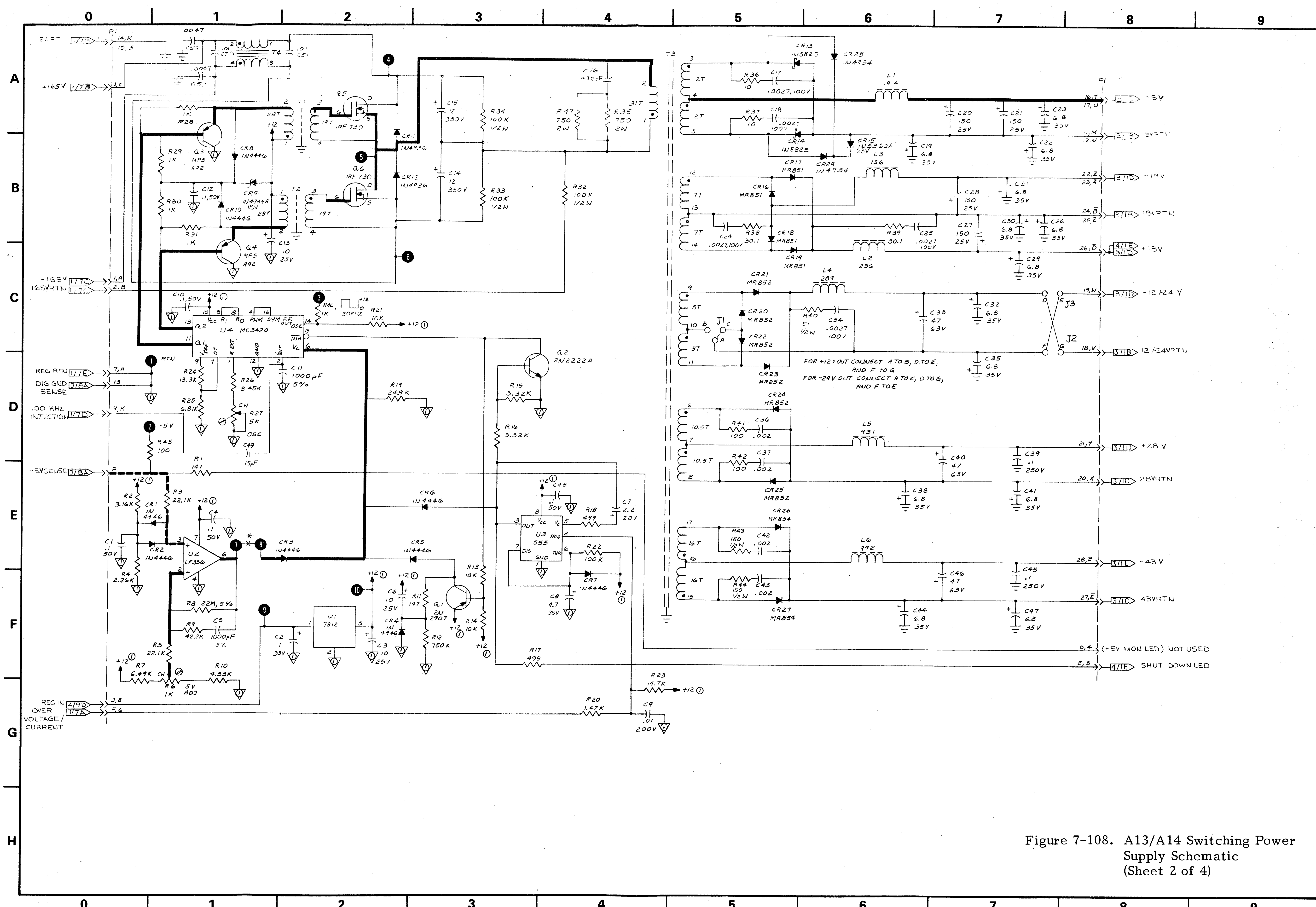


Figure 7-108. A13/A14 Switching Power Supply Schematic (Sheet 2 of 4)

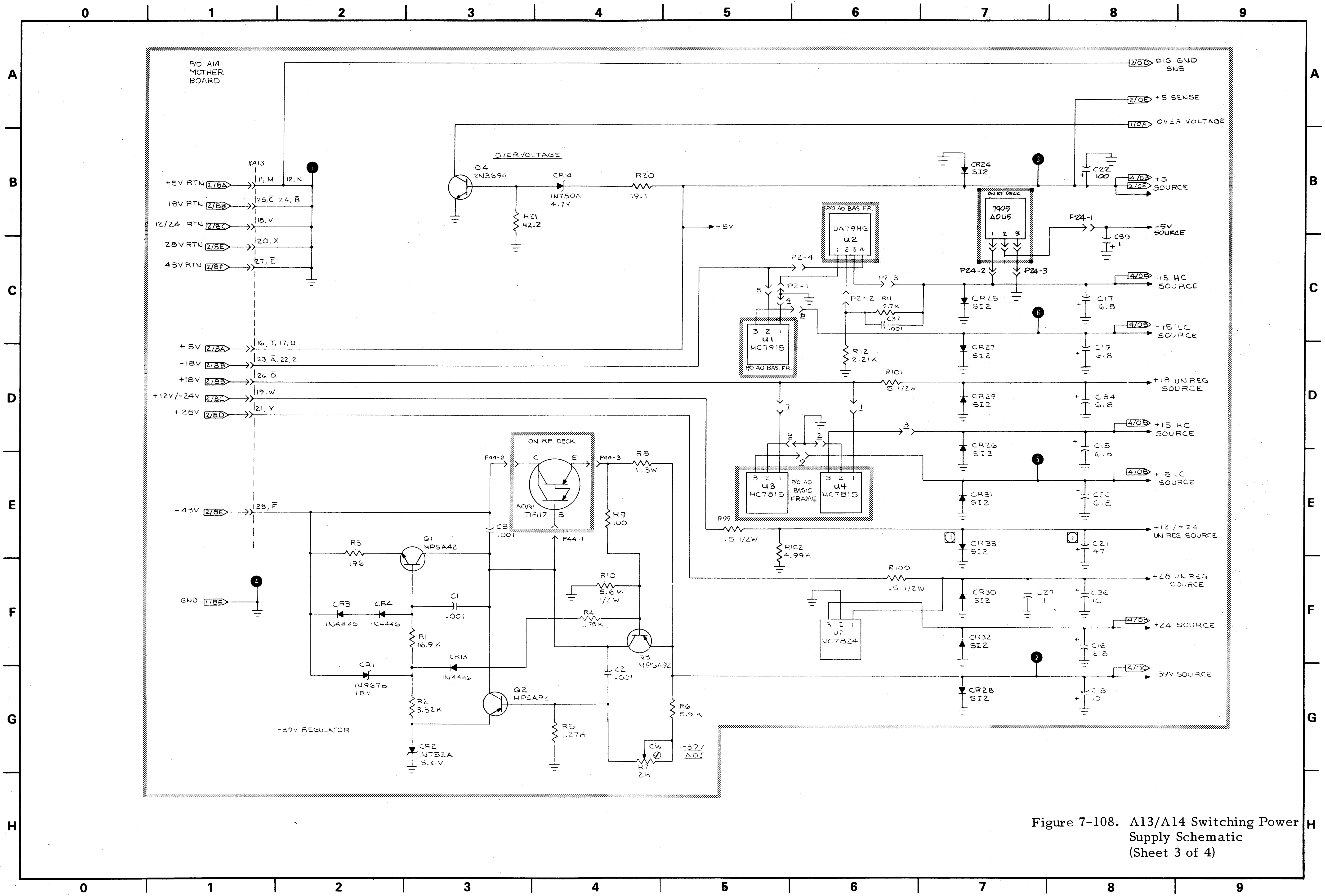


Figure 7-108. A13/A14 Switching Power Supply Schematic (Sheet 3 of 4)

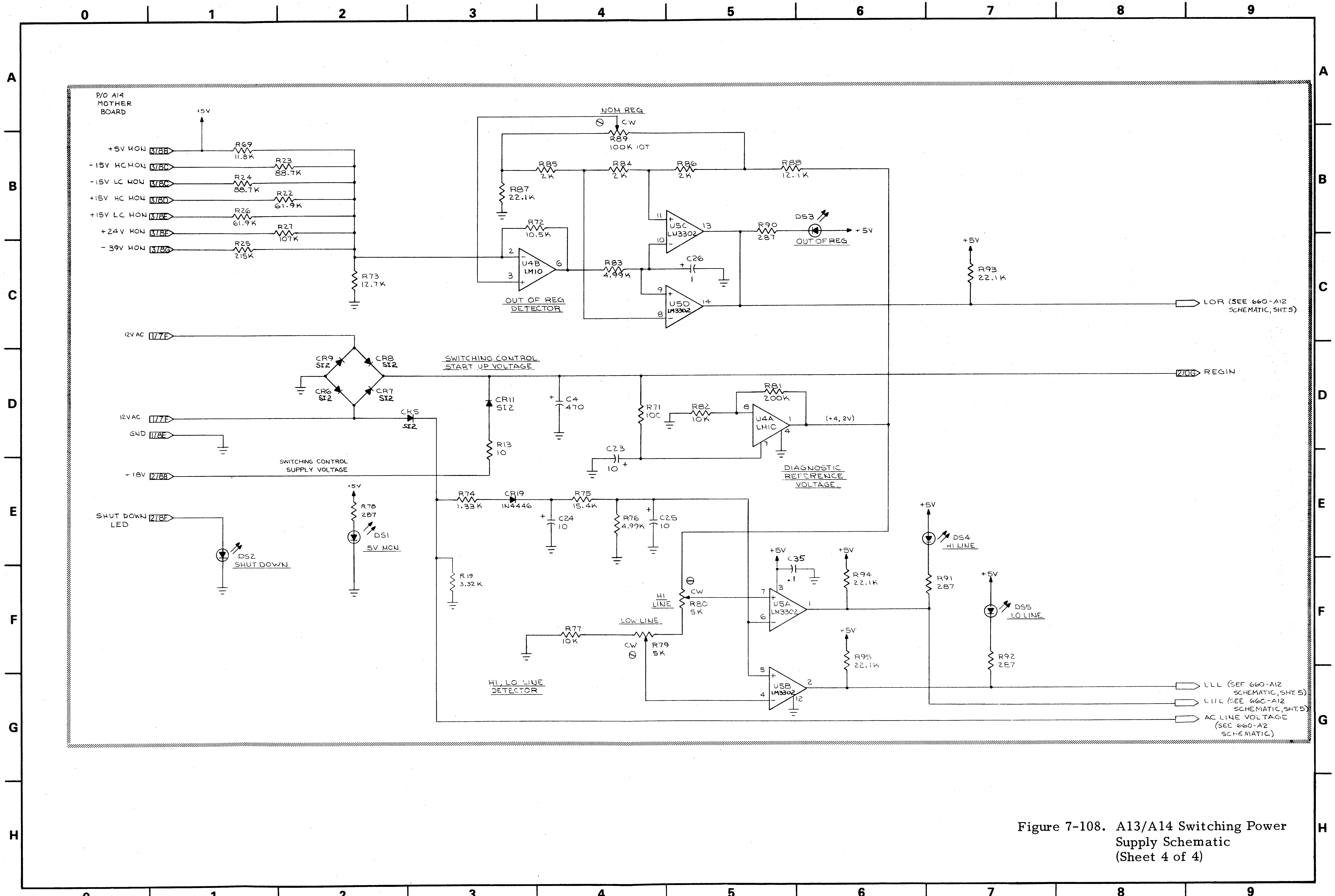


Figure 7-108. A13/A14 Switching Power Supply Schematic (Sheet 4 of 4)

7-15.2 A14 Motherboard PCB, Wire Lists and Service Data

The A14 Motherboard PCB provides the medium for connecting the A1-A10 and A13 PCBs with each other, with the A11 and A12 PCBs, with the RF Deck, and with the rear panel connectors and switches. The A14 PCB also contains three groups of circuits, as shown in Figure 7-109. These circuits are shown schematically with the PCB circuits to which they relate, as follows:

- Group I - Power Supply. Shown in the A13/A14 schematic, Figure 7-108.
- Group II - Linearizer ROM and Diagnostic (Self Test) Latch. Shown in the A12 PCB Schematic, Figure 7-15.
- Group III - YIG Oscillator, PIN Switching, and PIN Modulator Current Drive. Shown in the YIG Driver schematics, Figures 7-62 thru 7-82.

This paragraph contains the following service data:

- A tabulation of the A14 PCB connectors showing destinations for each (Table 7-19).
- A tabulation of the A14 PCB interconnections (wire lists) (Tables 7-20 thru 7-22).
- Diagrams that show YIG oscillator wiring (Figures 7-110 thru 7-124).
- A parts locator diagram for the A14 components (Figure 7-125).
- A schematic (Figure 7-126) showing the Osc 1 thru Osc 4 PIN Select and MOD Drive components located on the A14 PCB. These components are also individually shown on sheet 3 of the A6-A9 YIG Driver schematics.

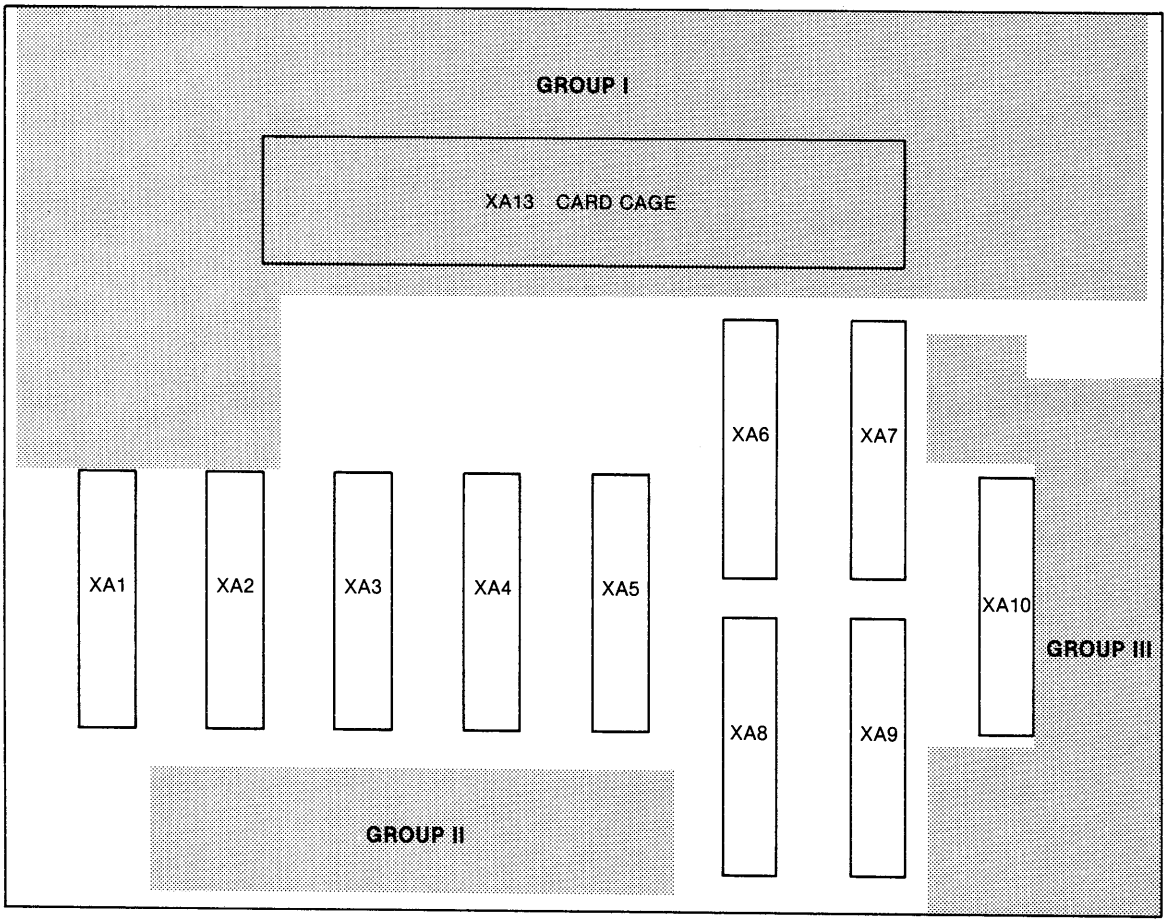


Figure 7-109. A14 Motherboard PCB, Circuit Groups

Table 7-19. A14 Connectors, Destinations

CONN. NO.	NO. OF PINS	DESTINATION
P1	10	Rear Panel - Line Voltage Selector Module
P2	4	-15V HC Regulator, A0U2
P3	26	No mate - Monitors bus for test purposes
P4	26	A18 GPIB Connector PCB
P5	26	Microprocessor - A12J5
P6	26	Microprocessor - A12J6
P7	26	Microprocessor - A12J7
P8	3	Not used
P10	4	Rear Panel - EXT AM INPUT and EXT SQ WAVE INPUT Connectors
P11	4	Not used
P12	5	Heterodyne Down Converter
P13	16	Osc 2 YIG
P14	16	Osc 1 YIG
P15	9	PIN Switch
P16	16	Osc 4 YIG (not used)
P17	16	Osc 3 YIG
P18	3	Transistor A6Q1
P19	3	Transistor A6Q2
P20	3	Transistor A6Q3
P21	3	Transistor A7Q1
P22	3	Transistor A7Q2
P23	3	Transistor A7Q3
P24	3	P13, P14, & A14C16
P25	3	Transistor A9Q1 (not used)
P26	3	Transistor A9Q2 (not used)
P27	3	Transistor A9Q3 (not used)
P28	3	Transistor A8Q1
P29	3	Transistor A8Q2
P30	3	Transistor A8Q3
P31	8	Step Attenuator (Option 2)
P33	2	Not used
P34	2	Rear Panel - EXT FM Ø LOCK INPUT Connector
P35	3	Heterodyne Down Converter Level Detector
P36	3	Coupler Level Detector
P37	2	Front Panel - EXTERNAL INPUT Connector
P38	2	Not used
XA1	56	A1 GPIB Interface PCB
XA2	56	A2 Ramp Generator PCB
XA3	56	A3 Marker Generator PCB
XA4	56	A4 Automatic Level Control PCB
XA5	56	A5 Frequency Instruction PCB
XA6	56	A6 HET/YIG Driver PCB
XA7	56	A7 YIG Driver PCB
XA8	56	A8 YIG Driver PCB
XA9	56	Not used
XA10	56	A10 FM/Attenuator PCB
XA13	56	A13 Switching Power Supply PCB
XA16	16	Rear Panel Connectors: • EXT SWEEP • SWEEP DWELL INPUT • SWEEP TRIGGER INPUT • BANDSWITCH BLANKING Switch • HORIZ OUTPUT DURING CW Switch • SEQ SYNC OUTPUT • MARKER OUTPUT • RETRACE BLANKING (+) • RETRACE BLANKING (-) • HORIZ OUTPUT • 1V/GHz • PENLIFT OUTPUT • BANDSWITCH BLANKING

Table 7-20. Power Supply Voltages, Distribution (XA-Numbered Connectors)

VOLTAGE	SOURCE	DESTINATION CONNECTOR AND PIN #, A14 BOARD									
		XA1	XA2	XA3	XA4	XA5	XA6	XA7	XA8	XA9	XA10
+5	XA13-16, 17, T, & U	14, R	14, R	14, R	14, R	14, R	11, M	11, M	11, M	11, M	6, F
+12/-24 (UNREG)	XA13-19						1	1	1	1	
+15	A0U3-3		11, M	11, M	11, M	11, M	8	8	8	8	
+15 HC	A0U4-3										24, A
-15	A0U1-3		12, N	12, N	12, N	12, N	9	9	9	9	
-15 HC	A0U2-3										23, B
+18 (UNREG)	XA13-26						B	B	B	B	
+24	A14U2-3										
+28 (UNREG)	XA13-21, Y										
-39V	A0Q1-Collector										

Table 7-21. Power Supply Voltages, Distribution (P-Numbered Connectors)

VOLTAGE	SOURCE	DESTINATION CONNECTOR AND PIN #, A14 BOARD													
		P3	P5	P6	P7	P12	P13	P14	P16	P17	P20	P23	P24	P27	P30
+5	XA13-16, 17, T, & U	26		25	16,17		15	15					1		
+12/-24 (UNREG)	XA13-19														
+15	A0U3-3		9												
+15 HC	A0U4-3					5	5	5	5	5					
-15	A0U1-3		8												
-15 HC	A0U2-3					3							2		
+18 (UNREG)	XA13-26														
+24	A14U2-3					2									
+28 (UNREG)	XA13-21, Y						4	4	4	4					
-39V	A0Q1-Collector										1	1		1	1

Table 7-22. Motherboard Wire List Connector Order

CONNECTOR & PIN NO.		SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P1	- 1	FILTERED AC LINE VOLTAGE (HOT)	VSM-S**	A14T2-1
	- 2	EARTH GROUND	VSM-GND	XA13-14, 15, R & S
	- 3	FILTERED AC LINE VOLTAGE (NEUTRAL)	VSM-P	A14T2-3
	- 4	AC LINE VOLTAGE (NEUTRAL)	A14T1-3	A0S1-5
	- 5	AC LINE VOLTAGE (HOT)	A14T1-2	VSM-R
	- 6	INPUT LINE VOLTAGE (NEUTRAL)	VSM-F	A14RT2
	- 7	165V RTN	VSM-E	XA13-2 & B
	- 8	INPUT LINE VOLTAGE (HOT)	A0S1-3	A14RT1
	- 9	12 VAC	A0T1-RED	A14CR9 - Cathode, A14CR8-Anode
	- 10	12 VAC	A0T1-RED	A14CR6 - Cathode, A14CR7 - Anode
P2	- 1	GROUND	A14 Ground Plane	A0U2-1
	- 2	CONTROL	A14R11/R12	A0U2-2
	- 3	-15V HC OUT	A0U2-3	A14CR14, 16, 21, 23, P12-3
	- 4	-18V IN	XA13-22, 23, Z, $\overline{A}$	A0U2-4
P3	- 1	SP13	P5-14	No mating connector. Used for monitoring Bus & SP lines
	- 2	SP11	P5-6	
	- 3	SP9	P5-7	
	- 4	SP 5	P5-22	
	- 5	SP 8	P5-12	
	- 6	SP 6	P7-6	
	- 7	SP 3	P7-7	
	- 8	SP 1	P7-8	
	- 9	µP LSB (BØ)	P6-9	
	- 10	µP B2	P6-8	
	- 11	µP B4	P6-7	
	- 12	µP B6	P6-6	
	- 13	DIGITAL GND	XA13-11, 12, M, N	
	- 14	SP14	P5-1	
	- 15	SP12	P5-19	
	- 16	SP10	P5-20	
	- 17	SP15	P5-11	
	- 18	SP7	P7-18	
	- 19	SP4	P7-19	
	- 20	SP2	P7-20	
	- 21	SPØ	P7-21	
	- 22	µP B1	P6-22	
	- 23	µP B3	P6-21	
	- 24	µP B5	P6-20	
	- 25	µP MSB (B7)	P6-19	
	- 26	+5V	XA13-16, 17, T, U	
P4	- 1	ADRS SW S3	A18J1-1	XA1-P
	- 2	ADRS SW S2	A18J1-2	XA1-N
	- 3	ADRS SW S1	A18J1-3	XA1-M
	- 4	LOGIC GND	A18J1-4	XA1-L
	- 5	DIO 4	A18J1-5	XA1-K
	- 6	DIO 1	A18J1-6	XA1-J
	- 7	DIO 2	A18J1-7	XA1-H
	- 8	DIO 3	A18J1-8	XA1-F
	- 9	EOI	A18J1-9	XA1-E
	- 10	SRQ	A18J1-10	XA1-D
	- 11	DAV	A18J1-11	XA1-C
	- 12	ATN	A18J1-12	XA1-B
	- 13	NRFD	A18J1-13	XA1-A
	- 14	ADRS SW S4	A18J1-14	XA1-13
	- 15	ADRS SW S5	A18J1-15	XA1-12
	- 16	CR/CR-LF	A18J1-16	XA1-11
	- 17	BUS GND	A18J1-17	XA1-10
	- 18	DIO 5	A18J1-18	XA1-9
	- 19	DIO 8	A18J1-19	XA1-8

* L = Low-Active State, H = High-Active State
**Line Voltage Selector Module

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- 20	$\overline{\text{DIO 7}}$	A18J1-20	XA1-7
- 21	$\overline{\text{DIO 6}}$	A18J1-21	XA1-6
- 22	BUS GND	A18J1-22	XA1-5
- 23	Not Used	A18J1-23	XA1-4
- 24	$\overline{\text{NDAC}}$	A18J1-24	XA1-3
- 25	$\overline{\text{IFC}}$	A18J1-25	XA1-2
- 26	$\overline{\text{REN}}$	A18J1-26	XA1-1
P5 - 1	SP14	A12P5-1	XA2-24, P3-14
- 2	H SWP	XA2-23	A12P5-2
- 3	SX4	A12P5-3	XA3-17
- 4	MODIFY SIGNAL	A12P5-4	XA3-U
- 5	M1 IDENTIFY	A12P5-5	XA3-21
- 6	SP11	A12P5-6	XA3-$\overline{A}$, P3-2
- 7	SP9	A12P5-7	XA3-$\overline{B}$, P3-3
- 8	-15V	A0U1-3	A12P5-8
- 9	+15V	A0U3-3	A12P5-9
- 10	ANALOG GND	A14 Ground Plane	A12P5-10
- 11	SP15	A12P5-11	XA4-20, P3-17
- 12	SP8	A12P5-12	XA4-21, P3-5
- 13	H UNLEVELED	XA4-22	A12P5-13
- 14	SP13	A12P5-14	XA2-$\overline{B}$, P3-1
- 15	L MODIFY CLEAR (SX29)	A12P5-15	XA3-16
- 16	L MODIFY/ACTIVE	XA3-19	A12P5-16
- 17	M2 IDENTIFY	A12P5-17	XA3-X
- 18	F0 IDENTIFY	A12P5-18	XA3-22
- 19	SP12	A12P5-19	XA3-23, P3-15
- 20	SP10	A12P5-20	XA3-24, P3-16
- 21	SX7	A12P5-21	A14U10-1
- 22	SP5	A12P5-22	A14U6-11, U9-13, P3-4
- 23	SX2	A12P5-23	A14U8-1
- 24	L EGD	XA4-17	A12P5-24
- 25	SX1	A12P5-25	A14U7-1
- 26	SXØ (Unused)	—	—
P6 - 1	L DOS	XA1-21	A12P6-1
- 2	L DOP (SP23)	A12P6-2	XA1-22
- 3	L KPS	XA1-23	A12P6-3
- 4	L GPIB RESET	A12P6-4	XA1-24
- 5	L KSV (SX3)	A12P6-5	XA1-$\overline{B}$
- 6	µP B6	A12P6-6	P3-12, A14U6-17, U7-16, U8-16, U10-16, XA1-$\overline{C}$, XA2-$\overline{C}$, XA3-$\overline{C}$, XA4-$\overline{C}$, XA5-$\overline{C}$
- 7	µP B4	A12P6-7	P3-11, A14U6-13, U7-12, U8-12, U10-12, XA1-$\overline{D}$, XA2-$\overline{D}$, XA3-$\overline{D}$, XA4-$\overline{D}$, XA5-$\overline{D}$
- 8	µP B2	A12P6-8	P3-10, A14U6-7, U7-6, U8-6, U10-6, XA1-$\overline{E}$, XA2-$\overline{E}$, XA3-$\overline{E}$, XA4-$\overline{E}$, XA5-$\overline{E}$
- 9	µP LSB (BØ)	A12P6-9	P3-9, A14U6-3, U7-2, U8-2, U10-2, XA1-$\overline{F}$, XA2-$\overline{F}$, XA3-$\overline{F}$, XA4-$\overline{F}$, XA5-$\overline{F}$
- 10	DIGITAL GND	XA13-11, 12, M, N	A12P6-10
- 11			A12P6-11
- 12	+5V	XA13-T, U, 16 and 17	A12P6-12
- 13			A12P6-13
- 14	TALK	XA1-20	A12P6-14
- 15	L LOCAL LOCKOUT	XA1-19	A12P6-15
- 16	SRQ	XA1-18	A12P6-16
- 17	L REMOTE	XA1-17	A12P6-17
- 18	LISTEN	XA1-16	A12P6-18

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- 19	μP MSB (B7)	A12P6-19	P3-25, A14U6-18, U7-19, U8-19, U10-19, XA1-25, XA2-25, XA3-25, XA4-25, XA5-25
- 20	μP B5	A12P6-20	P3-24, A14U6-14, U7-15, U8-15, U10-15, XA1-26, XA2-26, XA3-26, XA4-26, XA5-26
- 21	μP B3	A12P6-21	P3-23, A14U6-8, U7-9, U8-9, U10-9, XA1-27, XA2-27, XA3-27, XA4-27, XA5-27
- 22	μP B1	A12P6-22	P3-22, A14U6-4, U7-5, U8-5, U10-5, XA1-28, XA2-28, XA3-28, XA4-28, XA5-28
- 23 } - 24 }	DIGITAL GND	XA13-11, 12, M, N	{ A12P6-23 { A12P6-24
- 25 } - 26 }	+5V	{ XA13-T, U, 16 and 17	A12P6-25 A12P6-26
P7 - 1 } - 2 }	DIGITAL GND	XA13-11, 12, M, N	A12P7-1 A12P7-2
- 3 } - 4 }	+5V FOR A11 PCB	{ XA13-T, U, 16 and 17	A12P7-3 A12P7-4
- 5	MANUAL SWEEP	A12P7-5	XA5-17
- 6	SP6	A12P7-6	XA5-19, P3-6
- 7	SP3	A12P7-7	XA5-21, P3-7
- 8	SP1	A12P7-8	XA5-23, P3-8
- 9	Vacant		
- 10	Vacant		
- 11	Vacant		
- 12	RF SLOPE(S)	A12P7-12	XA4-U
- 13	+10V REF	XA5-S	A12P7-13
- 14 } - 15 }	DIGITAL GND	XA13-11, 12, M, N	{ A12P7-14 { A12P7-15
- 16 } - 17 }	+5V FOR A11 PCB	{ XA13-T, U, 16 and 17	{ A12P7-16 { A12P7-17
- 18	SP7	A12P7-18	XA5-18, P3-18
- 19	SP4	A12P7-19	XA5-20, P3-19
- 20	SP2	A12P7-20	XA5-22, P3-20
- 21	SPØ	A12P7-21	XA5-24, P3-21
- 22	MARKER AMPL(CW)	XA3-Z	A12P7-22
- 23	MARKER AMPL(S)	A12P7-23	XA3-Y
- 24	ANALOG GND	XA3-L	A12P7-24
- 25	ANALOG GND	A14 Ground Plane	A12P7-25
- 26	RF SLOPE (CW)	XA5-V	A12P7-26
P10 - 1	EXT SQ WAVE IN	EXT SQ WAVE INPUT	XA4-15
- 2	SHIELD LEAD	EXT SQ WAVE INPUT (SHIELD)	A14 ANALOG GROUND PLANE
- 3	EXT AM INPUT	EXT AM INPUT	XA4-16
- 4	ANALOG GROUND	EXT AM INPUT (SHIELD)	A14 ANALOG GROUND PLANE
P11	Not Used		
P12 - 1	+5V	XA13-16, 17, T, U	
- 2	+24V	A14U2-3	HDC +24V**
- 3	-15V HC	A0U2-3, P2-3	HDC -15V
- 4	ANALOG GND	A14 Ground Plane	HDC Ground
- 5	+15V HC	A0U4-3	HDC +15V**

*L=Low-Active State, H=High Active State.
**HDC=Heterodyne Down Converter

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.		SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P13	- 1	MOD DRIVER 2	XA7-K	No connection
	- 2	YIG 2 BIAS GND SENSE	YIG 2 OSC GND	XA7-N
	- 3	YIG 2 BIAS	P21-2	
	- 4	+28V	XA13-21, Y	
	- 5	+15V HC	AOU4-3	
	- 6	YIG 2 TUNING COIL (+)	XA7-T	
	- 7	YIG 2 TUNING COIL (-)	XA7-U	
	- 8	YIG 2 FILTER FM (-) COIL	XA10-16	
	- 9	YIG 2 FILTER FM COIL (+)	XA10-22	See Fig. 7-110 thru 7-124
	- 10	YIG 2 FM COIL (-) WJ	XA10-17	
	- 11	YIG 2 FM COIL (+) WJ	XA10-21	
	- 12	YIG 2 FM COIL (-) AVANTEK	XA10-18	
	- 13	YIG 2 FM COIL (+) AVANTEK	XA10-20	
	- 14	Vacant		
	- 15	-5V	P24-3	
	- 16	ANALOG GROUND	A14 Ground Plane	
P14	- 1	MOD DRIVER 1	XA6-K	BAND 1 MODULATOR
	- 2	YIG 1 BIAS GND SENSE	YIG 1 OSC GND	XA6-N
	- 3	YIG 1 BIAS	P18-2	
	- 4	+28V	XA13-21, Y	
	- 5	+15V HC	AOU4-3	
	- 6	YIG 1 TUNING COIL (+)	XA6-T	
	- 7	YIG 1 TUNING COIL (-)	XA6-U	
	- 8	YIG 1 FILTER FM COIL (-)	XA10-16	
	- 9	YIG 1 FILTER FM COIL (+)	XA10-22	See Fig. 7-110 thru 7-124
	- 10	YIG 1 FM COIL WJ (-)	XA10-17	
	- 11	YIG 1 FM COIL (+) WJ	XA10-21	
	- 12	YIG 1 FM COIL AVANTEK (-)	XA10-18	
	- 13	FM COIL, AVANTEK (+)	XA10-20	
	- 14	Vacant		
	- 15	-5V	P24-3	
	- 16	ANALOG GROUND	A14 Ground Plane	
P15	- 1	.01-8 GHz PIN PORT SEL	A14R105	Not Used
	- 2	HET PORT SELECT	A14R107	PIN Switch Het Port
	- 3	PIN PORT 1 SEL	A14R108	PIN Switch Port 1
	- 4	PIN PORT 2 SEL	A14Q13-E	PIN Switch Port 2
	- 5	PIN PORT 3 SEL	A14Q14-E	PIN Switch Port 3
	- 6	PIN PORT 4 SEL	A14Q17-E	PIN Switch Port 4
	- 7	PIN PORT 1 MOD	XA6-K, via A14R34	No connection
	- 8	PIN PORT 2 MOD	XA7-K, via A14R37	PIN Switch Mod Port 2
	- 9	PIN PORT 3 MOD	XA8-K, via A14R50	PIN Switch Mod Port 3
	- 10	PIN PORT 4 MOD	XA9-K, via A14R68	PIN Switch Mod Port 4
P16		Not Used		
P17	- 1	MOD DRIVER 3	XA8-K	No connection
	- 2	YIG 3 BIAS GND SENSE	YIG 3 OSC GND	XA8-N
	- 3	YIG 3 BIAS	P28-2	
	- 4	+28V	XA13-21, Y	
	- 5	+15V HC	AOU4-3	
	- 6	YIG 3 TUNING COIL (+)	XA8-T	
	- 7	YIG 3 TUNING COIL (-)	XA8-U	
	- 8	YIG 3 FILTER FM COIL (-)	XA10-16	See Fig. 7-110 thru 7-124
	- 9	YIG 3 FILTER FM COIL (+)	XA10-22	
	- 10	YIG 3 FM COIL (-) WJ	XA10-17	
	- 11	YIG 3 FM COIL (+) WJ	XA10-21	
	- 12	YIG 3 FM COIL (-) AVANTEK	XA10-18	
	- 13	YIG 3 FM COIL (+) AVANTEK	XA10-20	
	- 14	Vacant		
	- 15	Vacant		
	- 16	Vacant		
P18	- 1	A6Q1-E	XA6-P	A6Q1-E

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P18 - 2	A6Q1-C	A6Q1-C	P14-3 & XA6-R
- 3	A6Q1-B	XA6-S	A6Q1-B
P19 - 1	A6Q2-E	CR15 & P20-2	A6Q2-E
- 2	A6Q2-C	A6Q2-C	P14-7 & XA6-U
- 3	A6Q2-B	XA6-V	A6Q2-B
P20 - 1	A6Q3-E	-38V	A6Q3-E
- 2	A6Q3-C	A6Q3-C	P19-1
- 3	A6Q3-B	XA6-W	A6Q3-B
P21 - 1	A7Q1-E	XA7-P	A7Q1-E
- 2	A7Q1-C	A7Q1-C	P13-3 & XA7-R
- 3	A7Q1-B	XA7-S	A7Q1-B
P22 - 1	A7Q2-E	CR16 & P23-2	A7Q2-E
- 2	A7Q2-C	A7Q2-C	P13-7 & XA7-U
- 3	A7Q2-B	XA7-V	A7Q2-B
P23 - 1	A7Q3-E	-38V	A7Q3-E
- 2	A7Q3-C	A7Q3-C	P22-1
- 3	A7Q3-B	XA7-W	A7Q3-B
P24 - 1	GROUND	A14 Ground Plane	AOU5-1
- 2	-15V HC	P2-3	AOU5-2
- 3	-5V	AOU5-3	P13-15 & P14-15
P25 - 1	A9Q1-E	XA9-P	A9Q1-E
- 2	A9Q1-C	A9Q1-C	P16-3 & XA9-R
- 3	A9Q1-B	XA9-S	A9Q1-B
P26 - 1	A9Q2-E	CR23 & P27-2	A9Q2-E
- 2	A9Q2-C	A9Q2-C	XA9-U & P16-7
- 3	A9Q2-B	XA9-V	A9Q2-B
P27 - 1	A9Q3-E (-38V)	-38V	A9Q3-E
- 2	A9Q3-C	A9Q3-C	P26-1
- 3	A9Q3-B	XA9-W	A9Q3-B
P28 - 1	A8Q1-E	XA8-P	A8Q1-E
- 2	A8Q1-C	A8Q1-C	P17-3 & XA8-R
- 3	A8Q1-B	XA8-S	A8Q1-B
P29 - 1	A8Q2-E	CR21 & P30-2	A8Q2-E
- 2	A8Q2-C	A8Q2-C	XA8-U
- 3	A8Q2-B	XA8-V	A8Q2-B
P30 - 1	A8Q3-E (-38V)	-38V	A8Q3-E
- 2	A8Q3-C	A8Q3-C	P29-1
- 3	A8Q3-B	XA8-W	A8Q3-B
P31 - 1	L 10DB ATTN DRVR (YELLOW)	XA10-15	Option 2 70 dB Step Attenuator
- 2	H 10 DB ATTN DRVR (PURPLE)	XA10-14	
- 3	HB 40DB ATTN DRVR (WHITE)	XA10-13	
- 4	LB 40DB ATTN DRVR (BROWN)	XA10-12	
- 5	LA 40DB ATTN DRVR (BLUE)	XA10-11	
- 6	HA 40DB ATTN DRVR (ORANGE)	XA10-10	
- 7	L 20DB ATTN DRVR (GREEN)	XA10-9	
- 8	H 20DB ATTN DRVR (BLACK)	XA10-8	
- 9	ATTENUATOR SUPPLY	XA10-N	

* L = Low-Active State, H = High-Active State

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P33	Not Used		
P34 -1	EXT FM INPUT	EXT FM Ø LOCK INPUT (Rear Panel Connector)	XA10-S
-2	GROUND		XA10-V
P35 -1	.01-2GHz DETECTOR IN	.01-2 GHz LEVEL DETECTOR	XA4-2
-2	.01-2GHz DETECTOR RTN		XA4-1
-3	.01-2GHz THERMISTOR		XA4-A
P36 -1	2-18GHz DETECTOR IN	2-18 GHz LEVEL DETECTOR	XA4-B
-2	2-18GHz DETECTOR RTN		XA4-3
-3	2-18GHz THERMISTOR		XA4-C
P37 -1	EXT DET IN	EXTERNAL DETECTOR INPUT (Front Panel Connector)	XA4-4
-2	EXT DET RTN		XA4-D
P39 -1	EXT ALC GAIN (CCW)	EXT ALC GAIN Potentiometer	XA4-E
-2	EXT ALC GAIN (S)		XA4-F
-3	EXT ALC GAIN (CW)		XA4-J
P40 -1	EXT SWEEP RTN	EXT SWEEP INPUT CONN (rear panel)	A14R109
-2	EXT SWEEP INPUT		A14R110
-3	A14 Ground Plane	External Sweep Cable Shield	A14 Ground Plane
P41 -1	V/GHz RTN	XA5-$\overline{\text{B}}$	V/GHz CONN (Rear Panel)
-2	V/GHz OUTPUT	XA5-9	
-3	A14 Ground Plane	V/GHz Cable Shield	A14 Ground Plane
P42 -1	HORIZONTAL OUT RTN	A14R113	HORIZ OUTPUT CONN (Rear Panel)
-2	HORIZONTAL OUT RTN	A14U12-6	
-3	A14 Ground	HORIZONTAL OUT Cable Shield	A14 Ground Plane
P43 -1	FREQ OFFSET IN RTN	AUX I/O-24	XA5-3
-2	FREQ OFFSET IN	AUX I/O-12	XA5-2
-3	A14 Ground Plane	Freq Offset In Cable Shield	A14 Ground Plane
P44 -1	A0Q1-B	A14Q2-C	A0Q1-B
-2	A0Q1-C	XA13-28, $\overline{\text{F}}$	A0Q1-C
-3	A9Q1-E	A0Q1-E	A14R8
XA1 -1	$\overline{\text{REN}}$	P4-26	A1P1-1
-2	$\overline{\text{IFC}}$	P4-25	A1P1-2
-3	NDAC	P4-24	A1P1-3
-4	Not Used	P4-23	A1P1-4
-5	$\overline{\text{BUS}}$ GND	P4-22	A1P1-5
-6	$\overline{\text{DIO6}}$	P4-21	A1P1-6
-7	$\overline{\text{DIO7}}$	P4-20	A1P1-7
-8	$\overline{\text{DIO8}}$	P4-19	A1P1-8
-9	DIO5	P4-18	A1P1-9
-10	BUS GND	P4-17	A1P1-10
-11	CR/CR-LF	P4-16	A1P1-11
-12	ADRS SW S5	P4-15	A1P1-12
-13	ADRS SW S4	P4-14	A1P1-13
-14	+5V	XA13-T, U, 16, 17	A1P1-14
-15	+5V RETURN	A14 Ground Plane	A1P1-15
-16	L LISTEN	A1P1-16	P6-18

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- 17	L REMOTE	A1P1-17	P6-17
- 18	L SRQ	A1P1-18	P6-16
- 19	L LOCAL LOCKOUT	A1P1-19	P6-15
- 20	L TALK	A1P1-20	P6-14
- 21	L DOS	A1P1-21	P6-1
- 22	L DOP	A1P1-22	P6-2
- 23	L KPS	A1P1-23	P6-3
- 24	L GPIB RESET	A1P1-24	P6-4
- 25	μP MSB (B7)	P6-19	A1P1-25
- 26	μP B5	P6-20	A1P1-26
- 27	μP B3	P6-21	A1P1-27
- 28	μP B1	P6-22	A1P1-28
- A	NRFD	P4-13	A1P1-A
- B	ATN	P4-12	A1P1-B
- C	DAV	P4-11	A1P1-C
- D	SRQ	P4-10	A1P1-D
- E	EOI	P4-9	A1P1-E
- F	DIO3	P4-8	A1P1-F
- H	DIO2	P4-7	A1P1-H
- J	DIO1	P4-6	A1P1-J
- K	DIO4	P4-5	A1P1-K
- L	LOGIC GND	P4-4	A1P1-L
- M	ADRS SW S1	P4-3	A1P1-M
- N	ADRS SW S2	P4-2	A1P1-N
- P	ADRS SW S3	P4-1	A1P1-P
- R	+5V	XA13-T, U, 16, 17	A1P1-R
- S	+5V RETURN	A14 Ground Plane	A1P1-S
- T	H SEQ	XA2-16	A1P1-T
- U	L DWELL (LD)	A1P1-U	XA2-17
- V	L RETRACE BLANKING	XA2-18	A1P1-V
- W	Vacant		A1P1-W
- X	H INTENSITY MARKER	XA2-20	A1P1-X
- Y	Vacant		A1P1-Y
- Z	GPIB IN	A1P1-Z	A14U10-18
- A	H UNLC	XA4-22	A1P1-A
- B	L KSV (SX3)	P6-5	A1P1-B
- C	μP B6	P6-6	A1P1-C
- D	μP B4	P6-7	A1P1-D
- E	μP B2	P6-8	A1P1-E
- F	μP LSB BØ	P6-9	A1P1-F
XA2 - 1	Vacant		A2P1-1
- 2	BANDSWITCH BLANKING +	A2P1-2	XA16-5
- 3	BANDSWITCH BLANKING -	A2P1-3	XA16-12
- 4	RETRACE BLANKING (-)	A2P1-4	XA16-14
- 5	RETRACE BLANKING (+)	A2P1-5	XA16-9
- 6	H SEQ SYNC	A2P1-6	XA16-7
- 7	Vacant		A2P1-7
- 8	Vacant		A2P1-8
- 9	ANALOG GND	A14 Ground Plane	A2P1-9
- 10	ANALOG GND	A14 Ground Plane	A2P1-10
- 11	+15V	A0U3-3	A2P1-11
- 12	-15V	A0U1-3	A2P1-12
- 13	DIGITAL GND	A14 Ground Plane	A2P1-13
- 14	+5V	XA13-T, U, 16, 17	A2P1-14
- 15	L DWELL DETECTED	A2P1-15	A14U10-14
- 16	H SEQ	A2P1-16	XA1-T
- 17	L DWELL (LD)	XA1-U	A2P1-17
- 18	L RETRACE BLANKING	A2P1-18	XA1-V, XA3-18, V & XA4-18
- 19	H RF ON DURING RETRACE	XA4-Y	A2P1-19
- 20	H INTENSITY MARKER	XA3-20	A2P1-20
- 21	H DWELL	A2P1-21	A14U8-3
- 22	Vacant		A2P1-22
- 23	H SWP	A2P1-23	P5-2

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- 24	SP14	P5-1	A2P1-24
- 25	µP MSB (B7)	P6-19	A2P1-25
- 26	µP B5	P6-20	A2P1-26
- 27	µP B3	P6-21	A2P1-27
- 28	µP B1	P6-22	A2P1-28
- A	AC LINE VOLTAGE	A14CR5-Cathode	A2P1-A
- B	EXT RAMP IN	A14U11-6	A2P1-B
- C	Vacant		A2P1-C
- D	L EXT DWELL	XA16-3	A2P1-D
- E	L EXT TRIG PULSE IN	XA16-4	A2P1-E
- F	Vacant		A2P1-F
- H	L ACTIVATE RELAY	A2P1-H	A14K1, XA16-1
- J	Vacant		A2P1-J
- K	ANALOG GND	A14 Ground Plane	A2P1-K
- L	ANALOG GND	A14 Ground Plane	A2P1-L
- M	+15V	A0U3-3	A2P1-M
- N	-15V	A0U1-3	A2P1-N
- P	DIGITAL GND	A14 Ground Plane	A2P1-P
- R	+5V	XA13-T, U, 16, 17	A2P1-R
- S	Vacant		A2P1-S
- T	RAMP OUTPUT	A2P1-T	XA5-16
- U	Vacant		A2P1-U
- V	L RETRACE BLANKING	A2P1-V	XA1-V; XA3-18, V; XA4-18,
- W	L LEVEL DIP	A2P1-W	XA4-W
- X	H INTENSITY MARKER	XA3-20	A2P1-X, 20; A14U9-11
- Y	H EXT FM ENABLE	A2P1-Y	XA10-5
- $\underline{Z}$	L EOB	XA10-$\underline{E}$	A2P1-Z
- $\overline{A}$	L MARKER OCCURRED	A2P1-$\overline{A}$	XA16-16
- $\overline{B}$	SP13	P5-14	A2P1-$\overline{B}$
- $\overline{C}$	µP B6	P6-6	A2P1-$\overline{C}$
- $\overline{D}$	µP B4	P6-7	A2P1-$\overline{D}$
- $\overline{E}$	µP B2	P6-8	A2P1-$\overline{E}$
- $\overline{F}$	µP LSB (BØ)	P6-9	A2P1-$\overline{F}$
XA3 - 1	Vacant		A3P1-1
- 2	Vacant		A3P1-2
- 3	Vacant		A3P1-3
- 4	Vacant		A3P1-4
- 5	Vacant		A3P1-5
- 6	Vacant		A3P1-6
- 7	Vacant		A3P1-7
- 8	VIDEO MARKER	A3P1-8	XA16-8
- 9	ANALOG GND	A14 Ground Plane	A3P1-9
- 10	ANALOG GND	A14 Ground Plane	A3P1-10
- 11	+15V	A0U3-3	A3P1-11
- 12	-15V	A0U1-3	A3P1-12
- 13	DIGITAL GND	A14 Ground Plane	A3P1-13
- 14	+5V	XA13-T, U, 16, 17	A3P1-14
- 15	L ALTERNATE A	XA16-6	A3P1-15
- 16	L MODIFY CLEAR (SX29)	P5-15	A3P1-16
- 17	SX4	P5-3	A3P1-17
- 18	L RETRACE BLANKING	XA2-V,18	A3P1-18
- 19	L MODIFY ACTIVE	A3P1-19	P5-16
- 20	H INTENSITY MARKER	A3P1-20	XA2-X, XA2-20
- 21	L M1 IDENTIFY	P5-5	A3P1-21
- 22	L F0 IDENTIFY	P5-18	A3P1-22
- 23	SP12	P5-19	A3P1-23
- 24	SP10	P5-20	A3P1-24
- 25	µP MSB (B7)	P6-19	A3P1-25
- 26	µP B5	P6-20	A3P1-26
- 27	µP B3	P6-21	A3P1-27
- 28	µP B1	P6-22	A3P1-28
- A	Vacant		A3P1-A
- B	Vacant		A3P1-B
- C	Vacant		A3P1-C

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
-D	Vacant		A3P1-D
-E	Vacant		A3P1-E
-F	Vacant		A3P1-F
-H	Vacant		A3P1-H
-J	Vacant		XA16-10
-K	ANALOG GND	A14 Ground Plane	A3P1-K
-L	ANALOG GND	A14 Ground Plane	A3P1-L
-M	+15V	A0U3-3	A3P1-M
-N	-15V	A0U1-3	A3P1-N
-P	DIGITAL GND	A14 Ground Plane	A3P1-P
-R	+5V	XA13-T, U, 16, 17	A3P1-R
-S	L ALTERNATE ENABLE	XA16-11	A3P1-S
-T	RAMP, 0-10V	A3P1-T	XA5-15
-U	MODIFY SIGNAL	P5-4	A3P1-U
-V	L RETRACE BLANKING	A3P1-V	XA4-18
-W	RF MARKER	A3P1-W	XA4-19
-X	L M2 IDENTIFY	P5-17	A3P1-X
-Y	MARKER AMPL(S)	P7-23	A3P1-Y
-Z̲	MARKER AMPL(CW)	P7-22	A3P1-Z̲
-A̅	SP11	P5-6	A3P1-A̅
-B̅	SP9	P5-7	A3P1-B̅
-C̅	μP B6	P6-6	A3P1-C̅
-D̅	μP B4	P6-7	A3P1-D̅
-E̅	μP B2	P6-8	A3P1-E̅
-F̅	μP LSB (BØ)	P6-9	A3P1-F̅
XA4 -1	.01-2GHZ DETECTOR RTN	P35-2	A4P1-1
-2	.01-2GHZ THERMISTOR	P35-3	A4P1-2
-3	2-18GHZ DETECTOR RTN	P36-2	A4P1-3
-4	EXT DET RTN	P37-2	A4P1-4
-5	Vacant		A4P1-5
-6	Vacant		A4P1-6
-7	H RETRACE BLANKING	XA16-10	A4P1-7
-8	L CW MODE	XA5-8	A4P1-8, XA16-13
-9	ANALOG GND	A14 Ground Plane	A4P1-9
-10	ANALOG GND	A14 Ground Plane	A4P1-10
-11	+15V	A0U3-3	A4P1-11
-12	-15V	A0U1-3	A4P1-12
-13	DIGITAL GND	A14 Ground Plane	A4P1-13
-14	+5V	XA13-T, U, 16, 17	A4P1-14
-15	EXT SQ WAVE IN	P10-1	A4P1-15
-16	EXT AM INPUT	P10-3	A4P1-16
-17	L EGD	A4P1-17	P5-24
-18	L RETRACE BLANKING	XA2-18,V, XA13-18, V	A4P1-18
-19	RF MARKER	XA3-W	A4P1-19
-20	SP15	P5-11	A4P1-20
-21	SP8	P5-12	A4P1-21
-22	H UNLEVELED	A4P1-22	P5-13
-23	H ATTN 3	A4P1-23	XA10-2
-24	H ATTN 1	A4P1-24	XA10-1
-25	μP MSB (B7)	P6-19	A4P1-25
-26	μP B5	P6-20	A4P1-26
-27	μP B3	P6-21	A4P1-27
-28	μP B1	P6-22	A4P1-28
-A	.01-2GHZ DETECTOR IN	P35-1	A4P1-A
-B	2-18GHZ THERMISTOR	P36-3	A4P1-B
-C	2-18GHZ DETECTOR IN	P36-1	A4P1-C
-D	EXT DET IN	P37-1	A4P1-D
-E	ANALOG GND	A14 Ground Plane	A4P1-E
-F	EXT ALC GAIN (CW)	P39-3	A4P1-F
-H	EXT ALC GAIN (S)	P39-2	A4P1-H
-J	EXT ALC GAIN (CCW)	P39-1	A4P1-J
-K	ANALOG GND	A14 Ground Plane	A4P1-K
-L	ANALOG GND	A14 Ground Plane	A4P1-L
-M	+15V	A0U3-3	A4P1-M
-N	-15V	A0U1-3	A4P1-N

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
-P	DIGITAL GND	A14 Ground Plane	A4P1-P
-R	+5V	XA13-T, U, 16, 17	A4P1-R
-S	PIN MOD DRIVER	A4P1-S	XA6-7, XA7-7, XA8-7 XA9-7
-T	INT. RF SLOPE	XA5-V	A4P1-T
-U	RF SLOPE (Front Panel)	P7-12	A4P1-U
-V	L RF OFF	A4P1-V	XA6-5, XA7-5, XA8-5 & XA9-5
-W	L LEVEL DIP	XA2-W	A4P1-W
-X	L PIN SW OFF	A4P1-X	XA6-6, XA7-6, XA8-6 & XA9-6
-Y	H RF ON DURING RETRACE	XA2-19	A4P1-Y
-Z	L HET YIG SEL	XA6-H/XA7-H	A4P1-Z
-$\overline{A}$	H ATTN 4	A4P1-$\overline{A}$	XA10-B
-$\overline{B}$	H ATTN 2	A4P1-$\overline{B}$	XA10-A
-$\overline{C}$	μP B6	P6-6	A4P1-$\overline{C}$
-$\overline{D}$	μP B4	P6-7	A4P1-$\overline{D}$
-$\overline{E}$	μP B2	P6-8	A4P1-$\overline{E}$
-$\overline{F}$	μP LSB (B∅)	P6-9	A4P1-$\overline{F}$
XA5 -1	+24V	A14U2-3	A5P1-1
-2	FREQ OFFSET IN	P43-2	A5P1-2
-3	FREQ OFFSET RTN	P43-1	A5P1-3
-4	L HET YIG SELECT	XA6-H, XA7-H	A5P1-4, A14U8-18
-5	L PIN SELECT 1	XA6-A	A5P1-5, A14U7-3
-6	L YIG 2 SELECT	XA7-E	A5P1-6, A14U7-4
-7	L YIG 3 SELECT	XA8-E	A5P1-7, A14U7-7
-8	L CW MODE	A5P1-8	XA4-8
-9	V/GHZ OUTPUT	A5P1-9	P41-2
-10	ANALOG GND	A14 Ground Plane	A5P1-10
-11	+15V	A0U3-3	A5P1-11
-12	-15V	A0U1-3	A5P1-12
-13	DIGITAL GND	A14 Ground Plane	A5P1-13
-14	+5V	XA13-T, U, 16, 17	A5P1-14
-15	RAMP OUT	A5P1-15	XA3-T, A14R115
-16	RAMP INPUT	XA2-T	A5P1-16
-17	MAN SWEEP INPUT	P7-5	A5P1-17
-18	SP7	P7-18	A5P1-18
-19	SP6	P7-6	A5P1-19
-20	SP4	P7-19	A5P1-20
-21	SP3	P7-7	A5P1-21
-22	SP2	P7-20	A5P1-22
-23	SP1	P7-8	A5P1-23
-24	SP0	P7-21	A5P1-24
-25	μP MSB (B7)	P6-19	A5P1-25
-26	μP B5	P6-20	A5P1-26
-27	μP B3	P6-21	A5P1-27
-28	μP B1	P6-22	A5P1-28
-A	FC B2	{ XA6-Y, XA7-Y, XA8-Y or XA9-Y	A5P1-A
-B	FC B3	{ XA6-Z, XA7-Z XA8-Z or XA9-Z	A5P1-B
-C	FC B∅	{ XA6-$\overline{A}$, XA7-$\overline{A}$, XA8-$\overline{A}$, XA9-$\overline{A}$	A5P1-C
-D	FC B1	{ XA6-$\overline{B}$, XA7-$\overline{B}$ XA8-$\overline{B}$, XA9-$\overline{B}$	A5P1-D
-E	FC B4	{ XA6-$\overline{C}$, XA7-$\overline{C}$, XA8-$\overline{C}$, XA9-$\overline{C}$	A5P1-E
-F	FC B5	{ XA6-$\overline{D}$, XA7-$\overline{D}$ XA8-$\overline{D}$, XA9-$\overline{D}$	A5P1-F
-H	FC B6	{ XA6-$\overline{E}$, XA7-$\overline{E}$, XA8-$\overline{E}$, XA9-$\overline{E}$	A5P1-H
-J	FC B7	{ XA6-$\overline{F}$, XA7-$\overline{F}$ XA8-$\overline{F}$, XA9-$\overline{F}$	A5P1-J
-K	ΔF ≤50 MHz	A5P1-K	XA10-U
-L	ΔF ≤50 MHz RTN	A5P1-L	XA10-T
-M	+15V	A0U3-3	A5P1-M

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
-N	-15V	A0U1-3	A5P1-N
-P	DIGITAL GND	A14 Ground Plane	A5P1-P
-R	+5V	XA13-T, U, 16, 17	A5P1-R
-S	+10V REF	A5P1-S	XA6-12, XA7-12 XA8-12, XA9-12 & P7-13
-T	CW FILTER	A5P1-T	XA6-13, XA7-13 XA8-13 & XA9-13
-U	FREQ CORRECTION	A5P1-U	XA6-14, XA7-14 XA8-14 & XA9-14
-V	RF SLOPE CONTROL	A5P1-V	XA4-T, P7-26
-W	FCEN/VPF	A5P1-W	XA6-16, XA7-16, XA8-16, XA9-16
-X	ΔF >50 MHz	A5P1-X	XA6-17, XA7-17, XA8-17 & XA9-17
-Y	ΔF SIG GND	A5P1-Y	XA6-18, XA7-18, XA8-18 & XA9-18
-Z	FCEN SIG GND	A5P1-Z	XA6-18, XA7-18, XA8-18 & XA9-18
-$\overline{A}$	F CEN	A5P1-$\overline{A}$	XA6-19, XA7-19, XA8-19 & XA9-19
-$\overline{B}$	ANALOG GND	A14 Ground Plane	A5P1-$\overline{B}$
-$\overline{C}$	μP B6	P6-6	A5P1-$\overline{C}$
-$\overline{D}$	μP B4	P6-7	A5P1-$\overline{D}$
-$\overline{E}$	μP B2	P6-8	A5P1-$\overline{E}$
-$\overline{F}$	μP LSB (BØ)	P6-9	A5P1-$\overline{F}$
XA6 -1	+12/-24V	XA13-W, 19	A6P1-1
-2	L HET PIN SEL	A6P1-2	A14CR17-Cathode
-3	H SNB HET	XA6-H	A6P1-3
-4	H SNR HET	XA6-J	A6P1-4
-5	L RF OFF	XA4-V	A6P1-5
-6	L PIN SW OFF	XA4-X	A6P1-6
-7	PIN MOD DRIVER	XA4-S	A6P1-7
-8	+15V	A0U3-3	A6P1-8
-9	-15V	A0U1-3	A6P1-9
-10	DIGITAL GND	A14 Ground Plane	A6P1-10
-11	+5V	XA13-T, U, 16, 17	A6P1-11
-12	+10V REF	XA5-S	A6P1-12
-13	CW FILTER	XA5-T	A6P1-13
-14	F CORR	XA5-U	A6P1-14
-15	REF GND	XA4-E	A6P1-15
-16	FCEN/VPF	XA5-W	A6P1-16
-17	ΔF >50 MHz	XA5-X	A6P1-17
-18	F CEN SIG GND	XA5-Z	A6P1-18
-19	F CEN	XA5-A	A6P1-19
-20	ANALOG GND 1	A14 Ground Plane	A6P1-20
-21	ROM B7 (MSB)	A14U6-19	A6P1-21
-22	ROM B6	A14U6-16	A6P1-22
-23	ROM B5	A14U6-15	A6P1-23
-24	ROM B4	A14U6-12	A6P1-24
-25	ROM B3	A14U6-9	A6P1-25
-26	ROM B2	A14U6-6	A6P1-26
-27	ROM B1	A14U6-5	A6P1-27
-28	ROM B0 (LSB)	A14U6-2	A6P1-28
-A	L PIN SELECT	A6P1-A	A14CR35-Cathode, A14CR18-Cathode
-B	+18V UNREG	A14R101	A6P1-B
-C	H SNB 1	A6P1-C	XA7-3
-D	H SNR 1	A6P1-D	XA7-4 & A14U7-13
-E	L YIG 1 SEL	A6P1-E	XA10-$\overline{F}$ & A14U7-3
-F	TRACK FILTER	A6P1-F	XA10-E
-H	L HET YIG SEL	A6P1-H	XA10-26
-J	L HET ROM SEL	A6P1-J	XA6-4

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- K	MOD DRIVER 1	A6P1-K	A14C32, A14R34
- L	DIGITAL GND	A14 Ground Plane	A6P1-L
- M	+5V	XA13-T, U, 16, 17	A6P1-M
- N	YIG 1 BIAS GND SENSE	A6P1-N	P14-2
- P	A6Q1-E	A6P1-P	P18-1
- R	A6Q1-C	A6P1-R	P18-2
- S	A6Q1-B	A6P1-S	P18-3
- T	YIG 1 COIL (+)	A6P1-T	P14-6
- U	YIG 1 COIL (-)	A6P1-U	P19-2, P14-7
- V	YIG 1 TUNE CONTROL	A6P1-V	P19-3
- W	YIG 1 TUNE SUPPLY	A6P1-W	P20-3
- X	ANALOG GND 1	A14 Ground Plane	A6P1-X
- Y	FC B2	A6P1-Y	XA5-A
- Z	FC B3	A6P1-Z	XA5-B
- $\overline{A}$	FC BØ (LSB)	A6P1-$\overline{A}$	XA5-C
- $\overline{B}$	FC B1	A6P1-$\overline{B}$	XA5-D
- $\overline{C}$	FC B4	A6P1-$\overline{C}$	XA5-E
- $\overline{D}$	FC B5	A6P1-$\overline{D}$	XA5-F
- $\overline{E}$	FC B6	A6P1-$\overline{E}$	XA5-H
- $\overline{F}$	FC B7 (MSB)	A6P1-$\overline{F}$	XA5-J
XA7 - 1	+12/-24V	XA13-W, 19	A7P1-1
- 2	L HET PIN SEL	A7P1-2	A14CR17-Cathode
- 3	H SNB 1	XA6-C	A7P1-3
- 4	H SNR 1	XA6-D	A7P1-4
- 5	L RF OFF	XA4-V	A7P1-5
- 6	L PIN SW OFF	XA4-X	A7P1-6
- 7	PIN MOD DRIVER	XA4-S	A7P1-7
- 8	+15V	A0U3-3	A7P1-8
- 9	-15V	A0U1-3	A7P1-9
- 10	DIGITAL GND	A14 Ground Plane	A7P1-10
- 11	+5V	XA13-T, U, 16, 17	A7P1-11
- 12	+10V REF	XA5-S	A7P1-12
- 13	CW FILTER	XA5-T	A7P1-13
- 14	F CORR	XA5-U	A7P1-14
- 15	REF GND	XA4-E	A7P1-15
- 16	FCEN/VPF	XA5-W	A7P1-16
- 17	ΔF >50 MHz	XA5-X	A7P1-17
- 18	F CEN SIG GND	XA5-Z	A7P1-18
- 19	F CEN	XA5-$\overline{A}$	A7P1-19
- 20	ANALOG GND 1	A14 Ground Plane	A7P1-20
- 21	ROM B7 (MSB)	A14U6-19	A7P1-21
- 22	ROM B6	A14U6-16	A7P1-22
- 23	ROM B5	A14U6-15	A7P1-23
- 24	ROM B4	A14U6-12	A7P1-24
- 25	ROM B3	A14U6-9	A7P1-25
- 26	ROM B2	A14U6-6	A7P1-26
- 27	ROM B1	A14U6-5	A7P1-27
- 28	ROM B0 (LSB)	A14U6-2	A7P1-28
- A	L PIN SELECT 2	A7P1-A	A14CR20-Cathode
- B	+18V UNREG	A14R101	A7P1-B
- C	H SNB 2	A7P1-C	XA8-3
- D	H SNR 2	A7P1-D	XA8-4 & A14U7-14
- E	L YIG 2 SEL	A7P1-E	XA10-28 & A14U7-4
- F	TRACK FILTER 2	A7P1-F	XA10-27
- H	L HET YIG SEL	A7P1-H	XA10-26
- J	L HET ROM SEL	A7P1-J	XA6-4
- K	MOD DRIVER 2	A7P1-K	A14R37
- L	DIGITAL GND	A14 Ground Plane	A7P1-L
- M	+5V	XA13-T, U, 16, 17	A7P1-M
- N	YIG 2 BIAS GND SENSE	A7P1-N	P13-2
- P	A7Q1-E	A7P1-P	P21-1
- R	A7Q1-C	A7P1-R	P21-2

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- S	A7Q1-B	A7P1-S	P21-3
- T	YIG 2 COIL (+)	A7P1-T	P13-6
- U	YIG 2 COIL (-)	A7P1-U	P22-2
- V	YIG 2 TUNE CONTROL	A7P1-V	P22-3
- W	YIG 2 TUNE SUPPLY	A7P1-W	P23-3
- X	ANALOG GND 1	A14 Ground Plane	A7P1-X
- Y	FC B2	A7P1-Y	XA5-A
- Z	FC B3	A7P1-Z	XA5-B
- $\overline{A}$	FC BØ (LSB)	A7P1-$\overline{A}$	XA5-C
- $\overline{B}$	FC B1	A7P1-$\overline{B}$	XA5-D
- $\overline{C}$	FC B4	A7P1-$\overline{C}$	XA5-E
- $\overline{D}$	FC B5	A7P1-$\overline{D}$	XA5-F
- $\overline{E}$	FC B6	A7P1-$\overline{E}$	XA5-H
- $\overline{F}$	FC B7 (MSB)	A7P1-$\overline{F}$	XA5-J
XA8 - 1	+12V/-24V	XA13-W, 19	A8P1-1
- 2	+18V UNREG	A14R101	A8P1-2
- 3	H SNB 2	XA7-C	A8P1-3
- 4	H SNR 2	XA7-D	A8P1-4
- 5	L RF OFF	XA4-V	A8P1-5
- 6	L PIN SW OFF	XA4-X	A8P1-6
- 7	PIN MOD DRIVER	XA4-S	A8P1-7
- 8	+15V	A0U3-3	A8P1-8
- 9	-15V	A0U1-3	A8P1-9
- 10	DIGITAL GND	A14 Ground Plane	A8P1-10
- 11	+5V	XA13-T, U, 16, 17	A8P1-11
- 12	+10V REF	XA5-S	A8P1-12
- 13	CW FILTER	XA5-T	A8P1-13
- 14	F CORR	XA5-U	A8P1-14
- 15	REF GND	XA4-K	A8P1-15
- 16	FCEN/VPF	XA5-W	A8P1-16
- 17	ΔF >50 MHz	XA5-X	A8P1-17
- 18	F CEN SIG GND	XA5-Z	A8P1-18
- 19	F CEN	XA5-A	A8P1-19
- 20	ANALOG GND 1	A14 Ground Plane	A8P1-20
- 21	ROM B7 (MSB)	A14U6-19	A8P1-21
- 22	ROM B6	A14U6-16	A8P1-22
- 23	ROM B5	A14U6-15	A8P1-23
- 24	ROM B4	A14U6-12	A8P1-24
- 25	ROM B3	A14U6-9	A8P1-25
- 26	ROM B2	A14U6-6	A8P1-26
- 27	ROM B1	A14U6-5	A8P1-27
- 28	ROM B0 (LSB)	A14U6-2	A8P1-28
- A	L PIN SELECT 3	A8P1-A	A14CR22-Cathode
- B	+18V UNREG	A14R101	A8P1-B
- C	H SNB 3	A8P1-C	XA9-3
- D	H SNR 3	A8P1-D	XA9-4 & A14U7-17
- E	L YIG 3 SEL	A8P1-E	XA10-M, A14U7-7, XA5-7
- F	TRACK FILTER 3	XA10-K	A8P1-F
- H	Vacant		A8P1-H
- J	Vacant		A8P1-J
- K	MOD DRIVER 3	A8P1-K	A14R50
- L	DIGITAL GND	A14 Ground Plane	A6P1-L
- M	+5V	XA13-T, U, 16, 17	A6P1-M
- N	YIG 3 BIAS GND SENSE	A8P1-N	P17-2
- P	A8Q1-E	A8P1-P	P28-1
- R	A8Q1-C	A8P1-R	P28-2
- S	A8Q1-B	A8P1-S	P28-3
- T	YIG 3 COIL (+)	A8P1-T	P17-6
- U	YIG 3 COIL (-)	A8P1-U	P29-2
- V	YIG 3 TUNE CONTROL	A8P1-V	P29-3
- W	YIG 3 TUNE SUPPLY	A8P1-W	P30-3
- X	ANALOG GND	A14 Ground Plane	A8P1-X

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- Y	FC B2	A8P1-Y	XA5-A
- Z	FC B3	A8P1-Z	XA5-B
- A̅	FC BØ (LSB)	A8P1-A̅	XA5-C
- B̅	FC B1	A8P1-B̅	XA5-D
- C̅	FC B4	A8P1-C̅	XA5-E
- D̅	FC B5	A8P1-D̅	XA5-F
- E̅	FC B6	A8P1-E̅	XA5-H
- F̅	FC B7 (MSB)	A8P1-F̅	XA5-J
XA9 - 1	+12/-24V	XA13-W, 19	A9P1-1
- 2	+18V UNREG	A14R101	A9P1-2
- 3	H SNB 3	XA8-C	A9P1-3
- 4	H SNR 3	XA8-D	A9P1-4
- 5	L RF OFF	XA4-V	A9P1-5
- 6	L PIN SW OFF	XA4-X	A9P1-6
- 7	PIN MOD DRIVER	XA4-S	A9P1-7
- 8	+15V	A0U3-3	A9P1-8
- 9	-15V	A0U1-3	A9P1-9
- 10	DIGITAL GND	A14 Ground Plane	A9P1-10
- 11	+5V	XA13-T, U, 16, 17	A9P1-11
- 12	+10V REF	XA5-S	A9P1-12
- 13	CW FILTER	XA5-T	A9P1-13
- 14	F CORR	XA5-U	A9P1-14
- 15	REF GND	XA4-K	A9P1-15
- 16	FCEN/VPF	XA5-W	A9P1-16
- 17	ΔF >50 MHz	XA5-X	A9P1-17
- 18	F CEN SIG GND	XA5-Z	A9P1-18
- 19	F CEN	XA5-A̅	A9P1-19
- 20	ANALOG GND 1	A14 Ground Plane	A9P1-20
- 21	ROM B7 (MSB)	A14U6-19	A9P1-21
- 22	ROM B6	A14U6-16	A9P1-22
- 23	ROM B5	A14U6-15	A9P1-23
- 24	ROM B4	A14U6-12	A9P1-24
- 25	ROM B3	A14U6-9	A9P1-25
- 26	ROM B2	A14U6-6	A9P1-26
- 27	ROM B1	A14U6-5	A9P1-27
- 28	ROM B0 (LSB)	A14U6-2	A9P1-28
- A	L PIN SELECT 4	A9P1-A	A14CR34-Cathode
- B	+18V UNREG	A14R101	A9P1-B
- C	Vacant		A9P1-C
- D	H SNR 4	A9P1-D	A14U7-18
- E	L YIG 4 SEL	A9P1-E	XA10-L & A14U7-8
- F	TRACK FILTER 4	XA10-J	A9P1-F
- H	Vacant		A9P1-H
- J	Vacant		A9P1-J
- K	MOD DRIVER 4	A9P1-K	A14R68
- L	DIGITAL GND	A14 Ground Plane	A9P1-L
- M	+5V	XA13-T, U, 16, 17	A9P1-M
- N	YIG 4 BIAS GND SENSE	A9P1-N	P16-2
- P	A9Q1-E	A9P1-P	P25-1
- R	A9Q1-C	A9P1-R	P25-2
- S	A9Q1-B	A9P1-S	P25-3
- T	YIG 4 COIL (+)	A9P1-T	P16-6
- U	YIG 4 COIL (-)	A9P1-U	P26-2
- V	YIG 4 TUNE CONTROL	A9P1-V	P26-3
- W	YIG 4 TUNE SUPPLY	A9P1-W	P27-3
- X	ANALOG GND	A14 Ground Plane	A9P1-X
- Y	FC B2	A9P1-Y	XA5-A
- Z	FC B3	A9P1-Z	XA5-B
- A̅	FC BØ (LSB)	A9P1-A̅	XA5-C
- B̅	FC B1	A9P1-B̅	XA5-D
- C̅	FC B4	A9P1-C̅	XA5-E
- D	FC B5	A9P1-D̅	XA5-F

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
- $\overline{E}$	FC B6	A9P1-$\overline{E}$	XA5-H
- $\overline{F}$	FC B7 (MSB)	A9P1-$\overline{F}$	XA5-J
XA10 - 1	H ATTN 1	XA4-24	A10P1-1
- 2	H ATTN 3	XA4-23	A10P1-2
- 3	H FM DIAG 1	A10P1-3	A14U8-14
- 4	Vacant		A10P1-4
- 5	H EXT FM ENABLE	XA2-Y	A10P1-5
- 6	+5V	XA13-T, U, 16, 17	A10P1-6
- 7	DIGITAL GND	A14 Ground Plane	A10P1-7
- 8	H 20DB ATTN DRVR (BLACK)	A10P1-8	P31-8
- 9	L 20DB ATTN DRVR (GREEN)	A10P1-9	P31-7
- 10	HA 40DB ATTN DRVR (ORANGE)	A10P1-10	P31-6
- 11	LA 40DB ATTN DRVR (BLUE)	A10P1-11	P31-5
- 12	HB 40DB ATTN DRVR (BROWN)	A10P1-12	P31-4
- 13	LB 40DB ATTN DRVR (WHITE)	A10P1-13	P31-3
- 14	H 10DB ATTN DRVR (PURPLE)	A10P1-14	P31-2
- 15	L 10DB ATTN DRVR (YELLOW)	A10P1-15	P31-1
- 16	TRACK FILTER COIL (RTN)	P16-8	A10P1-16
- 17	FM COIL, WJ (RTN)	P16-10	A10P1-17
- 18	FM COIL, AVANTEK (RTN)	P16-12	A10P1-18
- 19	Vacant		A10P1-19
- 20	FM COIL, AVANTEK (SOURCE)	A10P1-20	P14-13
- 21	FM COIL, WJ (SOURCE)	A10P1-21	P14-11
- 22	TRACK FILTER COIL (SOURCE)	A10P1-22	P14-9
- 23	+15V HC	A0U4-3	A10P1-23
- 24	-15V HC	A0U2-3	A10P1-24
- 25	ANALOG GND	A14 Ground Plane	A10P1-25
- 26	L HET YIG SEL	XA7-H	A10P1-26
- 27	TRACK FILTER 2	XA7-F	A10P1-27
- 28	L YIG 2 SEL	XA7-$\underline{E}$	A10P1-28
- A	H ATTN 2	XA4-$\underline{B}$	A10P1-A
- B	H ATTN 4	XA4-$\underline{A}$	A10P1-B
- C	H FM DIAG 2	A10P1-C	A14U8-17
- D	H FM DIAG	A10P1-D	A14U8-13
- E	L EOB	A10P1-E	XA2-Z
- F	+5V	XA13-T, U, 16, 17	A10P1-F
- H	DIGITAL GND	A14 Ground Plane	A10P1-H
- J	TRACK FILTER 4	XA9-F	A10P1-J
- K	TRACK FILTER 3	XA8-F	A10P1-K
- L	L YIG 4 SEL	XA9-E	A10P1-L
- M	L YIG 3 SEL	XA8-E	A10P1-M
- N	ATTN PWR SUPPLY	A10P1-N	P31-9
- P	Vacant		A10P1-P
- R	+24V	A14U2-3	A10P1-R
- S	EXT FM INPUT	P34-2	A10P1-S
- T	ΔF ≤50 MHz RTN	XA5-L	A10P1-T
- U	ΔF ≤50 MHz	XA5-K	A10P1-U
- V	EXT FM RTN	P34-1	A10P1-V
- W	PHASE LOCK RTN	P33-1	A10P1-W
- X	PHASE LOCK INPUT	P33-2	A10P-X
- Y	Vacant		A10P1-Y
- $\underline{Z}$	Vacant		A10P1-$\underline{Z}$
- $\underline{A}$	+15V HC	A0U4-3	A10P1-$\underline{A}$
- $\underline{B}$	-15V HC	A0U2-3	A10P1-$\underline{B}$
- $\underline{C}$	ANALOG GND	A14 Ground Plane	A10P1-$\underline{C}$
- $\underline{D}$	Vacant		A10P1-$\underline{D}$
- $\underline{E}$	TRACK FILTER 1	XA6-F	A10P1-$\underline{E}$
- $\underline{F}$	L YIG 1 SEL	XA6-E	A10P1-$\underline{F}$
XA13 - 1	-165V	A14CR12(-)	A13P1-1
- 2	165V RTN	A14P1-7	A13P1-2
- 3	+165V	A14R16	A13P1-3
- 4	Vacant		

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
-5	SHUT DOWN LED	A14DS2-2	A13P1-5
-6	OVER VOLTAGE/CURRENT	A14Q4-Collector, A14U1-5	A13P1-6
-7	REG RTN	A14CR9-Anode, A14CR6-Anode	A13P1-7
-8	REG IN	A14CR7-Cathode, A14CR8-Cathode	A13P1-8
-9	100 kHz INJECTION	P38-1	A13P1-9
-10	LINE SYNC	A14CR5-Cathode	A13P1-10
-11	DIGITAL GND	A14 Ground Plane	A13P1-11
-12	DIGITAL GND	A14 Ground Plane	A13P1-12
-13	DIGITAL GND SENSE	A14 Ground Plane	A13P1-13
-14	EARTH GND	A14P1-2	A13P1-14
-15	EARTH GND	A14P1-2	A13P1-15
-16	+5V SOURCE	A13P1-16	Analog & Digital Circuits
-17	+5V SOURCE	A13P1-17	
-18	+12V/-24V RTN	A14 Ground Plane	A13P1-18
-19	+12V/-24V	A13P1-19	XA6-XA9, Pin 1 (A14R99)
-20	+28V RTN	A14 Ground Plane	A13P1-20
-21	+28V	A13P1-21	P13-P17, Pin 4
-22, -23	-18V	A13P1-22, A13P1-23	A13P2-4 & A0U1-1
-24	18V RTN	A14 Ground Plane	A13P1-24
-25	(ANALOG GND)		A13P1-25
-26	+18V	A13P1-26	A14R13, A0U3-1, A0U4-1
-27	-43V RTN	A14 Ground Plane	A13P1-27
-28	-43V	A13P1-28	A0Q1-Base, A14CR1-Anode
-A	-165V	A14CR12(-)	A13P1-A
-B	165V RTN	A14P1-7	A13P1-B
-C	+165V	A14R16	A13P1-3
-D	Vacant		
-E	SHUT DOWN LED	A14DS2-2	A13P1-E
-F	OVER VOLTAGE/CURRENT	A14Q4-Collector, A14U1-5	A13P1-F
-H	REG RTN	A14CR9-Anode, A14CR6-Anode	A13P1-H
-J	REG IN	A14CR7-Cathode, A14CR8-Cathode	A13P1-8
-K	Not Used		
-L	LINE SYNC	A14CR5-Cathode	A13P1-L
-M	DIGITAL GND	A14 Ground Plane	A13P1-M
-N	DIGITAL GND		A13P1-N
-P	+5V SENSE	Analog & Digital Circuits	A13P1-P
-R, -S	EARTH GROUND	A14P1-2	A13P1-R, A13P1-S
-T, -U	+5V SOURCE	A13P1-T, A13P1-U	Analog & Digital Circuits
-V	+12V/-24V RTN	A14 Ground Plane	A13P1-V
-W	+12V/-24V	A13P1-W	XA6-XA9, Pin 1
-X	+28V RTN	A14 Ground Plane	A13P1-X
-Y	+28V	A13P1-Y	P13-P17, Pin 4
-Z̲, -A̲	-18V	A3P1-Z̲, A3P1-A̲	A13P2-4, A0U1-1̲
-B̲	18V RTN	A14 Ground Plane	A13P1-B̲
-C̲	(ANALOG GROUND)	A14 Ground Plane	A13P1-C̲
-D̄	+18V	A13P1-D̄	A14R13, A0U3-1, A0U4-1̲
-Ē	-43V RTN	A14 Ground Plane	A13P1-Ē
-F̄	-43V	A13P1-28	A0Q1-Base, A14CR1-Anode

* L = Low-Active State, H = High-Active State

Table 7-22. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA16 - 1	EXT RAMP IN	EXT SWEEP (Rear Panel Connector)	XA2-H
- 2	ACTIVATE RELAY Return	A14 Ground Plane	PENLIFT OUTPUT Shield
- 3	EXT DWELL	SWEEP DWELL INPUT (Rear Panel Connector)	XA2-D
- 4	EXT TRIGGER PULSE IN	SWEEP TRIGGER INPUT (Rear Panel Connector)	XA2-E
- 5	BANDSWITCH BLANKING +	XA2-2	BANDSWITCH BLANKING +, - Switch
- 6	HORIZ OUTPUT DURING CW	CW RAMP Switch	XA3-15
- 7	SEQ SYNC	XA2-6	SEQ SYNC OUTPUT (Rear Panel Connector)
- 8	VIDEO MARKER	XA3-8	MARKER OUTPUT (Rear Panel Connector)
- 9	RETRACE BLANKING +	XA2-5	RETRACE BLANKING OUTPUT + (Rear Panel Connector)
- 10	HORIZONTAL OUTPUT	XA3-J	HORIZ OUTPUT (Rear Panel Connector)
- 11	+5V RETURN	XA2-4	HORIZ OUTPUT DURING CW ON/OFF Switch
- 12	BANDSWITCH BLANKING -	XA4-8	BANDSWITCH BLANKING +, - Switch
- 13	V/GHZ	XA2-3	1V/GHz Output (Rear Panel Connector)
- 14	RETRACE BLANKING -	XA2-S	RETRACE BLANKING OUTPUT (Rear Panel Connector)
- 15	ACTIVATE RELAY	XA4-7	PENLIFT OUTPUT (Rear Panel Connector)
- 16	Vacant	P1-$\bar{A}$	AUX I/O Connector

* L = Low-Active State, H = High-Active State

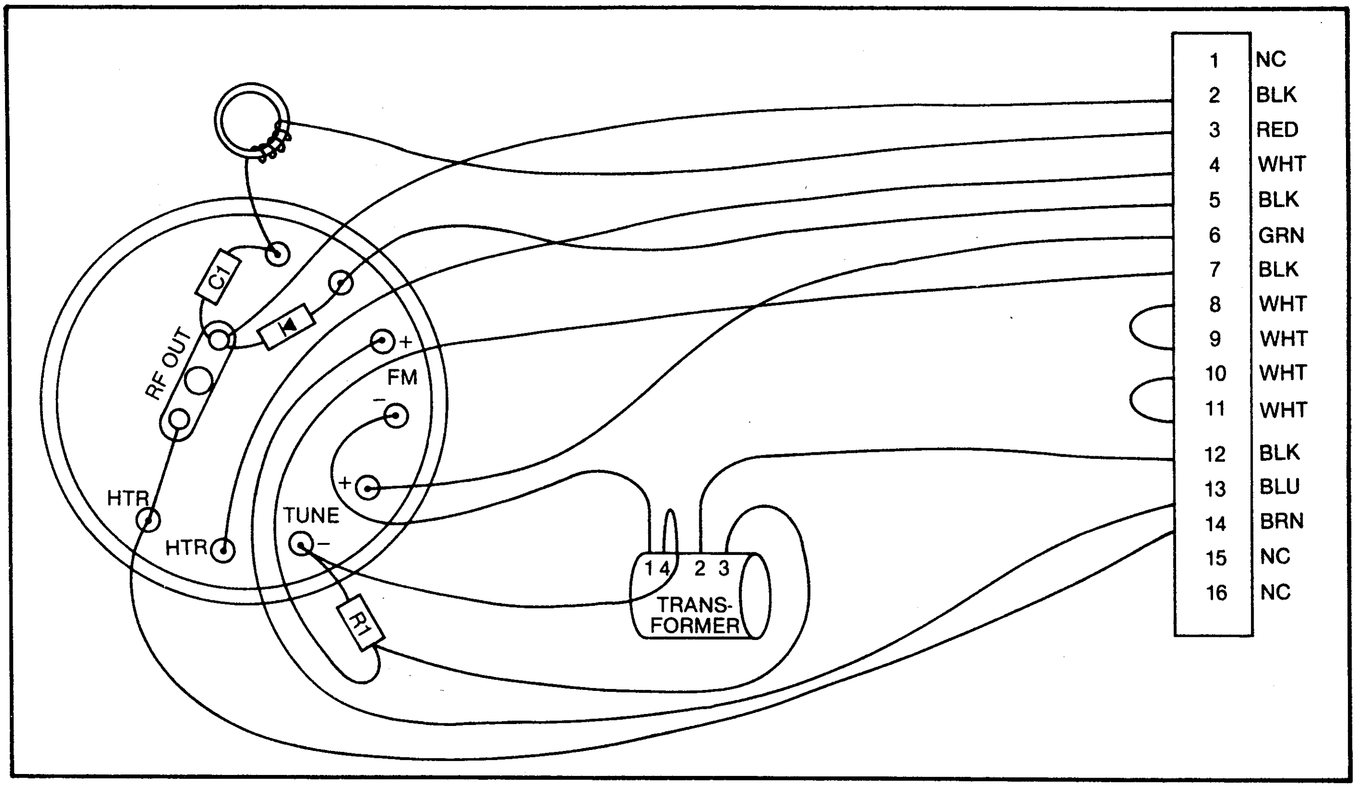


Figure 7-110. 6609A A6 Oscillator Wiring Diagram

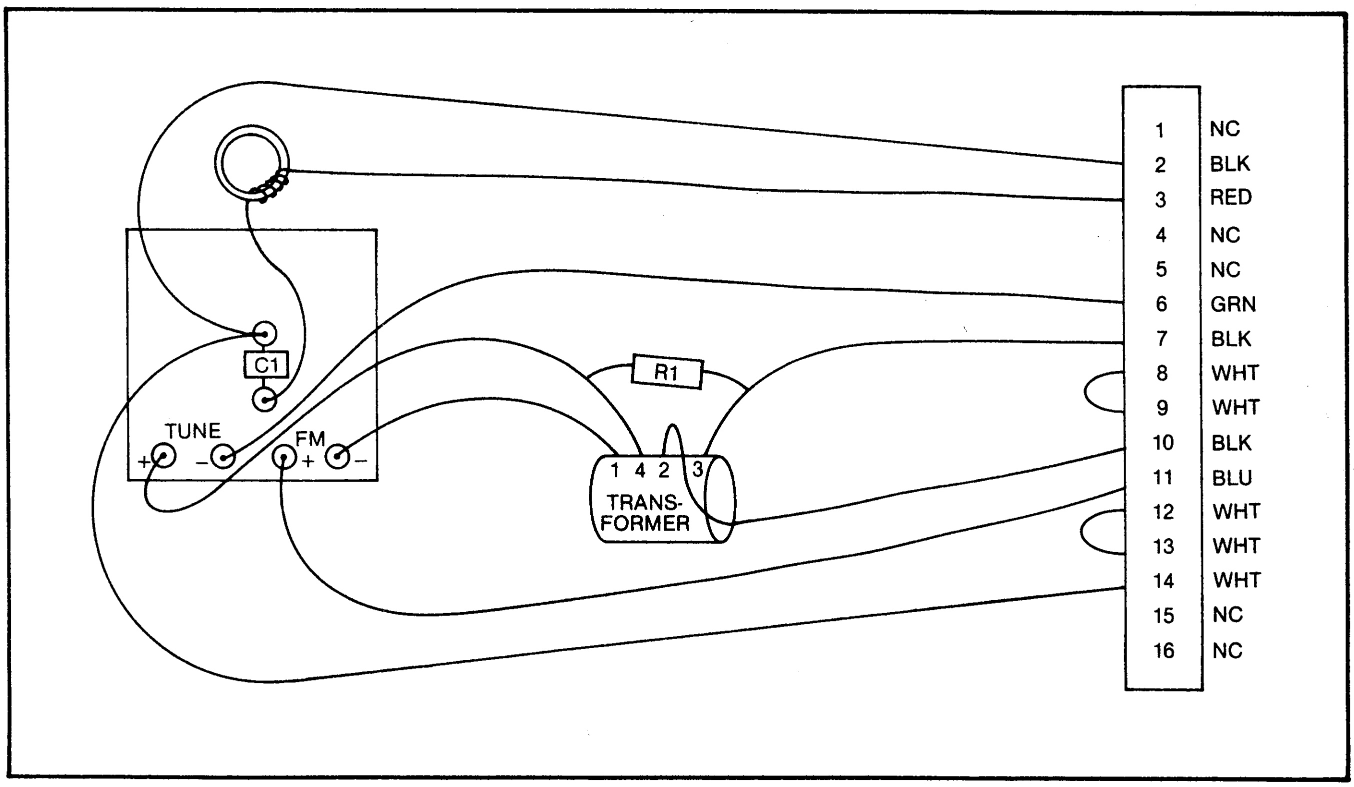


Figure 7-111. 6642A A6 Oscillator Wiring Diagram

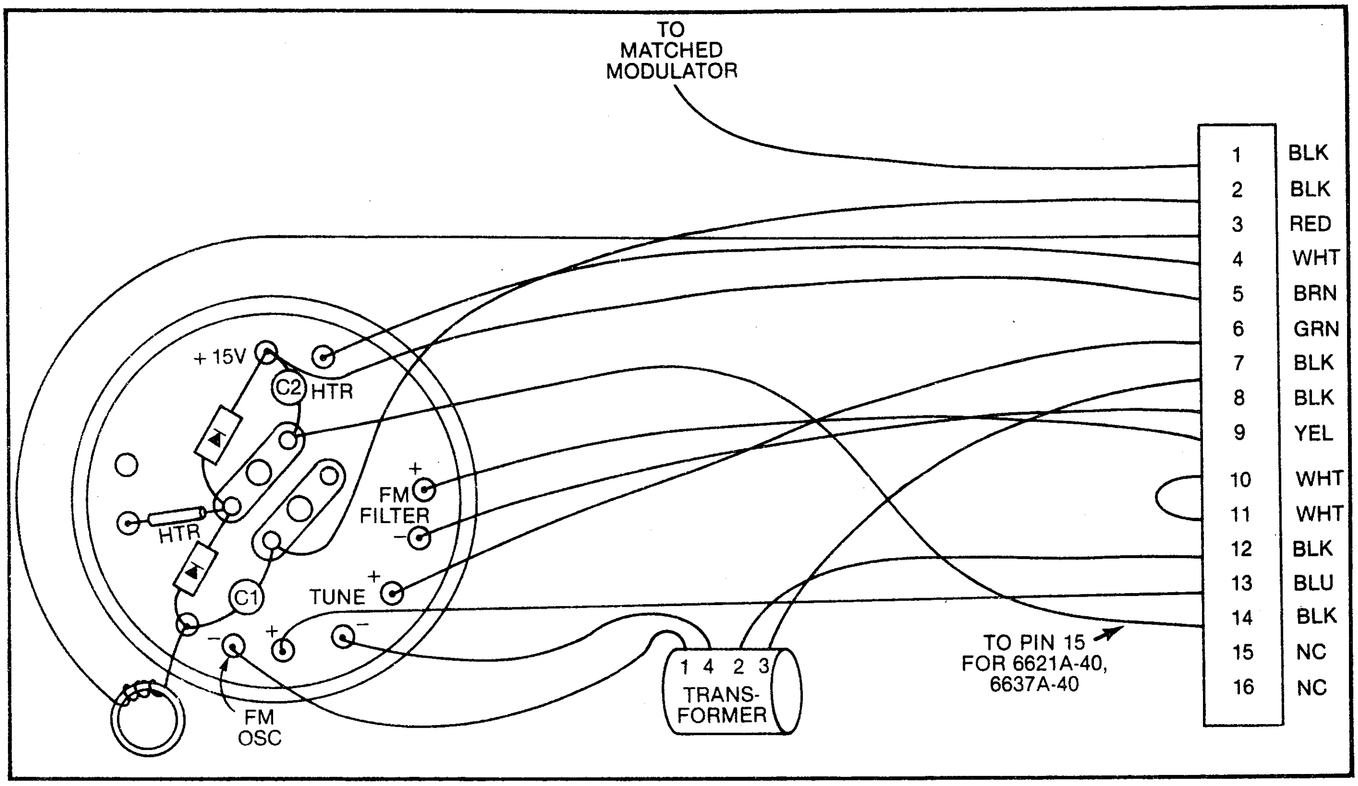


Figure 7-112. A6 Oscillator Wiring Diagram (except 6609A & 6642A)

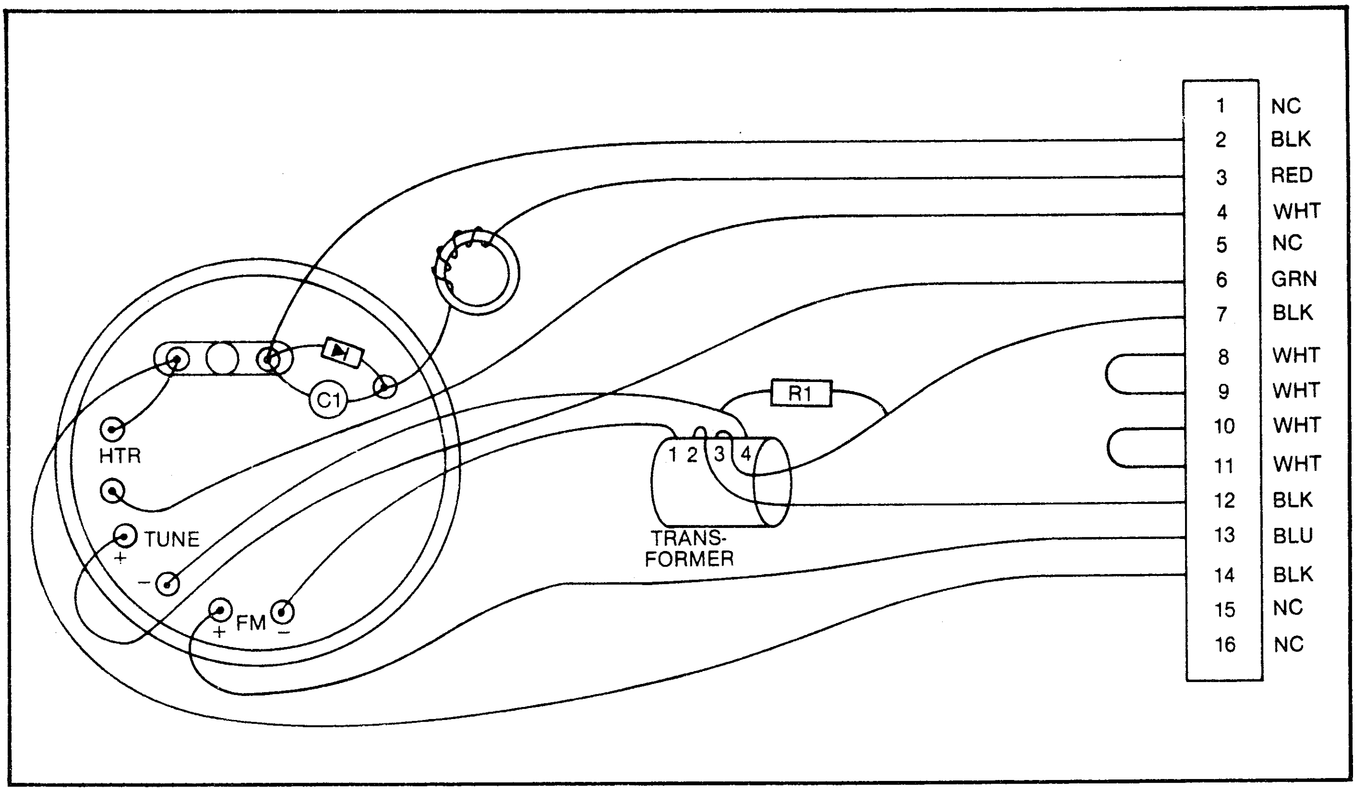


Figure 7-113. 6621A/6629A/6637A/6638A/6647A/6648A A7 Avantek Oscillator Wiring Diagram

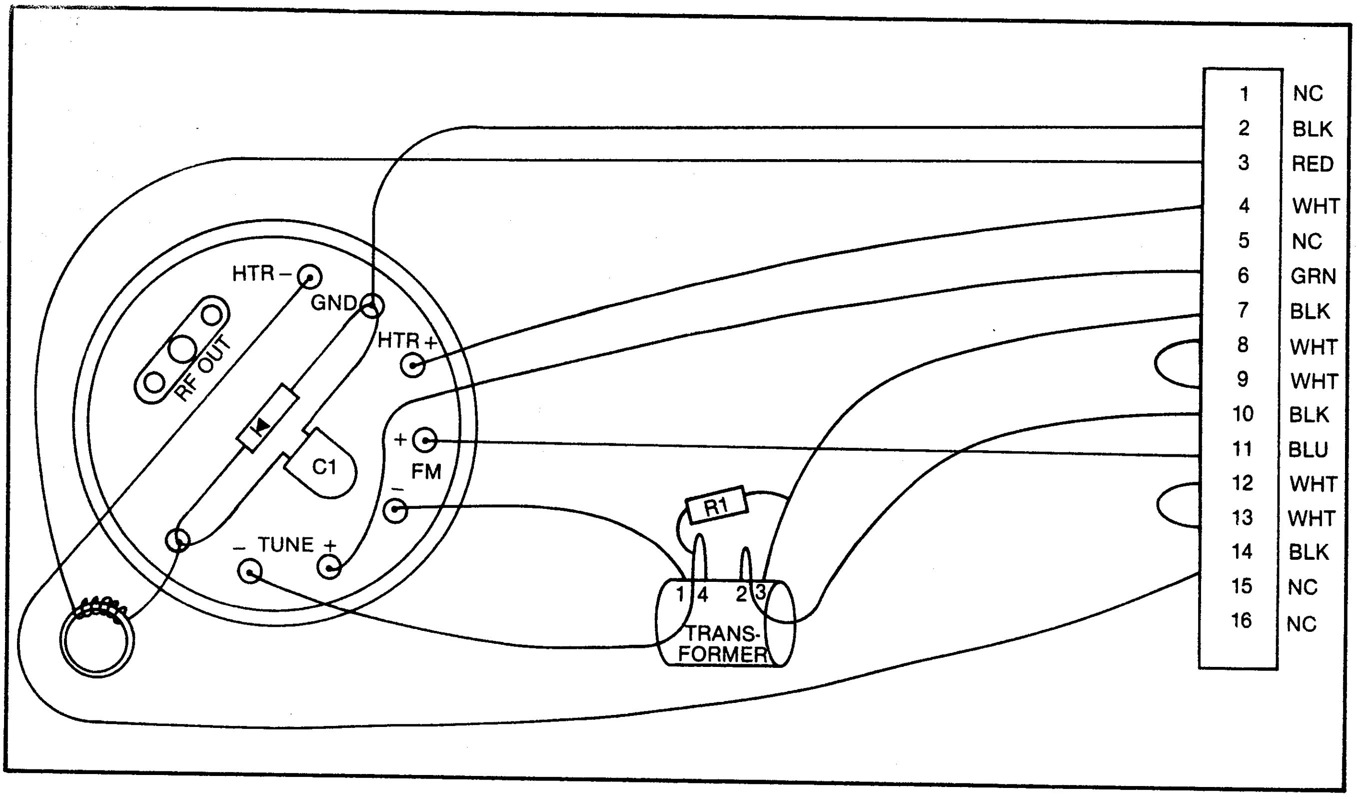


Figure 7-114. 6621A/6629A/6637A/6638A/6647A/6648A A7 Avantek Oscillator Wiring Diagram

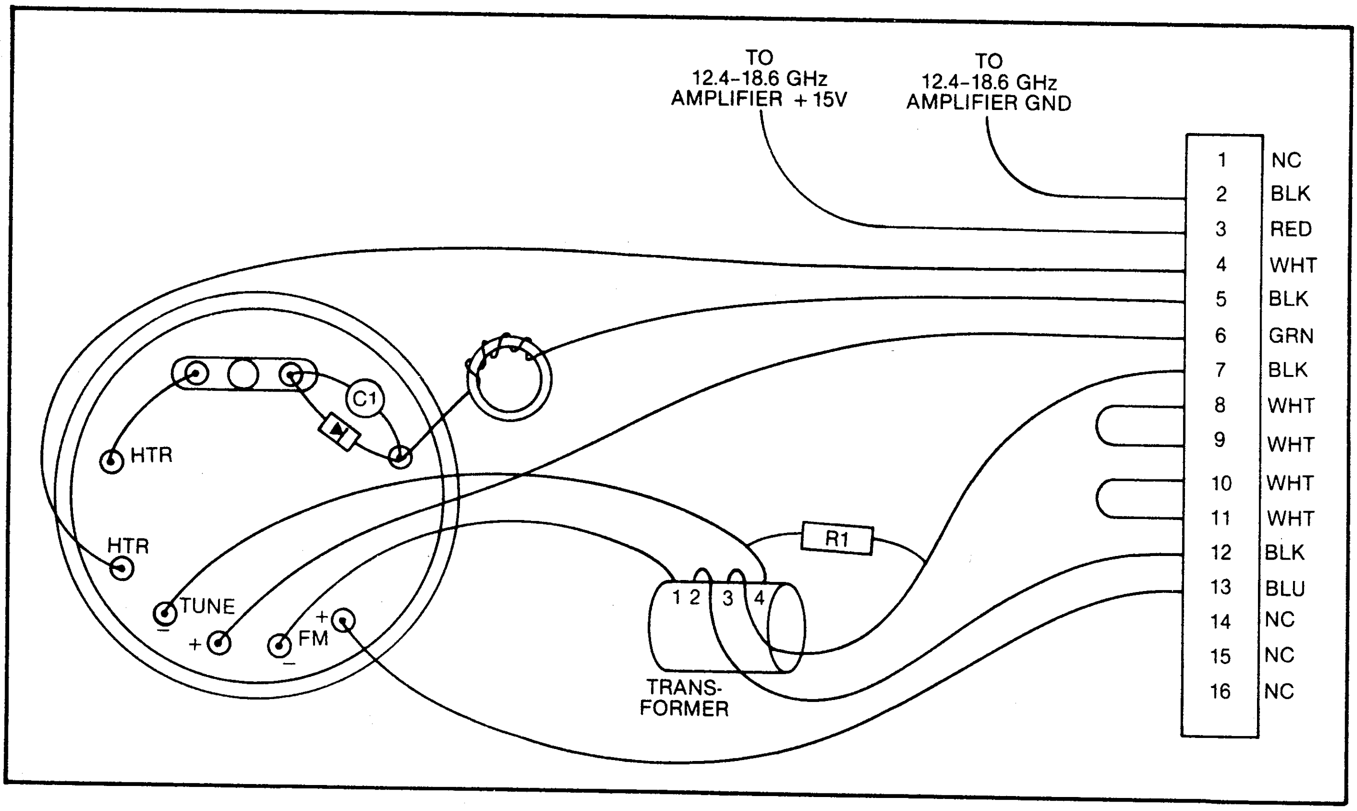


Figure 7-115. 6621A-40/6629A-40/6637A-40 A7 Avantek Oscillator Wiring Diagram

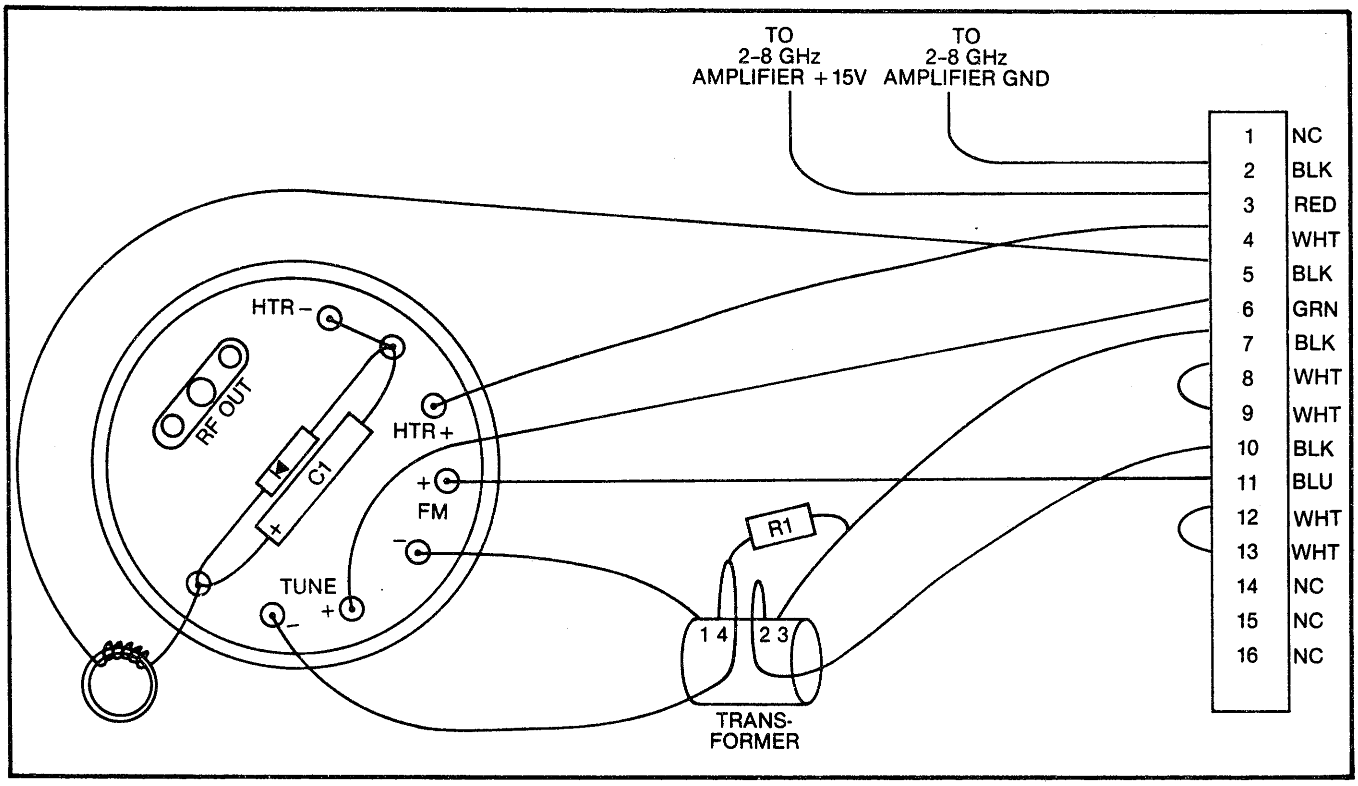


Figure 7-116. 6621A-40/6629A-40/6637A-40 A7 WJ Oscillator Wiring Diagram

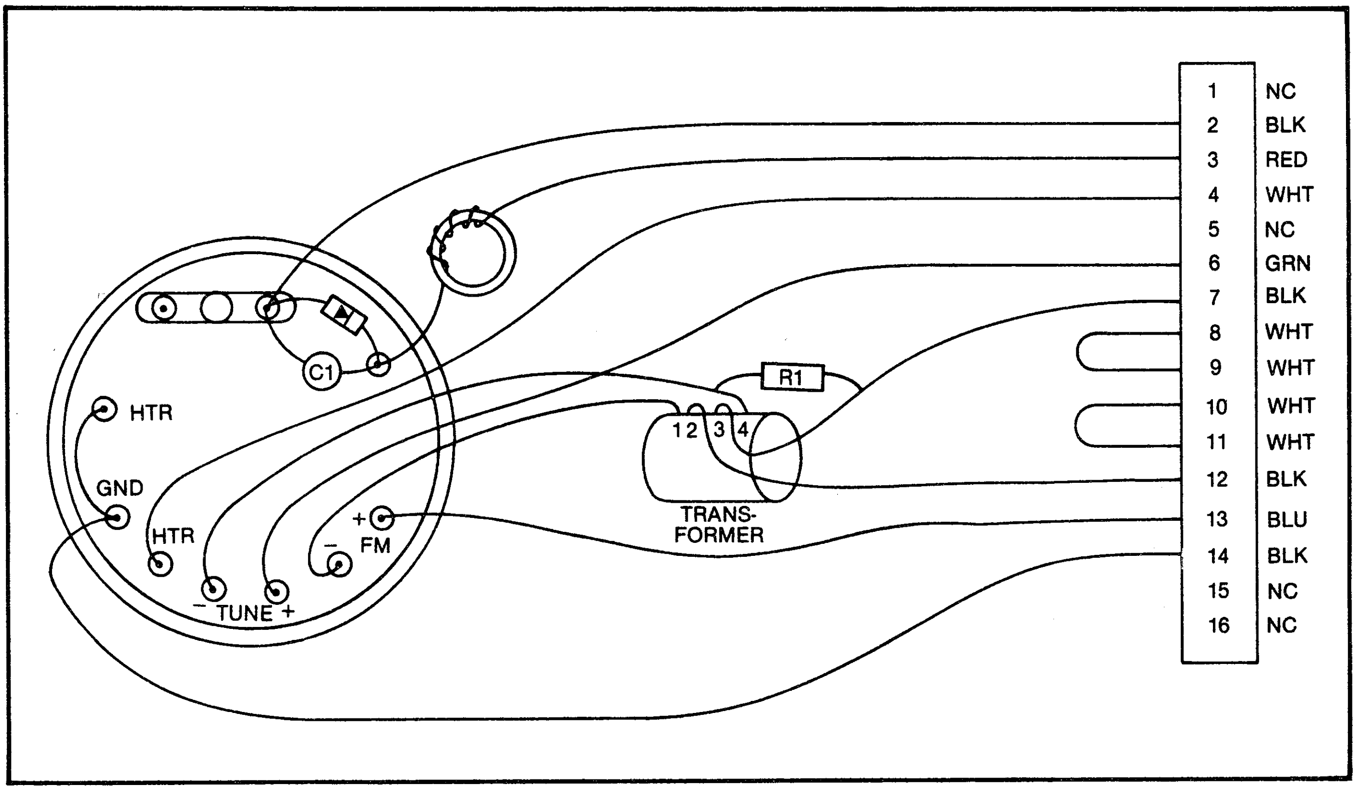


Figure 7-117. 6653A/6659A A7 Avantek Oscillator Wiring Diagram

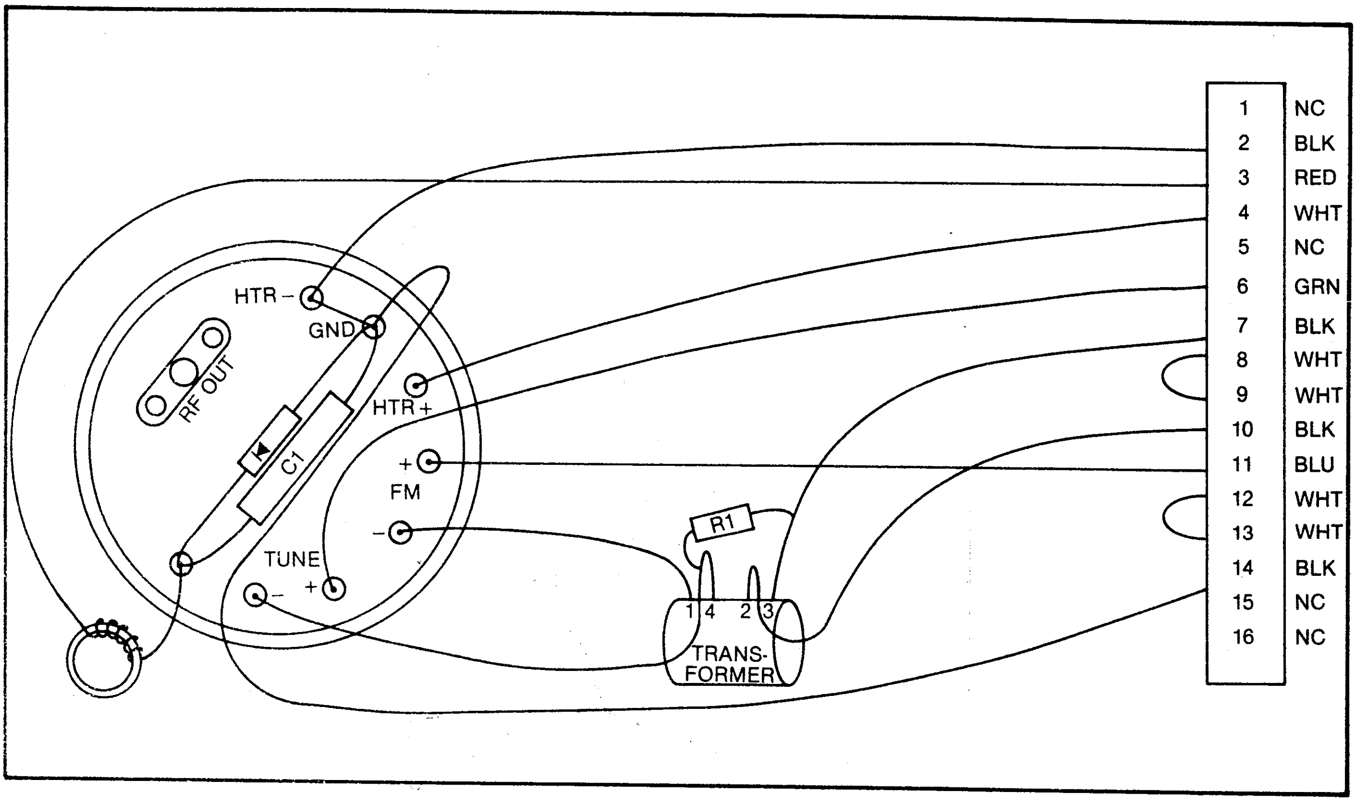


Figure 7-118. 6653A/6659A A7 WJ Oscillator Wiring Diagram

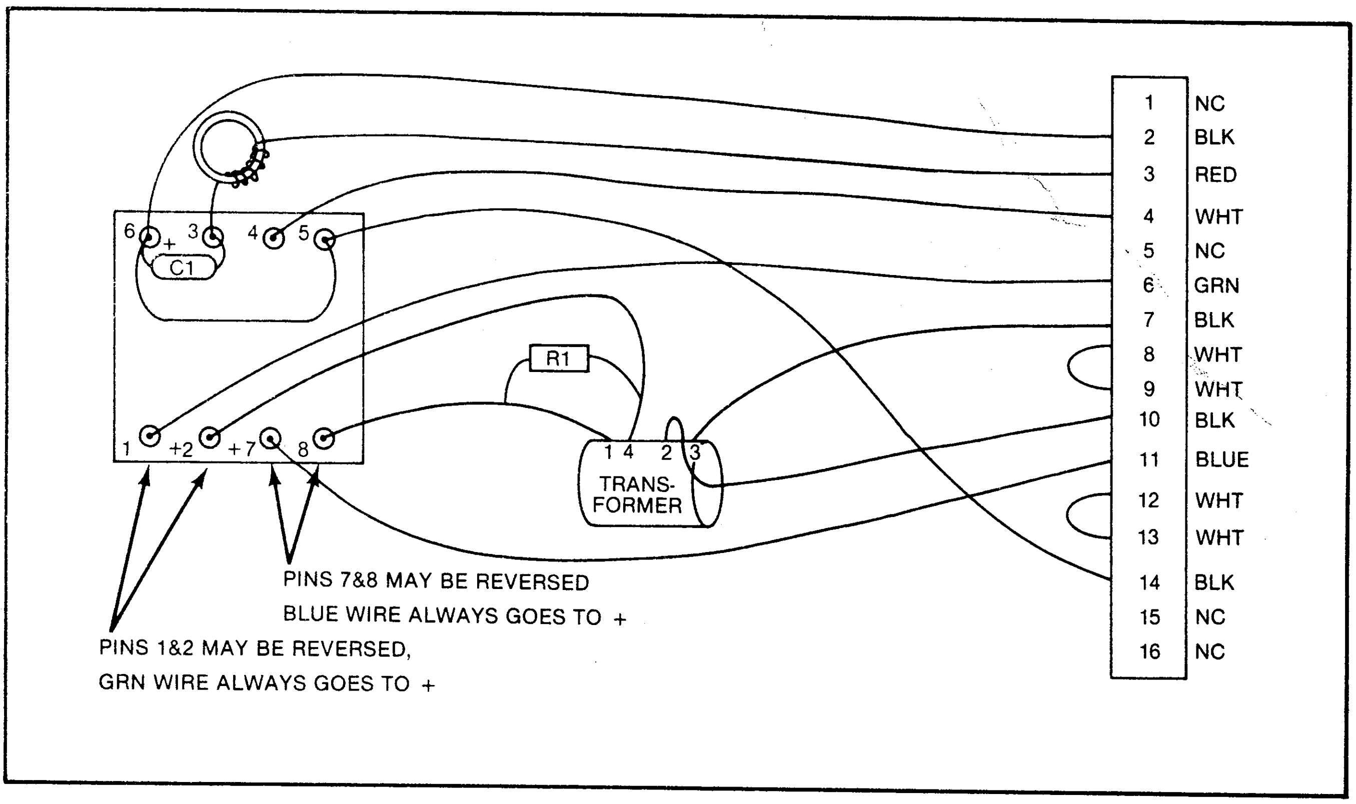


Figure 7-119. 6629A/6637A/6642A(A7)/6647A A8 WJ Oscillator Wiring Diagram

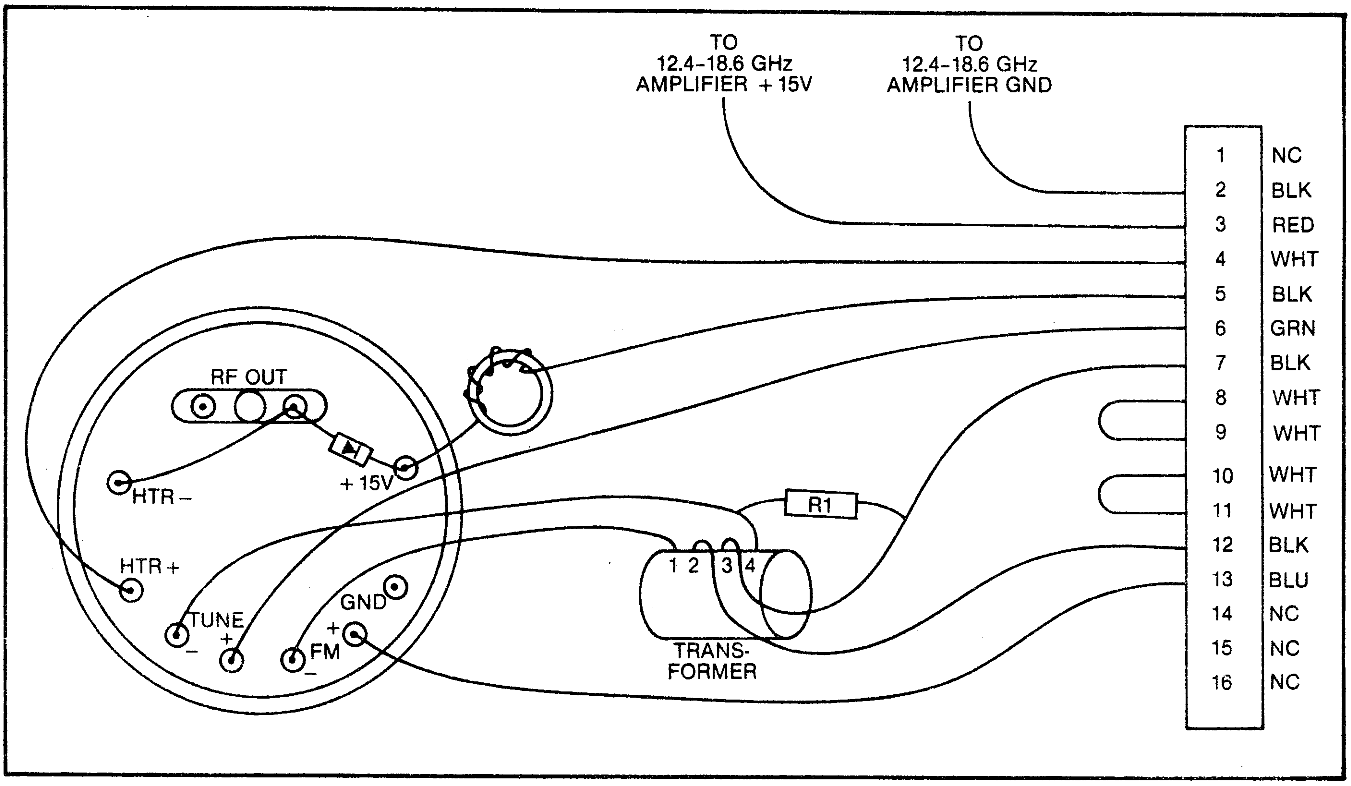


Figure 7-120. 6629A-40/6637A-40 A8 Avantek Oscillator Wiring Diagram

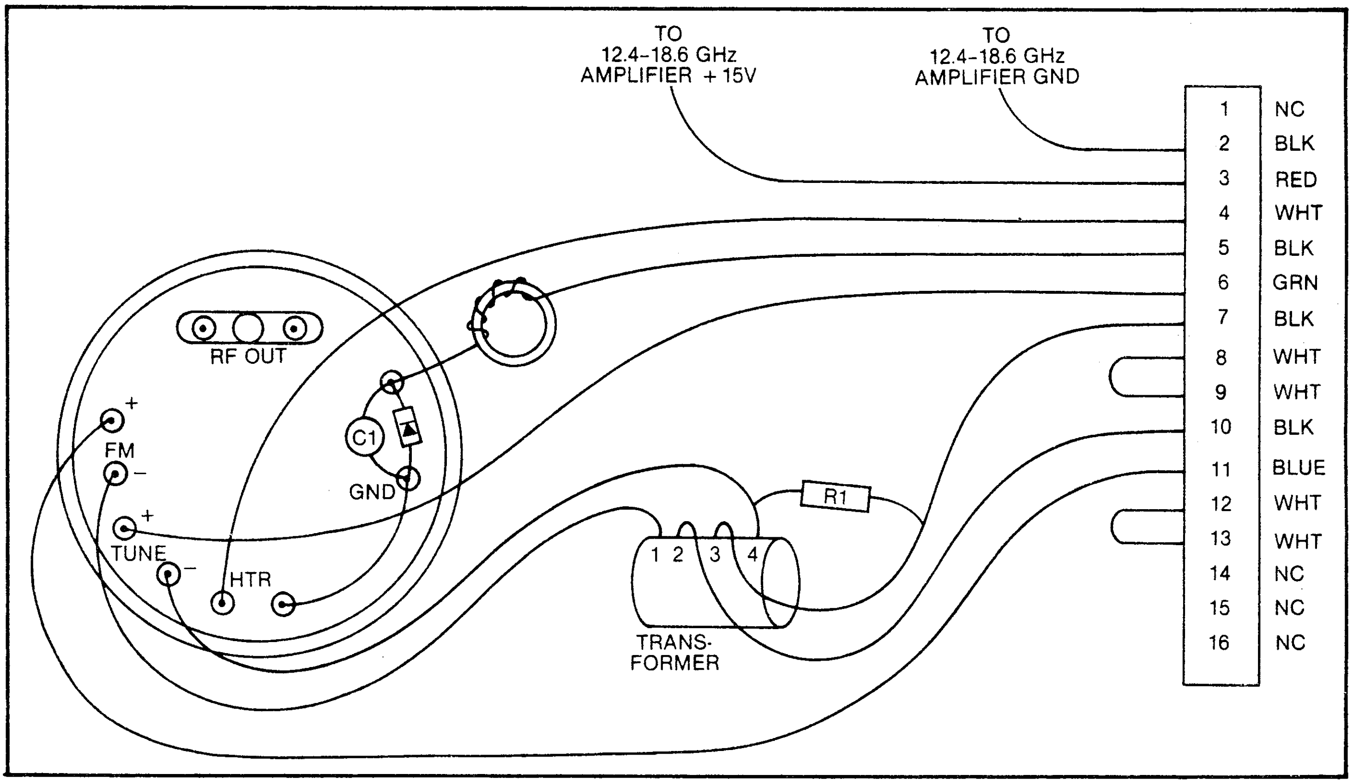


Figure 7-121. 6629A-40/6637A-40 A8 WJ Oscillator Wiring Diagram

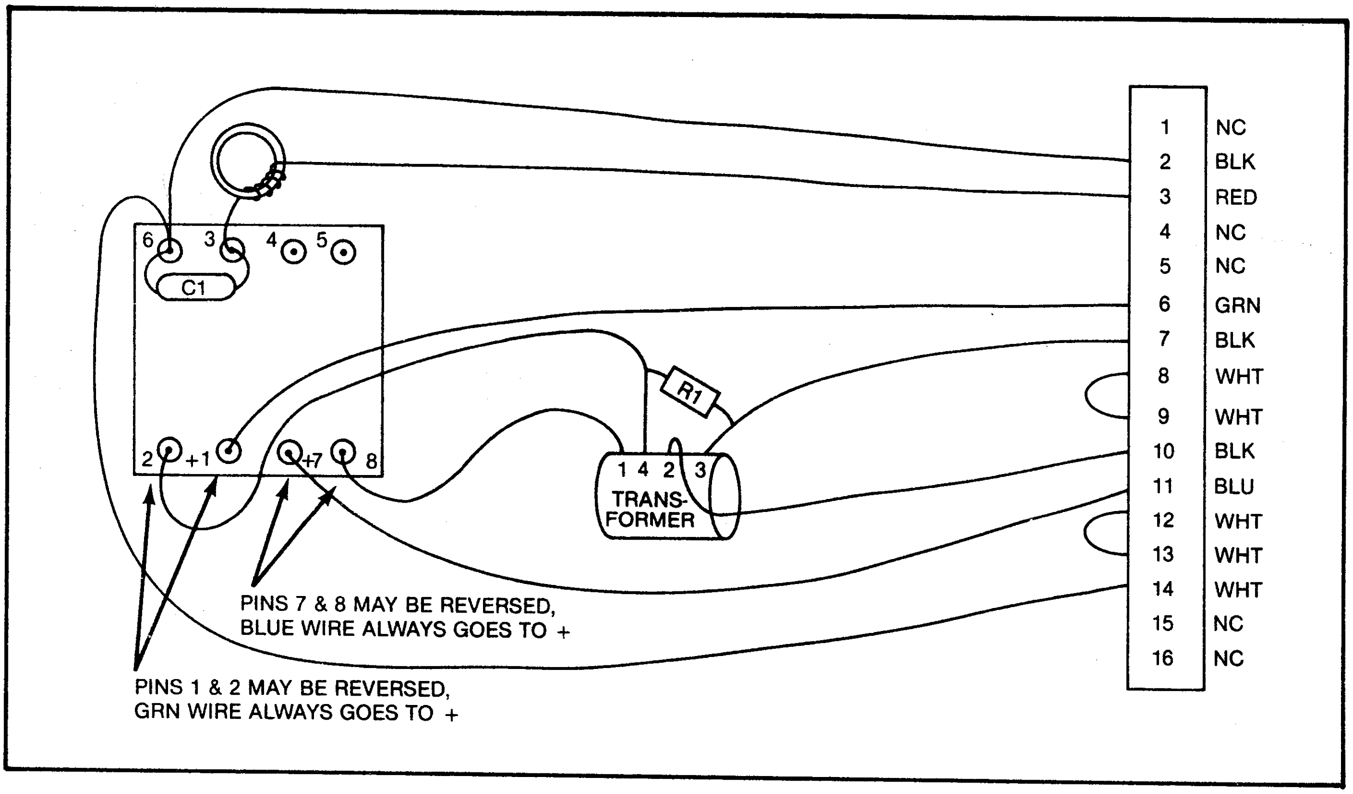


Figure 7-122. 6638A/6648A A8 Oscillator Wiring Diagram

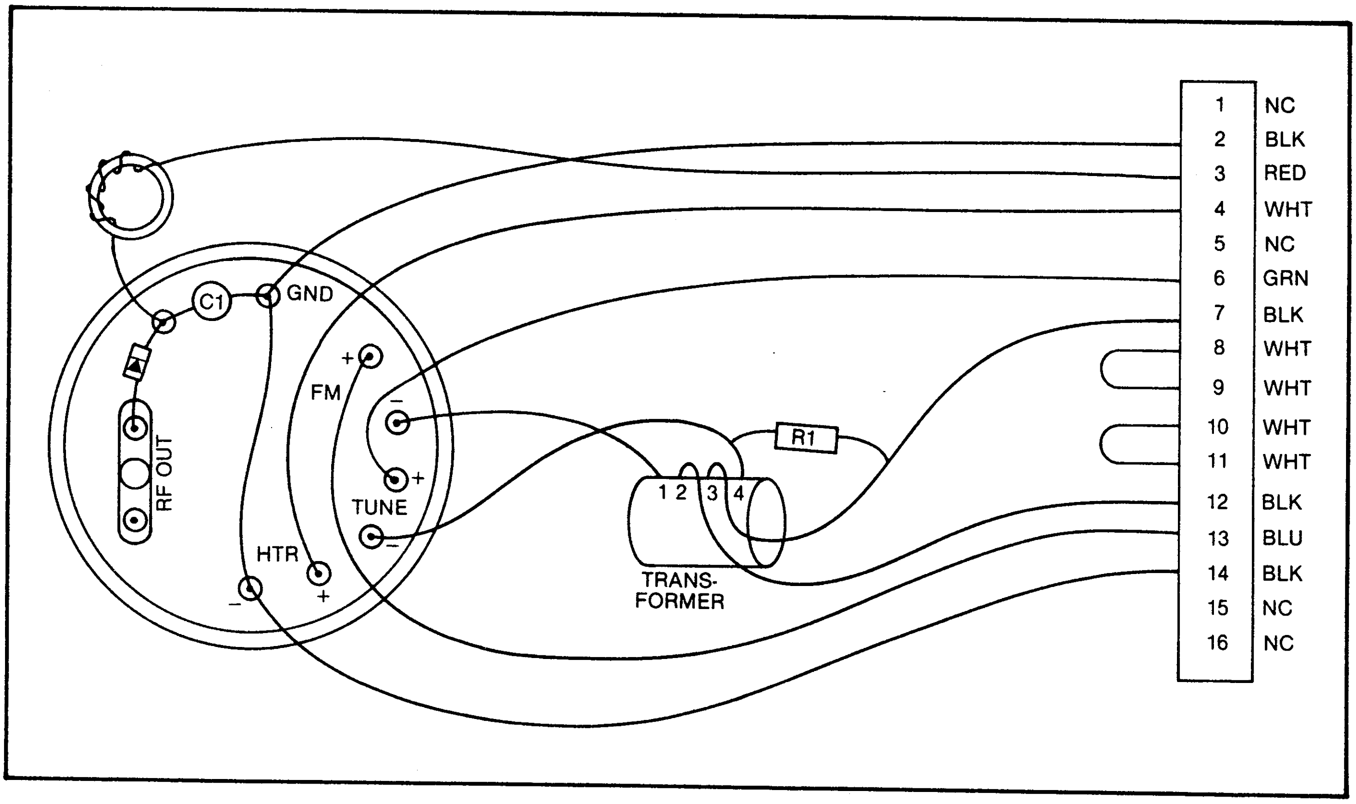


Figure 7-123. 6653A/6659A A8/A9 Avantek Oscillator Wiring Diagram

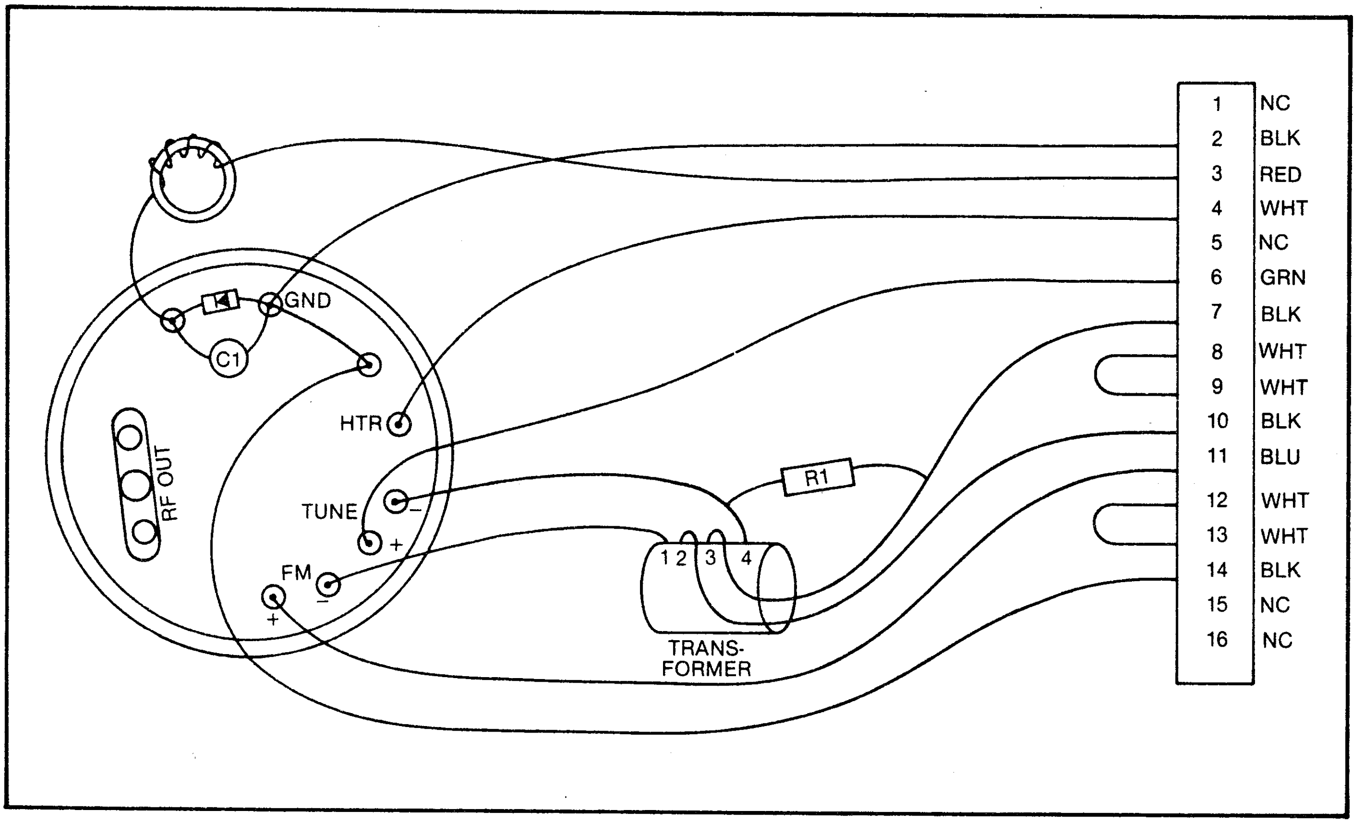


Figure 7-124. 6653A/6659A A8 WJ Oscillator Wiring Diagram

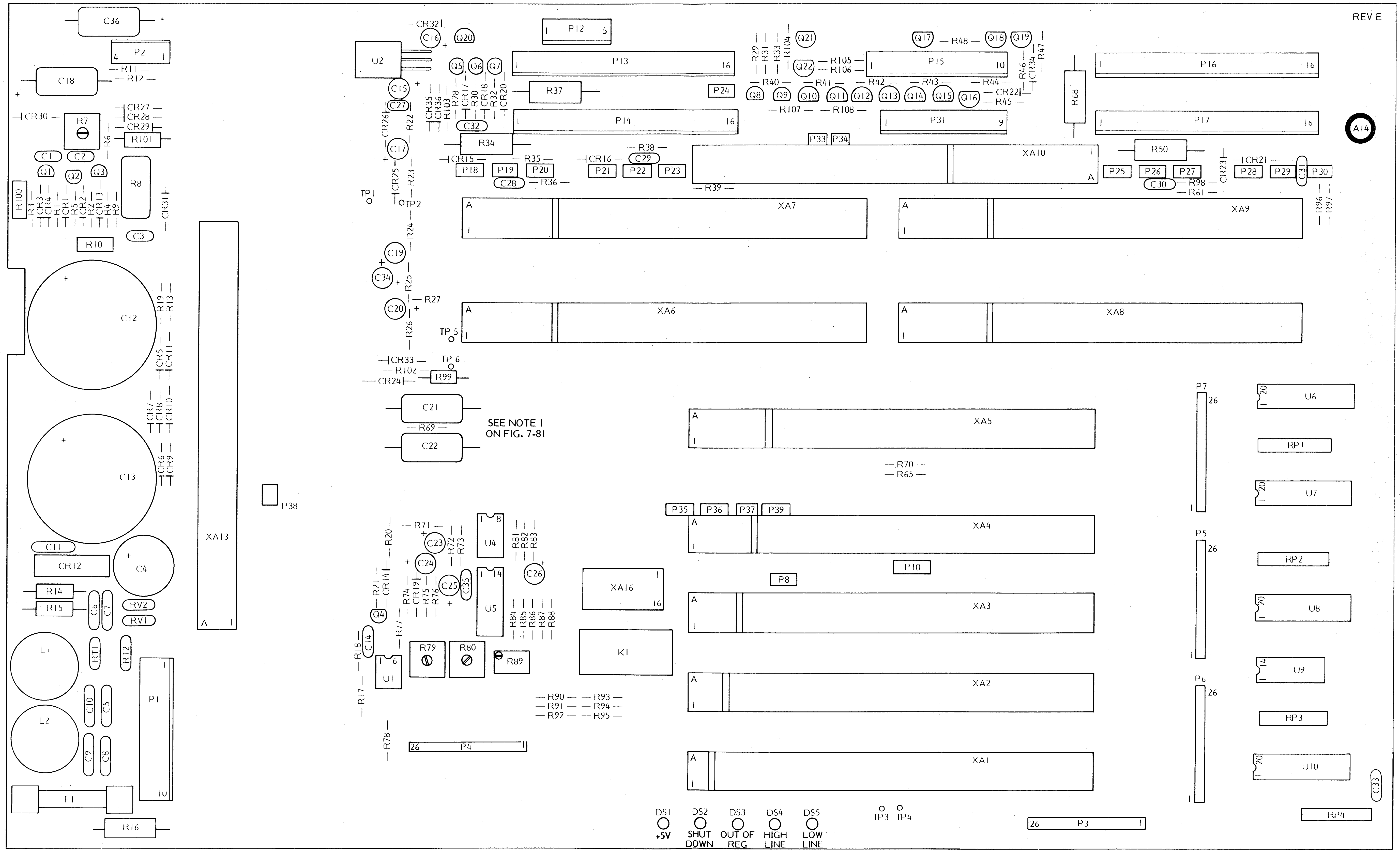


Figure 7-125. A14 Motherboard PCB Parts Locator Diagram

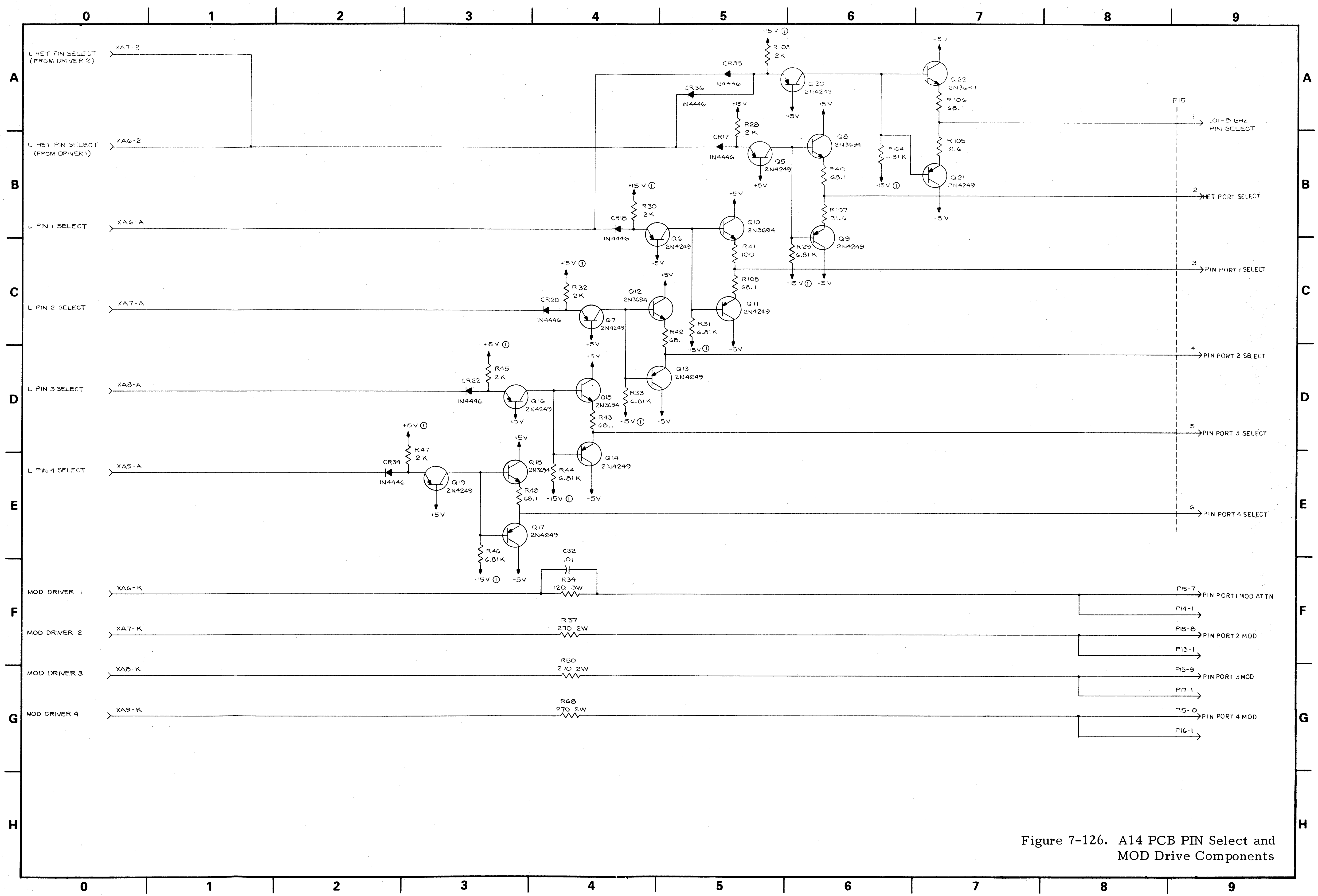
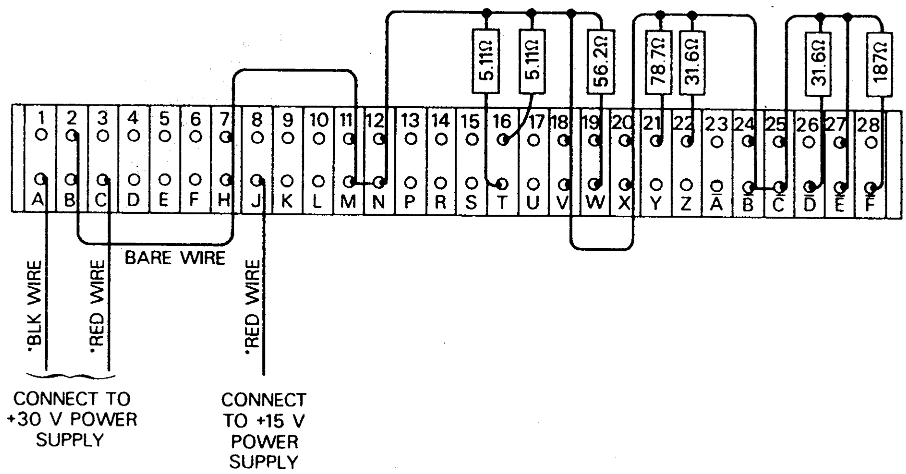


Figure 7-126. A14 PCB PIN Select and MOD Drive Components

A13 PCB TEST CONNECTOR - END VIEW



*WIRE SHOULD BE 24-GUAGE, APPROXIMATELY 2 FT IN LENGTH.

Resistor Legend

PURPOSE	PINS*	VALUE (OHMS)
Load for +5V Supply	16, T 17, U	5.11 (2 ea.)
Load for -18V Supply	22, Z 23, Ā	31.6
Load for +18V Supply	26, D̄	31.6
Load for -12/+24V Supply	19, W	56.2
Load for +28V Supply	21, Y	78.7
Load for -43V Supply	28, F̄	187

*Other resistor lead connects to ground bus

A13 Test Connector Parts List

NAME	WILTRON PART NO.
Connector-Receptacle, 56-pin	551-198
Resistor, 5.11Ω, 1/8W*	110-5.11-1
Resistor, 31.6Ω, 1/8W**	110-31.6-1
Resistor, 56.2Ω, 1/8W	110-56.2-1
Resistor, 78.7Ω, 1/8W	110-78.7-1
Resistor, 187Ω, 1/8W	110-187-1

*Resistor values are not critical.

**2 ea.

Figure 7-131. A13 PCB Test Connector

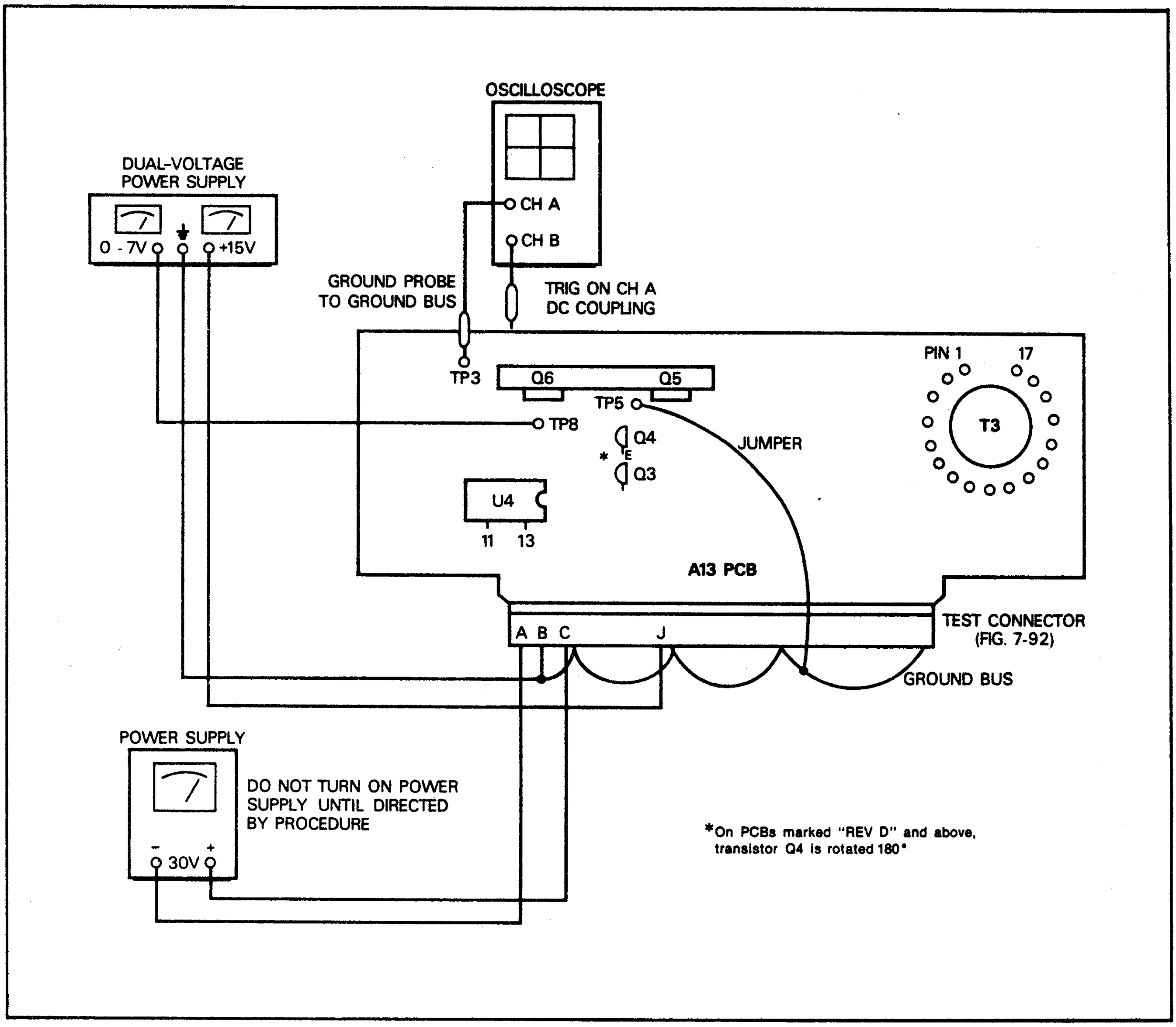


Figure 7-132. Test Equipment Setup for A13 PCB Benchtop Tests

Table 7-23. A13 PCB Low-Voltage Troubleshooting Procedure

General: This table provides instructions for troubleshooting the A14 PCB overcurrent-protection and A13 PCB voltage-supply circuits. The table, which is an extension of the "IS VOLTAGE 330V?" decision block in Figure 7-127, starts with the fact that (1) fuse A14F1 is blown, and (2) the A13 PCB caused it to blow.

Part 1 of this procedure describes troubleshooting the A14 overcurrent-protection circuit. This troubleshooting will detect whether Over-Current Sense IC U1 was destroyed by the over-current condition. Part 2 describes a low-voltage, benchtop method for troubleshooting the A13 PCB. Such a method is necessary because of the hazardous voltages present when the A13 PCB is operating from line voltage.

Part 1, Troubleshooting the A14 PCB Overcurrent-Protection Circuit

1. Turn off the sweep generator, disconnect the line cord, and wait at least 5 minutes for capacitor voltages to decay to a safe level.

2. Remove the voltage-protection shield from the underside of the A14 PCB.

3. Connect the positive (+) lead of a 3A, 3V dc power supply (HP 6281 or equivalent) to the lead on A14R6 that is nearest the rear panel.

4. Connect the positive (+) lead of a digital multimeter (DMM) to XA13, pin F or 6, and the negative (-) lead to chassis ground; set up the DMM to read ohms (10kΩ scale). A reading of ≈18kΩ should be observed.

5. Momentarily (≤5 seconds) touch the power supply's negative (-) lead to the other side of A14R16; observe the resistance reading on the DMM. A reading of <1 kΩ indicates that U1 is good.

NOTE

While the resistance of A14U1 is being read, ensure that (1) A14R16 draws 3 amps of current and (2) the voltage across it stays at 3 volts.

6. Replace faulty components and reinstall voltage-protection shield; then proceed to Part 2.

Part 2, Troubleshooting the A13 PCB Voltage-Supply Circuits

1. Remove the A13 PCB from the sweep generator and place on a suitable work surface.

2. Install the A13 PCB Test Connector (Figure 7-131).

3. Inspect the PCB and replace any obviously damaged components.

4. Remove the jumper from between test points 7 and 8, and connect a jumper between TP5 and the ground bus.

Table 7-23. A13 PCB Low-Voltage Troubleshooting Procedure (continued)

CAUTION

It is recommended that the A13 PCB be tagged with a label warning that the TP7-TP8 test jumper is removed. If this jumper is not in place while line voltage is applied, the switching power supply operates unregulated, and serious damage could occur to power supply circuits.

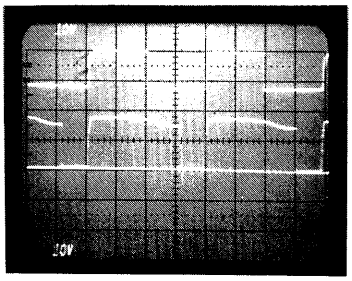
5. Connect the dual-voltage power supply as shown in Figure 7-132.

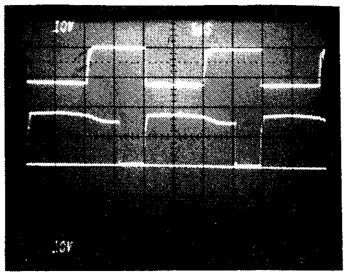
6. Turn on the power supply, and set the variable (0-7V) supply to +5 volts and the fixed (+15V) supply to +15 volts.

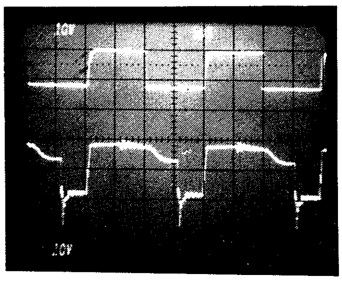
7. Connect the 30V supply as shown in Figure 7-132, but DO NOT TURN IT ON.

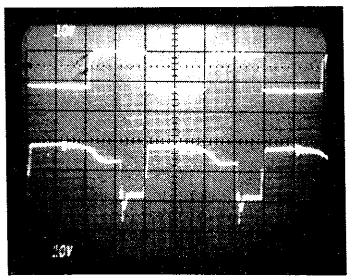
8. Connect Channel A of the oscilloscope to TP3 and observe the 50 kHz oscillator pulse. This pulse supplies the reference-timing pulse for future waveform analysis.

9. Using Channel B of the oscilloscope, check the waveforms at U4, pins 11 and 13, and at the emitters of Q3 and Q4. These waveforms should resemble those in figures "A" thru "D" below. Varying the +5V variable supply's voltage should cause the pulse width (PW) to vary: 0V should provide maximum PW, and ≈6.5V should shut the circuit down (both the test and sync signals will disappear).


U4, pin 11
A


U4, pin 13
B

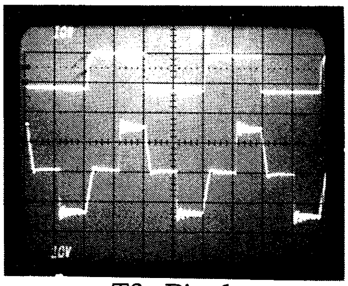

Q3-E
C


Q4-E
D

10. Reset the variable supply to +5 volts.

Table 7-23. A13 PCB Low-Voltage Troubleshooting Procedure (continued)

11. Turn on the 30-volt supply, and check the waveform at T3, pin 1. The waveform should resemble "E" below.



T3, Pin 1
E

12. Check the A13 output voltages at the "hot" side of the load resistors. As the input 0-7V supply is varied from min. to max., the A13 voltages should vary as shown below.

+5V Supply, Pin 16	from 0 to ≈ +0.6 volts
-18V Supply, Pin 22	from 0 to ≈ -2.5 volts
+18V Supply, Pin $\overline{D}$	from 0 to ≈ +2.5 volts
-12/+24V Supply, Pin 19	from 0 to ≈ -3.0 volts
+28V Supply, Pin 21	from 0 to ≈ +4.0 volts
-43V Supply, Pin $\overline{F}$	from 0 to ≈ -6.5 volts

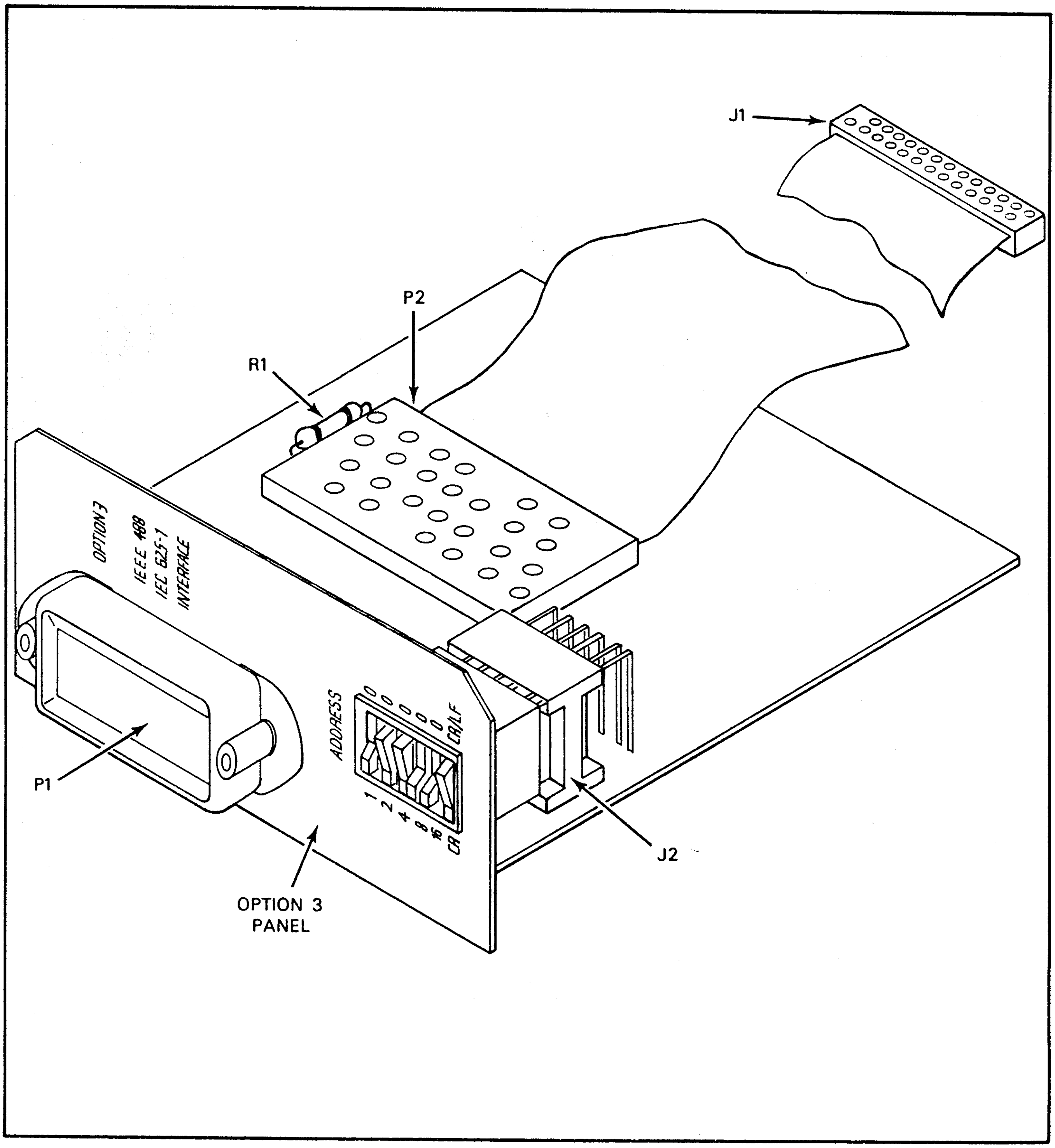
13. After completing the A13 tests and repairs, reinstall the jumper between test points 7 and 8 before reinstalling the PCB into the sweep generator.

CAUTION

To prevent possible damage to A13 should a short still exist, perform the following before applying full line voltage to the sweep generator:

- Inspect resistors A14R99, A14R100, and A14R101 for evidence of overheating. These resistors respectively fuse the -12/+24V, +28V, and +18V unregulated supplies.

- Use a variac to apply line power. Bring the line voltage up slowly while observing the A14 "SHUT DOWN" LED. If a short is still present, this LED should start flashing (A13 cycling on and off) between 80 and 100 Vac.



Option 3 (GP1B) Connector Panel

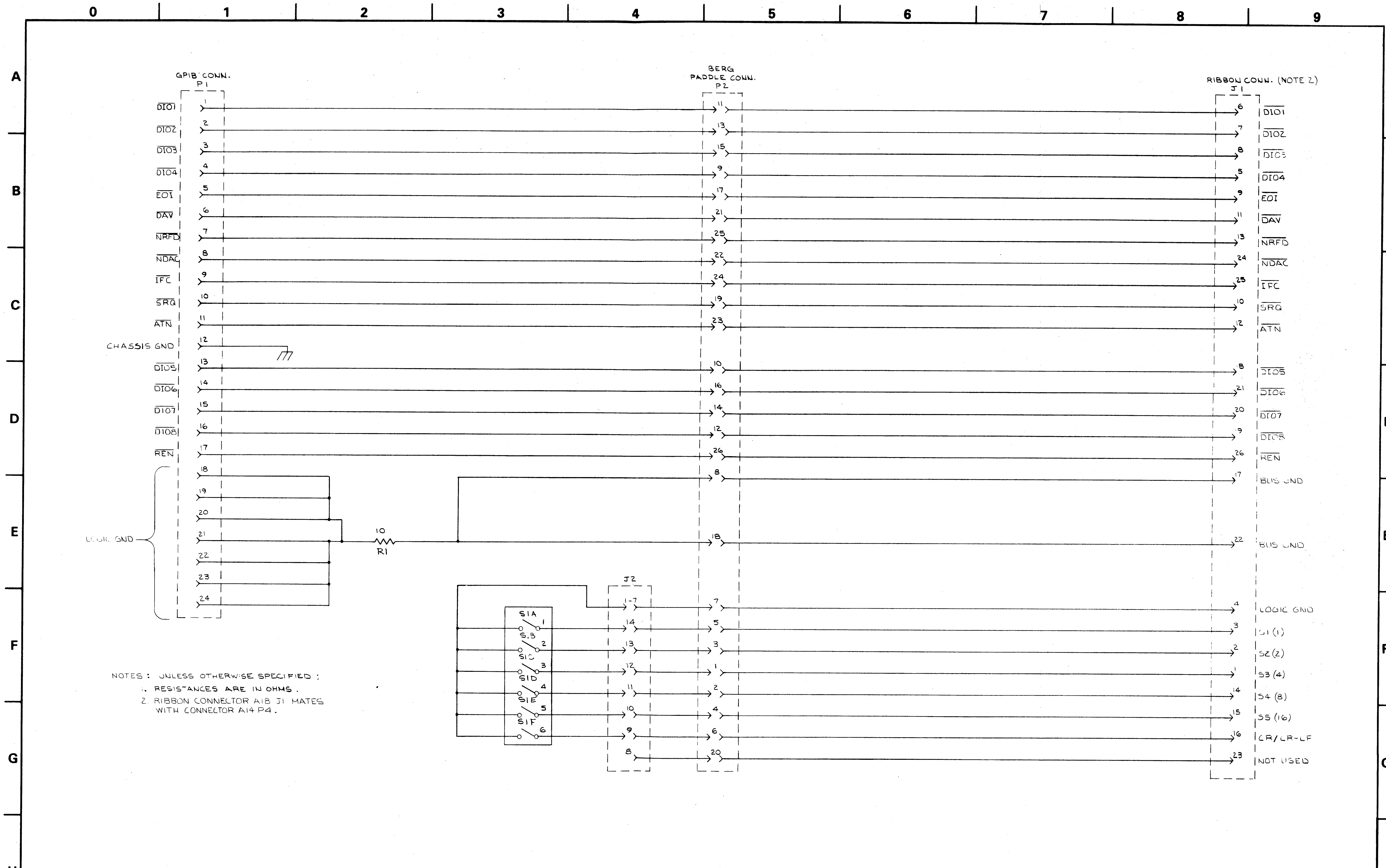


Figure 7-133. A18 GPIB Connector PCB Schematic

APPENDIX 1

QUICK REFERENCE DATA

Command Code Index

MNE-MONIC	NAME	TABLE NO.
AUT	Auto Trigger	3-9
CFØ	CW Select FØ	3-9
CF1	CW Select F1	3-9
CF2	CW Select F2	3-9
CLR	Clear Keypad	3-9
CM1	CW Select M1	3-9
CM2	CW Select M2	3-9
CNT	Continue Sweep	3-14
CS0	Horizontal Output Off During CW Operation	3-14
CS1	Horizontal Output On During CW Operation	3-14
DB	dB Data Terminator	3-9
DFØ	Sweep Range ΔF F0	3-9
DF1	Sweep Range ΔF F1	3-9
DL1	Detector Leveling	3-9
DLF	Enter ΔF Frequency	3-9
DM	dBm Data Terminator	3-9
DN	Decrement Selected Parameter	3-14
DSØ	Front Panel Displays Off	3-14
DS1	Front Panel Displays On	3-14
DWØ	Dwell at Marker Mode Off	3-12
DW1	Dwell at Marker Mode On	3-12
ESØ	End of Sweep Mode Off	3-12
ES1	End of Sweep Mode On	3-12
EXT	External Trigger	3-9
FØ	Enter Parameter FØ	3-9
F1	Enter Parameter F1	3-9
F2	Enter Parameter F2	3-9
FF	Sweep Range F1-F2	3-9
FLØ	CW Filter Off	3-14
FL1	CW Filter On	3-14
FMØ	Frequency Modulation Off	3-9
FM1	Frequency Modulation On	3-9
FUL	Sweep Range Full	3-9
FVØ	Frequency Vernier Off	3-9
FVS	Set Frequency Vernier	3-9
GH	GHz Data Terminator	3-9
GTD	GET* Mode Execute "DN" Command	3-11
GTN	GET Mode Execute "N" Command	3-11
GTS	GET Mode Trigger Sweep	3-11
GTU	GET Mode Execute "UP" Command	3-11
IL1	Internal Leveling	3-9
IM1	Intensity Marker	3-9
LIN	Line Trigger	3-9
LVØ	Leveling Off	3-9
LVL	Enter Level Parameter	3-9
M1	Enter M1 Parameter	3-9
M2	Enter M2 Parameter	3-9
MAN	Manual Sweep	3-9
MH	MHz Data Terminator	3-9
MKØ	Markers Off	3-9
MM	Sweep Range M1-M2	3-9
MS	Millisecond Data Terminator	3-9
N	Go to Next Increment (Digital Sweep)	3-10
ODF	Output ΔF Frequency	3-13
OI	Identify Instrument	3-13
OFØ	Output FØ Frequency	3-13
OF1	Output F1 Frequency	3-13
OF2	Output F2 Frequency	3-13
OFL	Output Low-End Frequency	3-13
OFH	Output High-End Frequency	3-13
OLV	Output RF Level	3-13
OM1	Output M1 Frequency	3-13
OM2	Output M2 Frequency	3-13
OSB	Output Status Byte	3-13
OST	Output Sweep Time	3-13
PEØ	Parameter Entry Error Mode Off	3-12
PE1	Parameter Entry Error Mode On	3-12
PL1	Power Meter Leveling	3-9
RCL	Recall Front Panel Setup	3-14
RFØ	RF Off	3-9
RF1	RF On	3-9
RL	Return to Local	3-14
RM1	RF Marker On	3-9
RSS	Reset Sweep	3-14
RST	Reset Front Panel	3-9
RTØ	RF During Retrace Off	3-9
RT1	RF During Retrace On	3-9
SAV	Save Front Panel Setup	3-14
SEØ	Syntax Error Mode Off	3-12
SE1	Syntax Error Mode On	3-12
SEC	Seconds Data Terminator	3-9
SH	Shift	3-9
SIZ	Increment Size	3-10
SQØ	SRQ Mode Off	3-12
SQ1	SRQ Mode On	3-12
STP	Step Sweep	3-10
STS	Step Select	3-10
SWT	Enter Sweep Time Parameter	3-9
TRS	Trigger Sweep	3-9
TST	Self Test	3-9
ULØ	Unleveled Condition Mode Off	3-12
UL1	Unleveled Condition Mode On	3-12
UP	Increment Selected Parameter	3-14
VM1	Video Marker On	3-9

*Group Execute Trigger

Default Settings

1. Front Panel Controls

   FREQUENCY RANGE: FULL (low and high-end frequencies are displayed)

   FM AND PHASELOCK: Off

   LEVELING: INTERNAL

   RF ON: On

   RETRACE RF: Off

   TRIGGER: AUTO

   MARKERS: All off

2. Front-Panel-Control-Related Bus Commands

   FULL

   FMØ

   IL1

   RF1

   RTØ

   AUT

   MKØ

3. Numeric Parameters

   See reverse side

Reset (Default) Setting for Numeric Parameters

All Models:
SWEEP TIME: 50 ms
LEVEL: Maximum Leveled Power (Table 1-1)
ΔF: 1000 Hz

Model: 6609A

F1: 10 MHz
F2: 2000 MHz
F0: 1000 MHz
M1: 500 MHz
M2: 1500 MHz

Model: 6617A

F1: 10 MHz
F2: 8000 MHz
F0: 4000 MHz
M1: 3000 MHz
M2: 7000 MHz

Model: 6621A

F1: 2000 MHz
F2: 12000 MHz
F0: 9000 MHz
M1: 3000 MHz
M2: 11000 MHz

Model: 6621A-40

F1: 2000 MHz
F2: 12000 MHz
F0: 9000 MHz
M1: 3000 MHz
M2: 11000 MHz

Model: 6629A

F1: 8000 MHz
F2: 18000 MHz
F0: 13000 MHz
M1: 9000 MHz
M2: 17000 MHz

Model: 6629A-40

F1: 8000 MHz
F2: 18000 MHz
F0: 13000 MHz
M1: 9000 MHz
M2: 17000 MHz

Model: 6637A

F1: 2000 MHz
F2: 18000 MHz
F0: 10000 MHz
M1: 3000 MHz
M2: 17000 MHz

Model: 6637A-40

F1: 2000 MHz
F2: 18000 MHz
F0: 10000 MHz
M1: 3000 MHz
M2: 17000 MHz

Model: 6638A

F1: 2000 MHz
F2: 20000 MHz
F0: 11000 MHz
M1: 3000 MHz
M2: 19000 MHz

Model: 6642A

F1: 18000 MHz
F2: 40000 MHz
F0: 25000 MHz
M1: 19000 MHz
M2: 39000 MHz

Model: 6647A

F1: 10 MHz
F2: 18000 MHz
F0: 10000 MHz
M1: 1000 MHz
M2: 17000 MHz

Model: 6648A

F1: 10 MHz
F2: 20000 MHz
F0: 10000 MHz
M1: 3000 MHz
M2: 19000 MHz

Model: 6653A

F1: 2000 MHz
F2: 26000 MHz
F0: 14000 MHz
M1: 3000 MHz
M2: 25000 MHz

Model: 6659A

F1: 10 MHz
F2: 26000 MHz
F0: 14000 MHz
M1: 3000 MHz
M2: 25000 MHz

APPENDIX 2

STEP SWEEP STEP-TO-FREQUENCY CONVERSION FORMULA

Formula:

$$F = F_{start} + \left[\frac{N}{4095} \times \left(F_{stop} - F_{start}\right)\right]$$

where F_{start} is the low end of the frequency sweep, as determined by sweep range programming (i.e., Full, F1-F2, M1-M2, etc.)

F_{stop} is the high end of the frequency sweep, as determined by sweep range programming.

N is the step number currently selected. The step number currently selected is found using the following formula:

$$N_{sts} + \left(N_{size} \times \text{number of times the "N" command has been executed}\right)$$

where N_{sts} is the Step Select (STS) Command number.

N_{size} is the Increment Size (SIZ) Command number.

For example, assume the following:

a. Front Panel Control-Related Programming:
   Sweep Range: ΔF, with FØ = 2 GHz and ΔF = 10 MHz
   Command: DFØ FØ2GH DLF1ØMH

b. Step Sweep Programming:
   Sweep Start = 0 volts
   Step Size = 819 steps
   No. of Frequency Points: 6
   Command: STP STSE SIZ819E N N N N N

Calculation to Find 1st Frequency Point:

N = 0 + (819 x 0)
F = 1.995 GHz

Calculation to Find 2nd Frequency Point:

N = 0 + (819 x 1)
= 819

$$F = 1.995 \times 10^9 + \left[\frac{819}{4095} \times (2.005 - 1.995)\right] \times 10^9$$

= 1.997 GHz

Calculation to Find 3rd Frequency Point:

N = 0 + (819 x 2)
= 1638

$$F = 1.995 \times 10^9 + \left[\frac{1638}{4095} \times (2.005 - 1.995)\right] \times 10^9$$

= 1.999

Frequencies at 4th, 5th, and 6th Frequency Points:

4th point = 2.001 GHz
5th point = 2.003 GHz
6th point = 2.005 GHz

APPENDIX 3
μP OUTPUT PORTS
(μP-TO-ANALOG INTERFACE)

Sixteen of the twenty-four microprocessor output ports are used to receive data on the analog PCBs. These ports are either octal-latch integrated circuits (ICs) or digital-to-analog converters that contain built-in octal latches. The digital data required for control or implementation of analog functions does not always require eight bits. More or less than eight bits are required for some functions; therefore, certain of the output ports have either:

- one port segmented so that it can be used to latch several different data control-groups of less than 8 bits, or
- two ports combined to latch data control-groups of greater than 8 bits.

The allocation of control-groups with output ports is shown in Table A3-1, and the control-groups are described in Table A3-2.

Table A3-1. Output Port Control Groups, with Correlation between µP Data Bus and Control Group Bits

PORT NO.	CONTROL GROUP	µP DATA BUS BITS WITH CORRESPONDING CONTROL-GROUP DATA BITS							
		B7	B6	B5	B4	B3	B2	B1	B0
0 1	1 LS MS	D7 D15	D6 D14	D5 D13	D4 D12	D3 D11	D2 D10	D1 D9	D0 D8
2	18	D7	D6	D5	D4	D3	D2	D1	D0
3 4	2	D7	D6	D5	D4	D3 D11	D2 D10	D1 D9	D0 D8
4	14				D0				
4	9	D2	D1	D0					
5	4	D7	D6	D5	D4	D3	D2	D1	D0
6 7	3	D7	D6	D5	D4	D3 D11	D2 D10	D1 D9	D0 D8
7	11	D3	D2	D1	D0				
8	5	D7	D6	D5	D4	D3	D2	D1	D0
9	6	D7	D6	D5	D4	D3	D2	D1	D0
10	7	D7	D6	D5	D4	D3	D2	D1	D0
11	8	D7	D6	D5	D4	D3	D2	D1	D0
12	12						D2	D1	D0
12	15			D2	D1	D0			
13 14	13	D7	D6	D5	D4	D3	D2	D1	D0 D8
14	10			D4	D3	D2	D1	D0	
14	23		D0						
14	16	D0							
15	20							D1	D0
15	22						D0		
15	19					D0			
15	17	D3	D2	D1	D0				

Table A3-2. Output Port Control Groups, Descriptions

CONTROL GROUP	NAME	NO. OF BITS	PORT NO.	DESCRIPTION
1	F center DAC	16	0, 1	Negative true logic representing a CW mode frequency or the center frequency in a sweep mode.
2	Step Frequency DAC	12	3, 4	Positive true logic representing the GPIB Step Sweep ramp count.
3	Sweep Width (ΔF) DAC	12	6, 7	Positive true logic representing the width of the frequency sweep.
4	ROM Linearizer Address DAC	8	5	Positive true logic containing the address of the selected linearizer ROM correction frequency.
5	ALC Reference DAC	8	8	Negative true logic representing the front panel LEVEL setting.
6	Marker F0 DAC	8	9	Positive true logic representing the F0 marker frequency.
7	Marker M1 DAC	8	10	Positive true logic representing the M1 marker frequency.
8	Marker M2 DAC	8	11	Positive true logic representing the M2 marker frequency.
9	Sweep Select	3	4	D2 D1 D0 Source of Ramp 0 1 1 A2 PCB ramp output 1 0 1 Step Frequency DAC output 1 1 1 MANUAL SWEEP potentiometer output
10	Trigger Mode	5	14	D4 D3 D2 D1 D0 0 0 0 0 0 Trigger disable 0 0 0 0 1 Auto trigger mode 0 0 0 1 0 Line trigger mode 0 0 1 0 0 Ext/Single Sweep mode 0 0 1 0 0 Reset ramp 0 0 1 0 0 Trigger ramp from zero
11	Wide/Medium/Narrow/CW	4	7	D2 D1 D0 1 1 1 CW select 0 1 1 Narrow sweep 1 0 1 Medium sweep 1 1 0 Wide sweep D3 0 ΔF≤200 MHz 1 ΔF>200 MHz
12	Marker Inhibit, F0, M1, M2	3	12	D2 D1 D0 1 1 1 All markers on 0 X X F0 marker off X 0 X M1 marker off X X 0 M2 marker off X = Don't care
13	Ramp Rate Select	9	13, 14	Bits D0-D7 are positive true logic bits representing the front panel SWEEP TIME setting. Bit D8 is the > or <1 second control bit. The coding for this bit is as follows: 0 = Sweep speed <1 second, 1 = Sweep speed >1 second.

Table A3-2. Output Port Control Groups, Descriptions (Continued)

CONTROL GROUP	NAME	NO. OF BITS	PORT NO.	DESCRIPTION
14	CW Filter On/Off	1	4	D0 0 CW filter in 1 CW filter out
15	Marker Mode Active	3	12	D2 D1 D0 0 0 0 Markers disabled 0 0 1 RF marker mode 0 1 0 Video marker mode 1 0 0 Intensity marker mode
16	External FM Ø Lock Enable	1	14	D0 0 Ext FM not enabled 1 Ext FM enabled
17	Programmable Attenuator (Option 2)	4	15	D3 D2 D1 D0 Attenuation 0 0 0 0 0 dB 0 0 0 1 -10 dB 0 0 1 0 -20 dB 0 0 1 1 -30 dB 0 1 0 0 -40 dB 0 1 0 1 -50 dB 0 1 1 0 -60 dB 0 1 1 1 -70 dB
18	Frequency Vernier (Freq Ver) DAC	8	2	Where word o equals zero (0000 0000), there is maximum negative frequency correction; o equals 128 (1000 0000), there is no frequency correction; o equals 255 (1111 1111), there is maximum positive frequency correction.
19	RF On/Off	1	15	D0 0 RF off 1 RF on
20	ALC Leveling Mode	2	15	D1 D0 0 0 Unleveled 0 1 Internal leveling 1 0 External detector 1 1 External power meter
21	Not used			
22	Retrace RF	1	15	D0 0 RF on during retrace 1 RF off during retrace
23	Sequential Sync Disable	1	14	When D0 bit is HIGH, the sequential sync pulse is disabled.